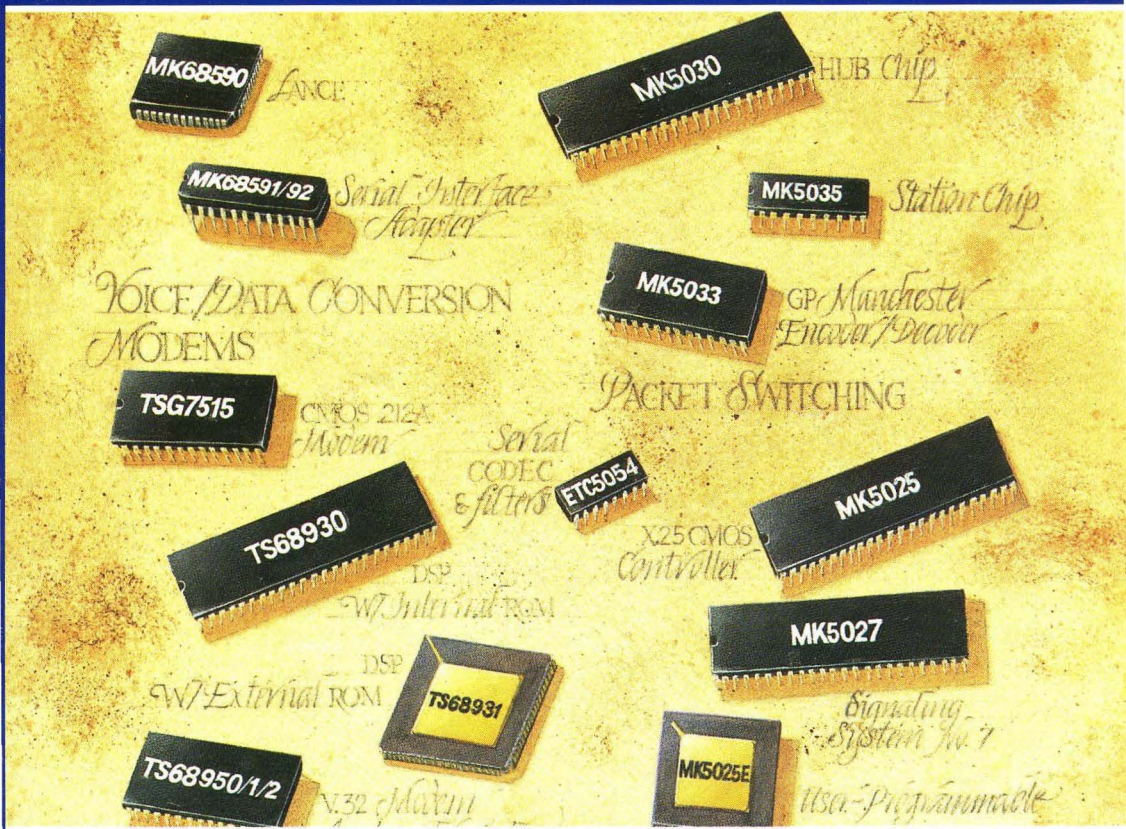
COMMUNICATIONS PRODUCTS

DATA BOOK



THOMSON
COMPONENTS
MOSTEK

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SUBSCRIBER BOARD ICs

CODEC II G (CODEC, FILTERS, & TIME SLOT ASSIGNMENT)

CODEC W/FILTER (COMBINATION)

CODEC's

FILTERS

SUBSCRIBER LINE INTERFACE CIRCUIT (SLIC)

TRUNK ICs

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DIALERS

REPERTORY TONEPULSE™ DIALERS

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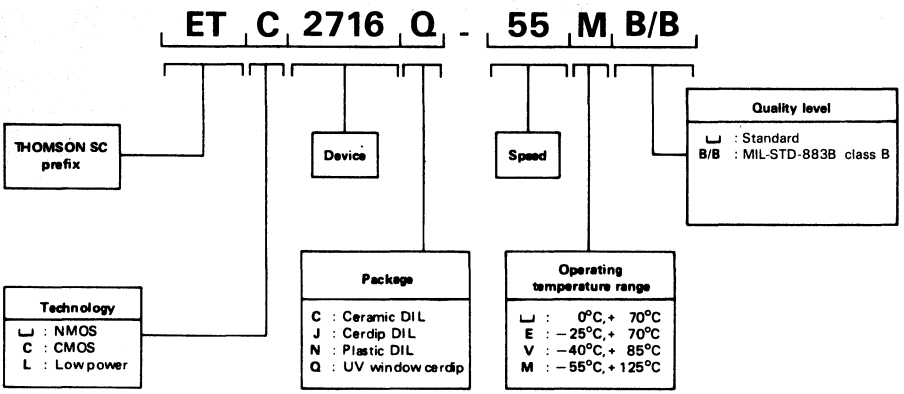
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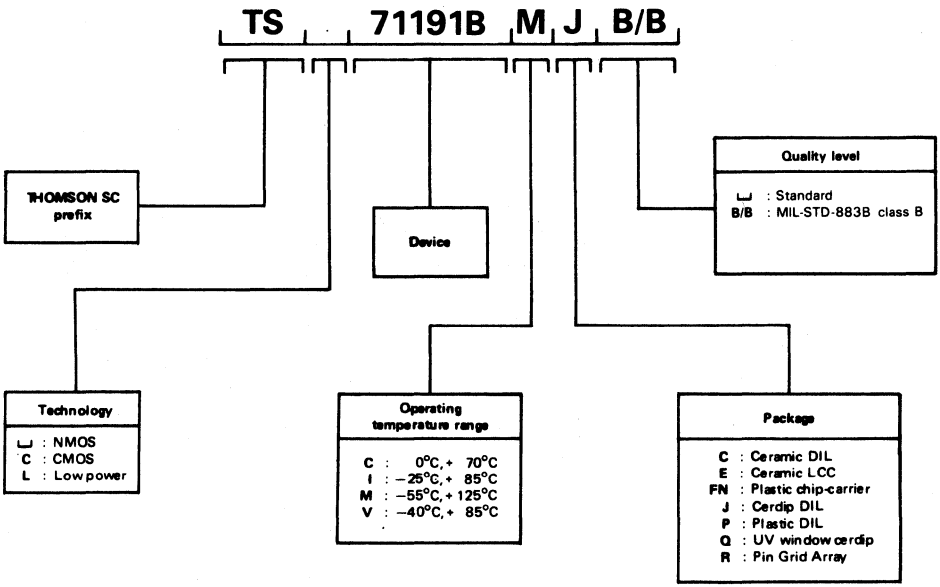
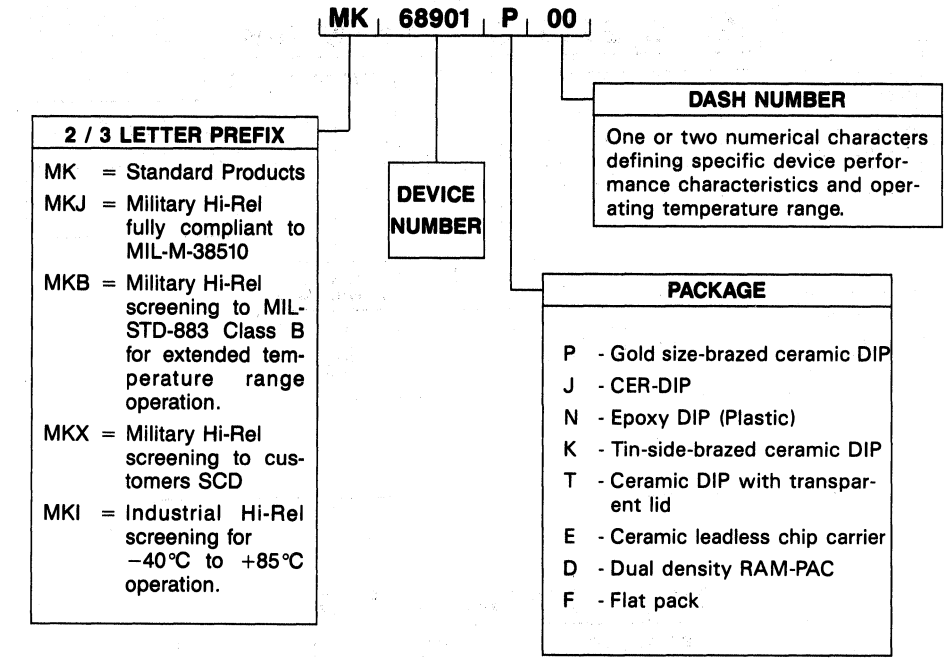
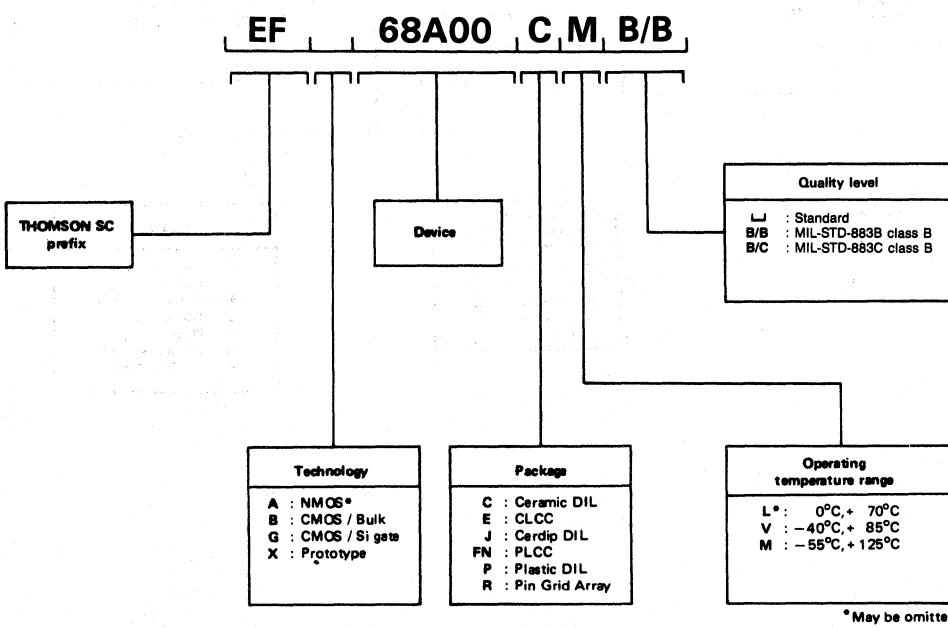
THOMSON SC prefix
Device
Speed
Quality level
␣ : Standard
B/B : MIL-STD-883B class B
Technology
␣ : NMOS
C : CMOS
L : Low power
Package
C : Ceramic DIL
J : Cerdip DIL
N : Plastic DIL
Q : UV window cerdip
Operating temperature range
␣ : 0°C, + 70°C
E : −25°C, + 70°C
V : −40°C, + 85°C
M : −55°C, + 125°C


TS 71191B M J B/B
THOMSON SC prefix
Device
Quality level
␣ : Standard
B/B : MIL-STD-883B class B
Technology
␣ : NMOS
C : CMOS
L : Low power
Operating temperature range
C : 0°C, + 70°C
I : −25°C, + 85°C
M : −55°C, + 125°C
V : −40°C, + 85°C
Package
C : Ceramic DIL
E : Ceramic LCC
FN : Plastic chip-carrier
J : Cerdip DIL
P : Plastic DIL
Q : UV window cerdip
R : Pin Grid Array


MK 68901 P 00
2 / 3 LETTER PREFIX
MK = Standard Products
MKJ = Military Hi-Rel fully compliant to MIL-M-38510
MKB = Military Hi-Rel screening to MIL-STD-883 Class B for extended temperature range operation.
MKX = Military Hi-Rel screening to customers SCD
MKI = Industrial Hi-Rel screening for −40°C to +85°C operation.
DEVICE NUMBER
DASH NUMBER
One or two numerical characters defining specific device performance characteristics and operating temperature range.
PACKAGE
P - Gold size-brazed ceramic DIP
J - CER-DIP
N - Epoxy DIP (Plastic)
K - Tin-side-brazed ceramic DIP
T - Ceramic DIP with transparent lid
E - Ceramic leadless chip carrier
D - Dual density RAM-PAC
F - Flat pack


EF 68A00 C M B/B
THOMSON SC prefix
Device
Quality level
␣ : Standard
B/B : MIL-STD-883B class B
B/C : MIL-STD-883C class B
Technology
A : NMOS*
B : CMOS / Bulk
G : CMOS / Si gate
X : Prototype
Package
C : Ceramic DIL
E : CLCC
J : Cerdip DIL
FN : PLCC
P : Plastic DIL
R : Pin Grid Array
Operating temperature range
L* : 0°C, + 70°C
V : −40°C, + 85°C
M : −55°C, + 125°C
*May be omitted.

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CHAPTER 1 - DATA COMMUNICATIONS

THOMSON COMPONENTS MOSTEK

MK5025

PRELIMINARY

COMMUNICATIONS PRODUCTS

FEATURES

- ☐ CMOS
- ☐ Fully compatible with both 8 or 16 bit systems.
- ☐ System clock rate to 10 MHz.
- ☐ Data rate up to 7 MBPS with 64 byte FIFOs in each direction.
- ☐ Complete Data Link Layer Implementation.
- ☐ Compatible with X.25 LAPB, ISDN LAPD, X.32, and X.75 Link Level Protocols.
- ☐ 48-pin DIP nearly pin-for-pin compatible with the Mostek LANCE chip (MK68590).
- ☐ Buffer Management includes:
  - — Initialization Block
  - — Separate Receive and Transmit Rings
  - — Variable Descriptor Ring and Window Size.
- ☐ On chip DMA control and programmable burst length.
- ☐ Selectable single or extended control field.
- ☐ Programmable 1 or 2 byte address field and Global Address.
- ☐ Handles all HDLC (ADCCP) frame formatting:
  - — Zero bit insert and delete
  - — FCS generation and detection
  - — Frame delimiting with flags.
- ☐ Handles all error recovery, sequencing, and S and U frame control.
- ☐ Transparent mode with or without address filtering allows disabling X.25 processing for customized applications.
- ☐ Selectable FCS of 16 or 32 bits.
- ☐ Data Link Services:
  - — Compatible with ISO Data Link Services
  - — Compatible with LAPD Data Link Services.
- ☐ Testing Facilities:
  - — Internal Loopback
  - — Silent Loopback
  - — Optional Internal Data Clock Generation
  - — Self Test.

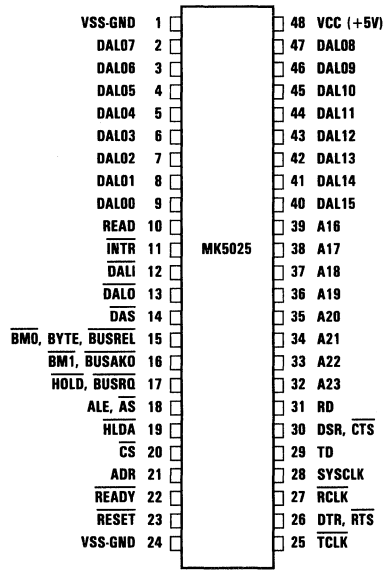


Figure 1. Pin Connection

- ☐ All inputs and outputs are TTL compatible.
- ☐ Programmable for Full or Half Duplex operation.
- ☐ Programmable minimum frame spacing on transmit (flags between frames).

DESCRIPTION

The Thomson Components - Mostek X.25 Link Level Controller (MK5025) is a VLSI semiconductor device which provides a complete link level data communication control conforming to the 1984 CCITT version of X.25. This includes frame formatting, transparency (so-called "bit-stuffing"), error recovery by retransmission, sequence number control, U (unnumbered) frame control, and S (supervisory) frame control. The MK5025 also supports X.32 (XID), X.75, and ISDN LAPD. The MK5025 may be used with any of several popular 16 and 8 bit microprocessors, such as 68000, 6800, Z8000, Z80, LSI-11, 8086, 8088, 8080, etc.

PIN DESCRIPTION

LEGEND:

I	Input only	3S	3-State
O	Output only	OD	Open Drain (no internal pull-up)
IO	Input/Output		Active low (i.e. inverted)

SIGNAL NAME	PIN(S)	TYPE	DESCRIPTION
DAL<07:00>	2-9	IO/3S	The time multiplexed Data/Address bus. During the address portion of the memory transfer, DAL<07:00> contains the lower 8 bits of the memory address. During the data portion of a memory transfer, DAL <07:00> contains the read or write data, depending on the type of transfer.
READ	10	IO/3S	READ indicates the type of operation that the bus controller is performing during a bus transaction. READ is driven by the MK5025 only while it is the BUS MASTER. READ is valid during the entire bus transaction and is tristated by the MK5025 at all other times. MK5025 as a Bus Slave READ = HIGH - Data is placed on the DAL lines by the MK5025. READ = LOW - Data is taken from the DAL lines by the MK5025. MK5025 as a Bus Master READ = HIGH - Data is taken from the DAL lines by the MK5025. READ = LOW - Data is placed on the DAL lines by the MK5025.
$\overline{INTR}$	11	O/OD	INTERRUPT is an attention interrupt line that indicates that one or more of the following CSR0 status flags is set: MISS, MERR, ROR, TUR, RINT, TINT or PINT. INTERRUPT is enabled by CSR0<09>, INEA=1.
$\overline{DALI}$	12	O/3S	DAL IN is an external bus transceiver control line. $\overline{DALI}$ is driven by the MK5025 only while it is the BUS MASTER. $\overline{DALI}$ is active when it reads from the DAL lines during the data portion of a READ transfer. $\overline{DALI}$ is inactive during a WRITE transfer.
$\overline{DALO}$	13	O/3S	DAL OUT is an external bus transceiver control line. $\overline{DALO}$ is driven by MK5025 only while it is the BUS MASTER. $\overline{DALO}$ is asserted by MK5025 when the MK5025 drives the DAL lines during the address portion of a READ transfer or for the duration of a WRITE transfer.
$\overline{DAS}$	14	IO/3S	DATA STROBE defines the data portion of a bus transaction. By definition data is stable and valid at the low to high transition of $\overline{DAS}$. This signal is driven by the MK5025 while it is the BUS MASTER. At all other times the signal is tristated.
$\overline{BM0}$ BYTE $\overline{BUSREL}$	15	IO/3S	I/O pins 15 and 16 are programmable through CSR4. If bit 06 of CSR4 is set to a one, pin 15 becomes input $\overline{BUSREL}$ and is used by the host to signal the MK5025 to terminate a DMA Burst after the current bus transfer has completed. If bit 06 is set to a zero, pin 15 is an output and behaves as described below for pin 16.
$\overline{BM1}$ $\overline{BUSAKO}$	16	O/3S	Pins 15 and 16 are programmable through bit 00 of CSR4 (BCON). If CRS4<00> BCON = 0, I/O PIN 15 = $\overline{BM0}$ (O/3S) I/O PIN 16 = $\overline{BM1}$ (O/3S) BYTE MASK<1:0> Indicates the byte(s) on the DAL to be read or written

SIGNAL NAME	PIN(S)	TYPE	DESCRIPTION

during this bus transaction. MK5025 drives these lines only as a Bus Master. MK5025 ignores the BM lines when it is a Bus Slave.

Byte selection is done as outlined in the following table.

$\overline{BM1}$	$\overline{BM0}$	
LOW	LOW	ENTIRE WORD
LOW	HIGH	UPPER BYTE (DAL<15:08>)
HIGH	LOW	LOWER BYTE (DAL<07:00>)
HIGH	HIGH	ILLEGAL CONDITION

If CSR4<00> BCON = 1,
I/O PIN 15 = $\overline{BYTE}$ (O/3S)
I/O PIN 16 = $\overline{BUSAKO}$ (0)

Byte selection is done using the BYTE line and DAL<00> latched during the address portion of the bus transaction. MK5025 drives BYTE only as a Bus Master and ignores it when a Bus Slave. Byte selection is done as outlined in the following table.

$\overline{BYTE}$	DAL<00>	
LOW	LOW	ENTIRE WORD
LOW	HIGH	ILLEGAL CONDITION
HIGH	LOW	LOWER BYTE
HIGH	HIGH	UPPER BYTE

$\overline{BUSAKO}$ is a bus request daisy chain output. If MK5025 is not requesting the bus and it receives $\overline{HLDA}$, $\overline{BUSAKO}$ will be driven low. If MK5025 is requesting the bus when it receives $\overline{HLDA}$, $\overline{BUSAKO}$ will remain high.

$\overline{HOLD}$
$\overline{BUSRQ}$ 17 IO/OD Pin 17 is programmable through bit 00 of CSR4.
IF CSR4<00> BCON = 0,
I/O PIN 17 = $\overline{HOLD}$

$\overline{HOLD}$ request is asserted by the MK5025 when it requires a DMA cycle regardless of the previous state of the $\overline{HOLD}$ pin. $\overline{HOLD}$ is held low for the entire ensuing bus transaction.

IF CSR4<00> BCON = 1,
I/O PIN 17 = $\overline{BUSRQ}$

$\overline{BUSRQ}$ is asserted by the MK5025 when it requires a DMA cycle if the prior state of the $\overline{BUSRQ}$ pin was high. $\overline{BUSRQ}$ is held low for the entire ensuing bus transaction.

ALE
$\overline{AS}$ 18 O/3S The active level of ADDRESS STROBE is programmable through bit 01 of CSR4. The address portion of a bus transfer occurs while this signal is at its asserted level. This signal is driven by the MK5025 while it is the BUS MASTER. At all other times, the signal is tristated.

IF CSR4<01> ACON = 0,
I/O PIN 18 = ALE

ADDRESS LATCH ENABLE is used to demultiplex the DAL lines and define the address portion of the transfer. As ALE, the signal transitions from high to low during the address portion of the transfer and remains low during the data portion.

SIGNAL NAME	PIN(S)	TYPE	DESCRIPTION
			IF CSR4<01> ACON = 1, I/O PIN 18 = $\overline{AS}$ As $\overline{AS}$, the signal pulses low during the address portion of the bus transfer. The low to high transition of $\overline{AS}$ can be used by a slave device to strobe the address into a register.
$\overline{HLDA}$	19	I	HOLD ACKNOWLEDGE, is the response to $\overline{HOLD}$. When $\overline{HLDA}$ is low in response to MK5025's assertion of $\overline{HOLD}$, the MK5025 is the Bus Master. $\overline{HLDA}$ should be disasserted ONLY after $\overline{HOLD}$ has been released by MK5025.
$\overline{CS}$	20	I	CHIP SELECT indicates, when low, that the MK5025 is the slave device for the data transfer. $\overline{CS}$ must be valid throughout the entire transaction.
ADR	21	I	ADDRESS selects the Register Address Port or the Register Data Port. It must be valid throughout the data portion of the transfer and is only used by the chip when $\overline{CS}$ is low. ADR — PORT LOW — REGISTER DATA PORT HIGH — REGISTER ADDRESS PORT
$\overline{READY}$	22	IO/OD	When the MK5025 is a Bus Master, $\overline{READY}$ is an asynchronous acknowledgement from the bus memory that memory will accept data in a WRITE cycle or that memory has put data on the DAL lines in a READ cycle. As a Bus Slave, the MK5025 asserts $\overline{READY}$ when it has put data on the DAL lines during a READ cycle or is about from take data off the DAL lines during a WRITE cycle. $\overline{READY}$ is a response to $\overline{DAS}$ and it will be negated after $\overline{DAS}$ is negated.
$\overline{RESET}$	23	I	$\overline{RESET}$ is the Bus signal that will cause MK5025 to cease operation, clear its internal logic and enter an idle state.
$\overline{TCLK}$	25	I	TRANSMIT CLOCK. A 1X clock input for transmitter timing. TD changes on the falling edge of $\overline{TCLK}$. The frequency of $\overline{TCLK}$ may be up to 7 Mbps.
DTR $\overline{RTS}$	26	IO	DATA TERMINAL READY, REQUEST TO SEND. Modem Control Pin. Pin 26 is configurable through CSR5. This pin can be programmed to behave as output $\overline{RTS}$ or as a programmable IO pin DTR. If configured as $\overline{RTS}$, the MK5025 will assert this pin if it has data to send and throughout transmission of a frame.
$\overline{RCLK}$	27	I	RECEIVE CLOCK. A 1X clock input for receiver timing. RD is sampled on the rising edge of $\overline{RCLK}$. The frequency of $\overline{RCLK}$ may be up to 7 MHz.
SYSCLK	28	I	SYSTEM CLOCK. System clock used for internal timing of MK5025. SYSCLK should be a square wave, and be greater than 500 KHz and less than 10 MHz.
TD	29	O	TRANSMIT DATA. Transmit serial data output.
DSR $\overline{CTS}$	30	IO	DATA SET READY, CLEAR TO SEND. Modem Control Pin. Pin 30 is configurable through CSR5. This pin can be programmed to behave as input $\overline{CTS}$ or as a programmable IO pin DSR. If configured as $\overline{CTS}$, the MK5025 will transmit all 1's while $\overline{CTS}$ is high.

SIGNAL NAME	PIN(S)	TYPE	DESCRIPTION
RD	31	I	RECEIVE DATA. Received serial data input.
A<23:16>	32-39	O/3S	Address bits <23:16> used in conjunction with DAL<15:00> to produce a 24 bit address. MK5025 drives these lines only as a Bus Master.
DAL<15:08>	40-48	IO/3S	The time multiplexed Data/Address bus. For 16-bit operations, DAL<15:08> behaves similar to DAL<07:00> above for the high byte of data or the middle byte of the 24 bit address. For 8-bit operations, DAL<15:08> behaves similar to A <23:16> for the middle byte of the 24-bit address only.
VSS-GND	1, 24		Ground - 0 VDC
VCC	48		Power Supply Pin. +5.0 VDC ±5%

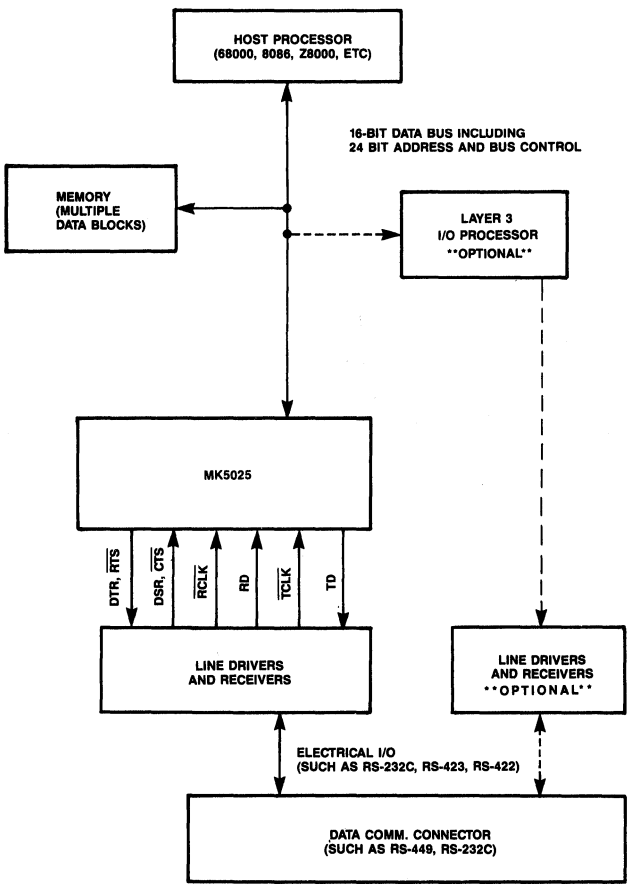


Figure 2. Possible System Configuration for the MK5025

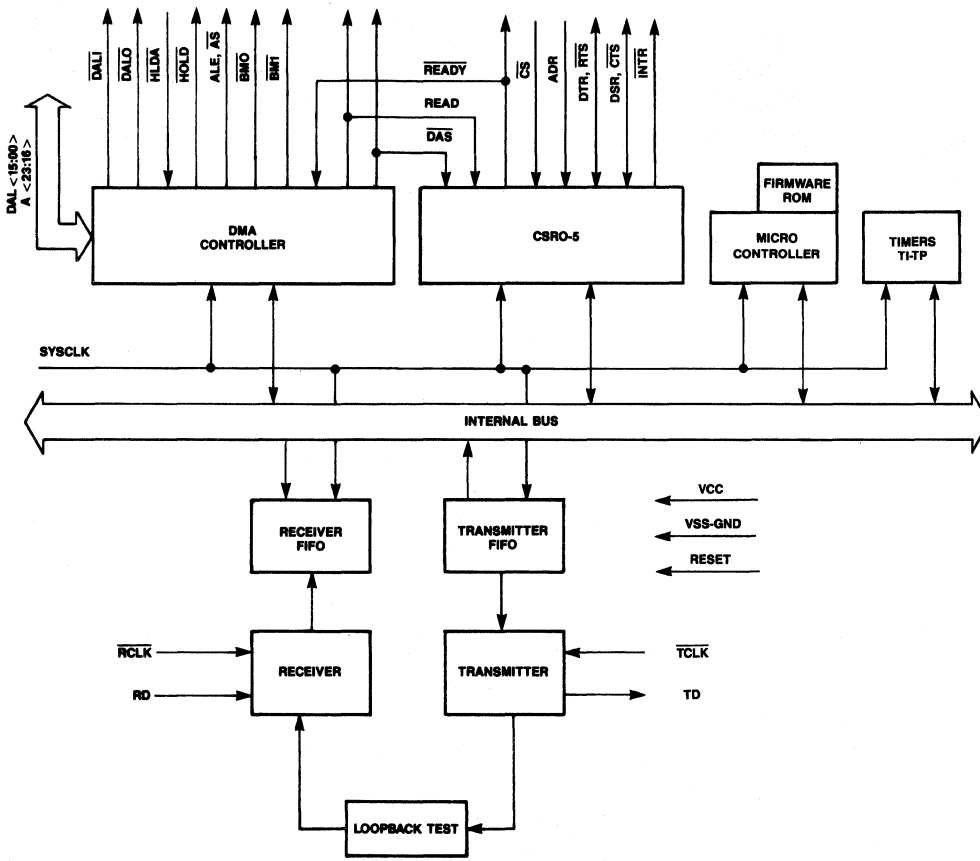


Figure 3. MK5025 Simplified Block Diagram

OPERATIONAL DESCRIPTION

The Mostek X.25 Link Controller (MK5025) device is a VLSI product intended for data communication applications requiring X.25 link level control (LAPB). The MK5025 will perform all frame formatting, such as frame delimiting with flags, FCS generation and detection, as well as zero-bit insertion and deletion for transparency. The MK5025 also includes a buffer management mechanism that allows the user to transmit and/or receive multiple packets. Contained in the buffer management is an on-chip dual channel DMA: one channel for receive and one channel for transmit. The MK5025 handles all supervisory (S) and unnumbered (U) frames. (See Table I.)

The MK5025 is intended to be used with any popular 16 or 8 bit microprocessor. A possible system configuration for the MK5025 is shown in figure 2.

The MK5025 will move multiple blocks of receive and transmit data directly into and out of memory through the Host's bus. An I/O acceleration processor can be used to off-load Network Level software from the Host. The I/O acceleration processor in figure 2 is recommended, but not required.

All signal pins on the MK5025 are TTL compatible. This has the advantage of making the MK5025 independent of the physical interface. As shown in Fig. 2, line drivers and receivers are used for electrical connection to the physical layer.

SERIAL INTERFACE

The MK5025 provides two seperate serial channels; one for received data and one for transmitted data. These serial channels are completely seperate and may be run at different clock frequencies up to 7 MHz. The receiver is responsible for recognizing frame boundaries, removal of inserted zeroes (for transparency), and checking the incoming FCS. Frames with incorrect FCS values are discarded. The receiver also parallelizes the incoming data which is placed into the receive data buffers within the receive descriptor ring. The receiver also recognizes link idle and frame abort sequences. The transmitter is responsible for framing and serializing the data frames placed in the transmit descriptor ring. The transmitter calculates the FCS of the outgoing data and appends it to the data. The transmitter generates flag sequences for interframe fill, at least two flags are transmitted between adjacent frames. The FCS calculations for both directions of serial data optionally follow either the 16-bit CRC-CCITT or the 32-bit CRC-32 algorithms. FCS generation and checking can also be optionally disabled if defined.

MICROPROCESSOR INTERFACE

The MK5025 can interface with the host bus in two ways: either as bus master or as a bus peripheral. The MK5025 contains a dual channel DMA on chip to handle data transfers to and from the host memory. All access to the initialization block and descriptor rings is handled in this way. The address bus is 24 bits wide and does not use any segmentation or paging methods. Data transfers can optionally be 8 and 16 bit operations, this allows easy interfacing with both 8 and 16 bit processors. DMA transfers can be up to 1, 8 or an unlimited number of words per transfer under program control. In bus slave mode the MK5025 allows access to its 6 control/status registers which are used to monitor and control the chip. These registers are used to control link procedures, configure interface options, control and monitor interrupt status, and more. Bus slave mode also allows both 8 and 16 bit accesses.

BUFFER MANAGEMENT

The basic organization of the buffer management is a circular queue of tasks in memory called descriptor rings. There are separate rings to describe the transmit and receive operations. Up to 128 buffers may be queued-up on a descriptor ring awaiting execution by the MK5025. The descriptor ring has a segment assigned to each buffer. Each segment holds a pointer for the starting address of the buffer, and holds a value for the length of the buffer in words (16 bits).

Each segment also contains two control bits called OWNA and OWNB, which denote whether the MK5025, the HOST, or the I/O ACCELERATION Processor (if present) "owns" the buffer. For transmit, when the MK5025 owns the buffer, the MK5025 is allowed and commanded to transmit the buffer. When the MK5025 does not own the buffer, it will not transmit that buffer. For receive, when the MK5025 owns a buffer, it may place received data into that buffer. Conversely, when the MK5025 does not own a receive buffer, it will not place received data in that buffer.

The MK5025 buffer management mechanism will handle frames which are longer than the length of an individual buffer. This is done by a chaining method which utilizes multiple buffers. The MK5025 tests the next segment in the descriptor ring in a "look ahead" manner. If the packet is too long for one buffer, the next buffer will be used after filling the first buffer; that is, "chained". The MK5025 will then "look ahead" to the next buffer, and chain that buffer if necessary, and so on.

The operational parameters for the buffer management are defined by the user in the initialization block. The parameters defined include the basic mode of operation, the number of entries for the transmitter and receiver descriptor rings, frame Address field, and etc.

PROTOCOL

The MK5025 contains a full implementation of the 1984 CCITT X.25 data link layer. It allows both basic and extended control fields, variable window sizes, and user-defined counter and timer values. Extended addressing and UI frames are optionally available for use in ISDN LAPD applications. XID and TEST frames are available for use in X.32. The interface between the MK5025 and the host (layer 3) conforms to both the ISO data link services standard and the ISDN LAPD data link services standard.

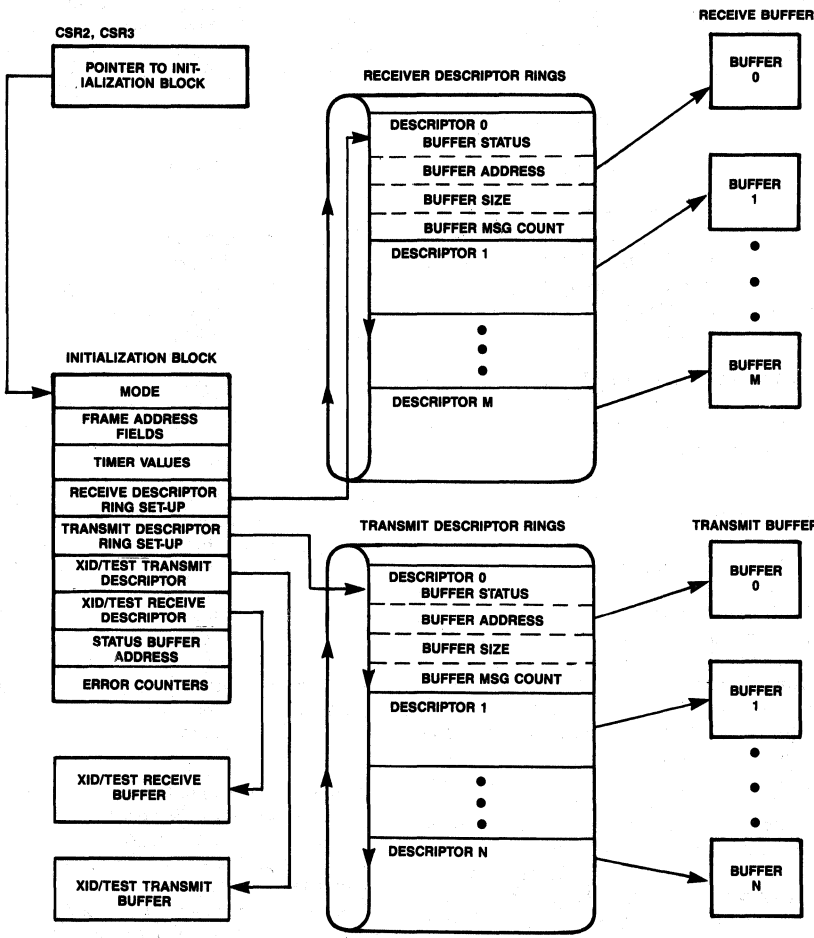


Figure 4. MK5025 Buffer Management

THE COMMAND/RESPONSE REPERTOIRE

The command/response repertoire of the MK5025 is shown in Tables 1a and 1b. This set conforms to ISDN LAPD and X.32, which are super-sets of X.25 Link Level. The MK5025 will process the S and U frames shown in Table I, and will handle the A and C fields for all I and UI frames.

The definitions for the symbols for the frame types are:

Name	Definition
I	Information frame
UI	Unnumbered Information
RR	Receiver Ready
DISC	Disconnect
RNR	Receiver Not Ready
UA	Unnumbered Acknowledge
REJ	Reject
FRMR	Frame Reject
SABM	Set Asynchronous Balance Mode
DM	Disconnect Mode
XID	Exchange Identification
TEST	Link Test frame

Table 1a. MK5025 Command/Response Repertoire.
Modulo 8 Operation

Format	Command	Resp	Encoding							
			1	2	3	4	5	6	7	8
Information Transfer	I		0	—	N(S)	—	P	—	N(R)	—
Supervisory	RR	RR	1	0	0	0	P/F	—	N(R)	—
	RNR	RNR	1	0	1	0	P/F	—	N(R)	—
	REJ	REJ	1	0	0	1	P/F	—	N(R)	—
Unnumbered	SABM		1	1	1	1	P	1	0	0
		DM	1	1	1	1	F	0	0	0
	*XID	*XID	1	1	1	1	P/F	1	0	1
	*UI	*UI	1	1	0	0	P/F	0	0	0
	DISC		1	1	0	0	P	0	1	0
		UA	1	1	0	0	F	1	1	0
		FRMR	1	1	1	0	F	0	0	1
	*TEST	*TEST	1	1	0	0	P/F	1	1	1

Table 1b. MK5025 Command/Response Repertoire.
Modulo 128 Operation.

Format	Command	Resp	Encoding									
			1	2	3	4	5	6	7	8	9	10-16
Information Transfer	I		0	———	———	———	N(S)	———	———	———	P	N(R)
Supervisory	RR	RR	1	0	0	0	0	0	0	0	P/F	N(R)
	RNR	RNR	1	0	1	0	0	0	0	0	P/F	N(R)
	REJ	REJ	1	0	0	1	0	0	0	0	P/F	N(R)
Unnumbered	SABME		1	1	1	1	P	1	1	0		
		DM	1	1	1	1	F	0	0	0		
	*XID	*XID	1	1	1	1	P/F	1	0	1		
	*UI	*UI	1	1	0	0	P/F	0	0	0		
	DISC		1	1	0	0	P	0	1	0		
		UA	1	1	0	0	F	1	1	0		
		FRMR	1	1	1	0	F	0	0	1		
	*TEST	*TEST	1	1	0	0	P/F	1	1	1		

* XID and UI Frames can be individually enabled for compatibility with X.32 and LAPD respectively. TEST frames are enabled with XID frames.

MK5025 ELECTRICAL SPECIFICATION

ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias . . . . . −25°C to +100°C
Storage Temperature . . . . . −65°C to +150°C
Voltage on Any Pin with Respect to Ground . . . . . −0.5 V to V_{CC} +0.5 V
Power Dissipation . . . . . 0.50 W

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

T_A=0°C to 70°C, V_{CC} = +5 V ±5 percent unless otherwise specified.

SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{IL}		−0.5		+0.8	V
V_{IH}		+2.0		V_{CC} +0.5	V
V_{OL}	@ I_{OL} = 3.2 mA			+0.5	V
V_{OH}	@ I_{OH} = −0.4 mA	+2.4			V
I_{IL}	@ V_{in} = 0.4 to V_{CC}			±10	μA
I_{CC}	T_{SCT} = 100 ns		50		mA

CAPACITANCE

Frequency = 1 MHz

SYMBOL	CONDITIONS	MIN	MAX	UNITS
C_{IN}			10	pF
C_{OUT}			10	pF
C_{IO}			20	pF

AC TIMING SPECIFICATIONS

T_A = 0°C to 70°C, V_{CC} = +5 V ±5 percent, unless otherwise specified.

NO.	SIGNAL	SYMBOL	PARAMETER	TEST CONDITIONS	MIN ns	TYP ns	MAX ns
1	SYSCLK	T_{SCT}	SYSCLK period		100		
2	SYSCLK	T_{SCL}	SYSCLK low time		45		
3	SYSCLK	T_{SCH}	SYSCLK high time		45		
4	SYSCLK	T_{SCR}	Rise time of SYSCLK		0		8
5	SYSCLK	T_{SCF}	Fall time of SYSCLK		0		8
6	$\overline{TCLK}$	T_{TCT}	$\overline{TCLK}$ period		140		
7	$\overline{TCLK}$	T_{TCL}	$\overline{TCLK}$ low time		63		
8	$\overline{TCLK}$	T_{TCH}	$\overline{TCLK}$ high time		63		
9	$\overline{TCLK}$	T_{TCR}	Rise time of $\overline{TCLK}$		0		8
10	$\overline{TCLK}$	T_{TCF}	Fall time of $\overline{TCLK}$		0		8
11	TD	T_{TDP}	TD data propagation delay after the falling edge of $\overline{TCLK}$	C_L = 50 pF			40
12	TD	T_{TDH}	TD data hold time after the falling edge of $\overline{TCLK}$	C_L = 50 pF	5		

AC TIMING SPECIFICATIONS

T_A = 0°C to 70°C, V_{CC} = +5 V ±5 percent, unless otherwise specified.

NO.	SIGNAL	SYMBOL	PARAMETER	TEST CONDITIONS	MIN ns	TYP ns	MAX ns
13	$\overline{RCLK}$	T_{RCT}	$\overline{RCLK}$ period		140		
14	$\overline{RCLK}$	T_{RCH}	$\overline{RCLK}$ high time		63		
15	$\overline{RCLK}$	T_{RCL}	$\overline{RCLK}$ low time		63		
16	$\overline{RCLK}$	T_{RCR}	Rise time of $\overline{RCLK}$		0		8
17	$\overline{RCLK}$	T_{RCF}	Fall time of $\overline{RCLK}$		0		8
18	RD	T_{RDR}	RD data rise time		0		8
19	RD	T_{RDF}	RD data fall time		0		8
20	RD	T_{RDH}	RD hold time after rising edge of $\overline{RCLK}$		5		
21	RD	T_{RDS}	RD setup time prior to rising edge of $\overline{RCLK}$		30		
22	A/DAL	T_{DOFF}	Bus Master driver disable after rising edge of $\overline{HOLD}$		0		50
23	A/DAL	T_{DON}	Bus Master driver enable after falling edge of $\overline{HLDA}$	T_{SCT} = 100 nS	0		200
24	$\overline{HLDA}$	T_{HHA}	Delay to falling edge of $\overline{HLDA}$ from falling edge of $\overline{HOLD}$ (Bus Master)		0		
25	$\overline{RESET}$	T_{RW}	$\overline{RESET}$ pulse width		30		
26	A/DAL	T_{CYCLE}	Read/write, address/data cycle time	T_{SCT} = 100 nS	600		
27	A	T_{XAS}	Address setup time to falling edge of ALE		100		
28	A	T_{XAH}	Address hold time after the rising edge of $\overline{DAS}$		50		
29	DAL	T_{AS}	Address setup time to the falling edge of ALE		75		
30	DAL	T_{AH}	Address hold time after the falling edge of ALE		20		
31	DAL	T_{RDAS}	Data setup time to the rising edge of $\overline{DAS}$ (Bus master read)		55		
32	DAL	T_{RDAH}	Data hold time after the rising edge of $\overline{DAS}$ (Bus master read)		0		
33	DAL	T_{DDAS}	Data setup time to the falling edge of $\overline{DAS}$ (Bus master write)		0		
34	DAL	T_{WDS}	Data setup time to the rising edge of $\overline{DAS}$ (Bus master write)		250		
35	DAL	T_{WDH}	Data hold time after the rising edge of $\overline{DAS}$ (Bus master write)		35		
36	DAL	T_{SRDH}	Data hold time after the rising edge of $\overline{DAS}$ (Bus slave read)	T_{SCT} = 100 nS	0		35
37	DAL	T_{SWDH}	Data hold time after the rising edge of $\overline{DAS}$ (Bus slave write)		0		
38	DAL	T_{SWDS}	Data setup time to the falling edge of $\overline{DAS}$ (Bus slave write)		0		
39	ALE	T_{ALEW}	ALE width high		110		

AC TIMING SPECIFICATIONS

T_A = 0°C to 70°C, V_{CC} = +5 V ±5 percent, unless otherwise specified.

NO.	SIGNAL	SYMBOL	PARAMETER	TEST CONDITIONS	MIN ns	TYP ns	MAX ns
40	ALE	T_{DALE}	Delay from rising edge of $\overline{DAS}$ to the rising edge of ALE		70		
41	$\overline{DAS}$	T_{DSW}	$\overline{DAS}$ width low		200		
42	$\overline{DAS}$	T_{ADAS}	Delay from the falling edge of ALE to the falling edge of $\overline{DAS}$		80		
43	$\overline{DAS}$	T_{RIDF}	Delay from the rising edge of $\overline{DALO}$ to the falling edge of $\overline{DAS}$ (Bus master read)		35		
44	$\overline{DAS}$	T_{RDYS}	Delay from the falling edge of $\overline{READY}$ to the rising edge of $\overline{DAS}$	T_{ARYD}=300 nS T_{SCT} = 100 nS	120		200
45	$\overline{DALI}$	T_{ROIF}	Delay from the rising edge of $\overline{DALO}$ to the falling edge of $\overline{DALI}$ (Bus master read)		70		
46	$\overline{DALI}$	T_{RIS}	$\overline{DALI}$ setup time to the rising edge of $\overline{DAS}$ (Bus master read)		150		
47	$\overline{DALI}$	T_{RIH}	$\overline{DALI}$ hold time after the rising edge of $\overline{DAS}$ (Bus master read)		0		
48	$\overline{DALI}$	T_{RIOF}	Delay from the rising edge of $\overline{DALI}$ to the falling edge of $\overline{DALO}$ (Bus master read)		70		
49	$\overline{DALO}$	T_{OS}	$\overline{DALO}$ setup time to the falling edge of ALE (Bus master read)		110		
50	$\overline{DALO}$	T_{ROH}	$\overline{DALO}$ hold time after the falling edge of ALE (Bus master read)		35		
51	$\overline{DALO}$	T_{WDSI}	Delay from the rising edge of $\overline{DAS}$ to the rising edge of $\overline{DALO}$ (Bus master write)		50		
52	$\overline{CS}$	T_{CSH}	$\overline{CS}$ hold time after the rising edge of $\overline{DAS}$ (Bus slave)		0		
53	$\overline{CS}$	T_{CSS}	$\overline{CS}$ setup time to the falling edge of $\overline{DAS}$ (Bus slave)		0		
54	ADR	T_{SAH}	ADR hold time after the rising edge of $\overline{DAS}$ (Bus slave)		0		
55	ADR	T_{SAS}	ADR setup time to the falling edge of $\overline{DAS}$ (Bus slave)		0		
56	$\overline{READY}$	T_{ARYD}	Delay from the falling edge of ALE to the falling edge of $\overline{READY}$ to insure a minimum bus cycle time (600 nS)	T_{SCT} = 100 nS			150
57	$\overline{READY}$	T_{SRDS}	Data setup time to the falling edge of $\overline{READY}$ (Bus slave read)		75		
58	$\overline{READY}$	T_{RDYH}	$\overline{READY}$ hold time after the rising edge of $\overline{DAS}$ (Bus master)		0		
59	$\overline{READY}$	T_{SRYH}	$\overline{READY}$ hold time after the rising edge of $\overline{DAS}$ (Bus slave)	T_{SCT} = 100 nS	0		35
60	READ	T_{SRH}	READ hold time after the rising edge of $\overline{DAS}$ (Bus slave)		0		
61	READ	T_{SRS}	READ setup time to the falling edge of $\overline{DAS}$ (Bus slave)		0		
62	$\overline{READY}$	T_{RDYD}	Delay from falling edge of $\overline{DAS}$ to falling edge of $\overline{READY}$ (Bus slave read)	T_{SCT} = 100 nS		200	

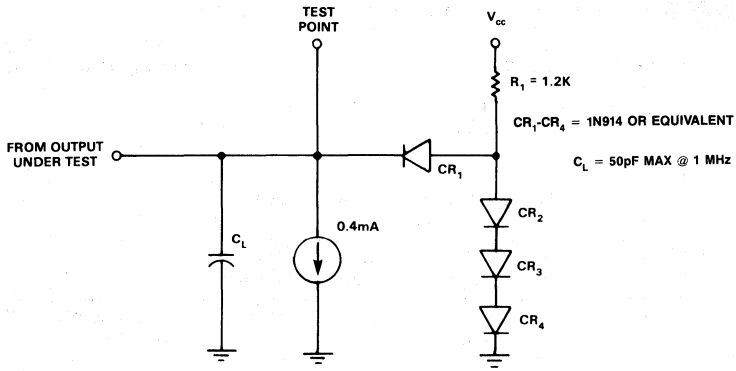
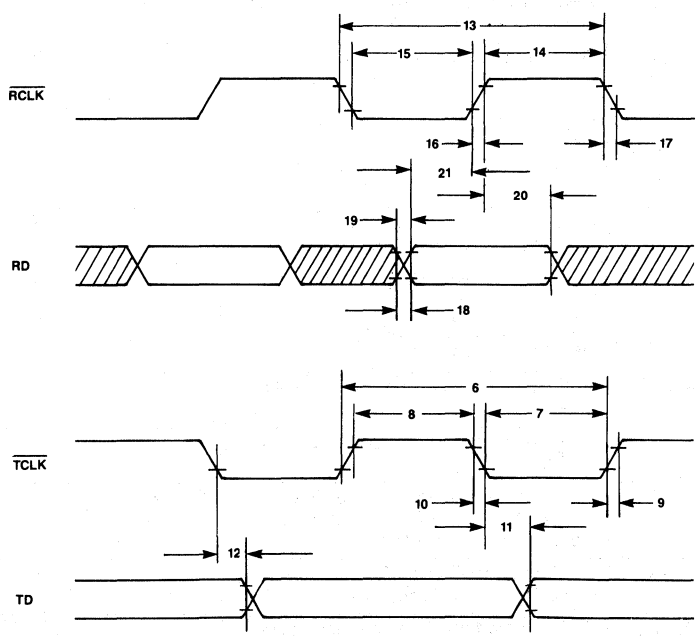


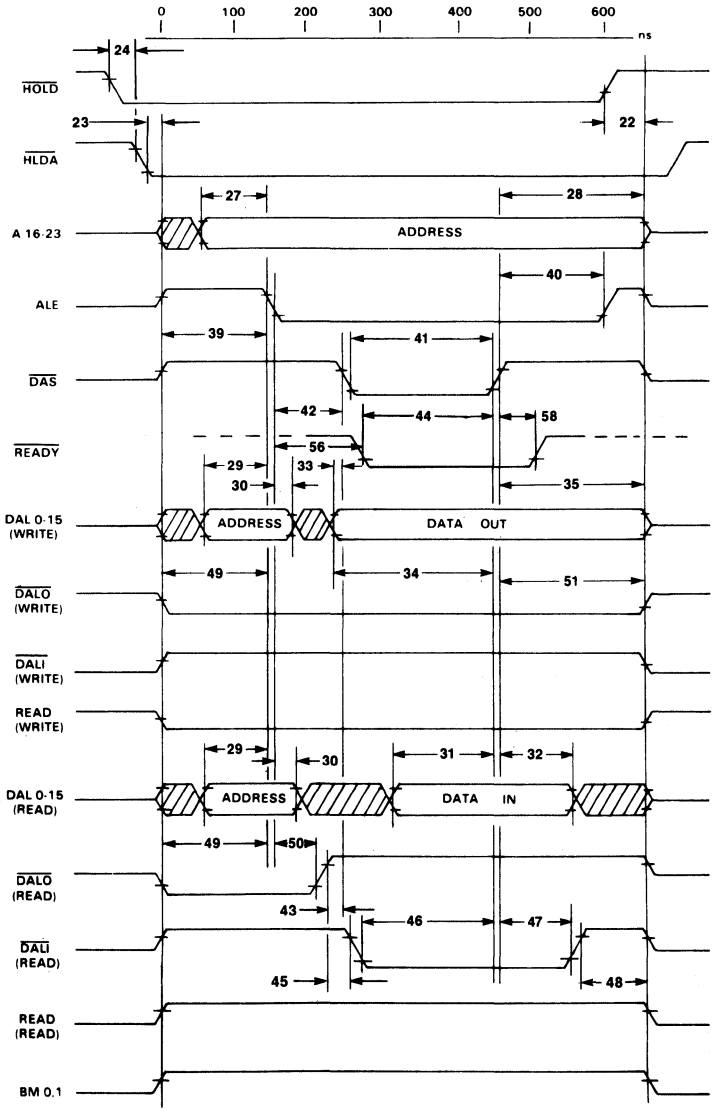
Figure 5. Output Load Diagram



TIMING MEASUREMENTS ARE MADE AT THE FOLLOWING VOLTAGES, UNLESS OTHERWISE SPECIFIED:

	"1"	"0"
OUTPUT	2.0 V	0.8 V
INPUT	2.0 V	0.8 V
FLOAT	90% V_{OH}	10% V_{OL}

Figure 6. MK5025 Serial Link Timing Diagram



NOTE: The Bus Master cycle time will increase from a minimum of 600 ns in 100 ns steps until the slave device returns READY.

Figure 7. MK5025 Bus Master Timing Diagram

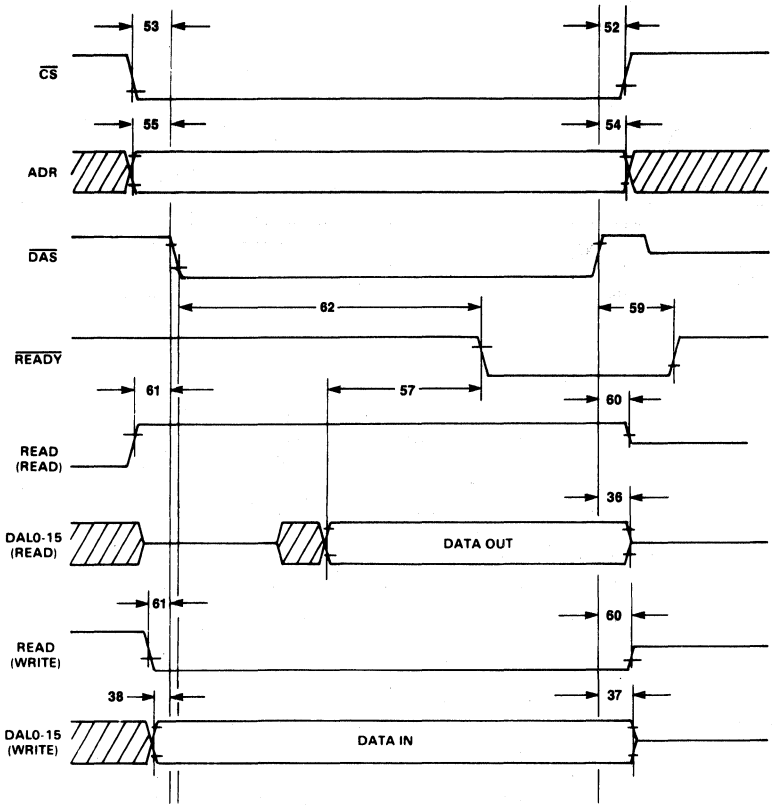


Figure 8. MK5025 Bus Slave Timing Diagram

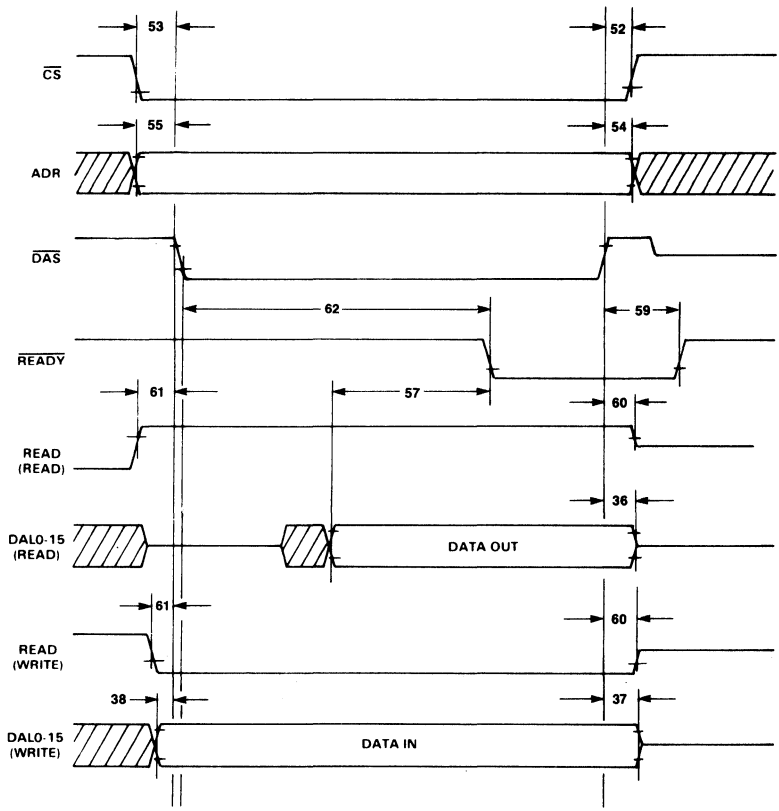
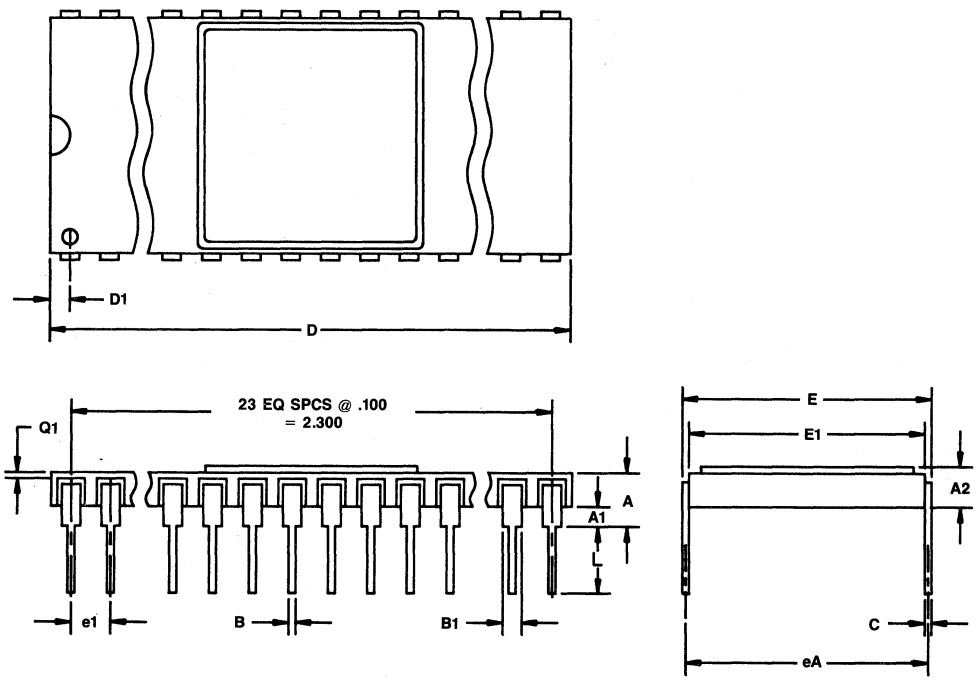


Figure 8. MK5025 Bus Slave Timing Diagram

PACKAGE DESCRIPTION



DIM.	INCHES		NOTES
	MIN.	MAX.	
A	—	.175	1
A1	.020	—	1
A2	.080	.110	
B	.015	.021	2
B1	.038	.057	
C	.008	.012	2
D	2.370	2.430	
D1	.035	.065	
E	.595	.625	
E1	.580	.610	
e1	.090	.110	
eA	.590	.665	
L	.125	—	
Q	.005	—	3

NOTES

1. Package standoff to be measured per JEDEC requirements.
2. The maximum limit shall be increased by .003 in. when solder lead finish is specified.
3. Measured from top of ceramic to nearest metallization.

TECHNICAL MANUAL

MOSTEK X.25 LINK LEVEL CONTROLLER (MK5025)

TABLE OF CONTENTS

SECTION 1
INTRODUCTION

The Mostek X.25 Link Level Controller (MK5025) is a VLSI semiconductor device which provides a complete link level data communication control conforming to the 1984 CCITT version of X.25. This includes frame formatting, transparency (so-called "bit-stuffing"), error recovery by retransmission, sequence number control, U (unnumbered) frame control, and S (supervisory) frame control. The 1984 specification includes several enhancements to the 1980 version of X.25. It includes extended control fields and a 16 or 32 bit FCS. The MK5025 also supports X.32 (XID) and X.75.

The chip also supports single channel LAPD for ISDN with its UI frames and extended addressing capabilities. However, LAPD is still being defined as of the writing of this specification and is subject to change. No guarantees are made regarding future compatibility.

A transparent mode provides an HDLC transport mechanism without link layer support. Extended addressing and control are optionally supported within transparent mode. Address filtering is also optional in transport mode.

One of the outstanding features of the MK5025 is its buffer management which includes on-chip DMA. This feature allows users to handle multiple frames of receive and transmit data at a time. (A conventional data link control chip plus a separate DMA chip would handle data for only a single block at a time.)

The MK5025 may be used with several popular microprocessors, such as 68020, 68000, 6800, Z8000, Z80, LSI-11, 8086, 8088, 8080, etc.

SECTION 2
FEATURES

- CMOS
- Fully compatible with both 8 or 16 bit systems.
- System clock rate to 10 MHz.
- Data rate up to 7 MBPS, with a 64-byte FIFO in each direction.
- Complete Level 2 Implementation.
- Compatible with X.25 LAPB, ISDN LAPD, X.32, and X.75 Link Level Protocols.
- 48-pin DIP pin-for-pin compatible with the Mostek SS7 Controller (MK5027) and nearly pin-for-pin compatible with the Mostek LANCE chip (MK68590).
- Buffer Management includes:
  - Initialization Block
  - Separate Receive and Transmit Rings
  - Variable Descriptor Ring and Window Size.
- On chip DMA control with programmable burst length.
- Selectable single or extended control field.
- Programmable 1 or 2 byte address field and Global Address.
- Transparent mode with or without addressing filtering for customized protocols using HDLC framing and DMA buffering.
- Handles all HDLC (ADCCP) frame formatting:
  - Zero bit insert and delete
  - FCS generation and detection
  - Frame delimiters by flags
- Five programmable timer counters:
  - T1, T3, TP, N1, N2.
- Handles all error recovery, sequencing, and S and U frame control
- Selectable FCS of 16 or 32 bits.
- Data Link Services:
  - Compatible with ISO Data Link Services
  - Compatible with LAPD Data Link Services.
- Testing Facilities:
  - Internal Loopback
  - Silent Loopback
  - Optional Internal Data Clock Generation
  - Self Test.
- All inputs and outputs are TTL compatible.
- Programmable for full or half duplex operation.
- Programmable minimum frame spacing (number of flags between frames).

SECTION 3
OPERATIONAL DESCRIPTION

The Thomson Components - Mostek X.25 Link Controller (MK5025) is a VLSI semiconductor device intended for data communication applications requiring X.25 link level control. The MK5025 will perform all frame formatting, such as: frame delimiting with flags, FCS generation and detection. The MK5025 also includes a buffer management mechanism that allows the user to transmit and/or receive multiple frames. Contained in the buffer management is an on-chip dual channel DMA: one channel for receive and one channel for transmit. The MK5025 handles all supervisory (S) and unnumbered (U) frames. (See Table I.)

The MK5025 is intended to be used with any popular 16 or 8 bit microprocessor. A possible system configuration for the MK5025 is shown in figure 1. This document assumes that the processor has a byte addressable address bus.

The MK5025 will move multiple blocks of receive and transmit data directly into and out of memory through the Host's bus. An I/O acceleration processor, such as the MK68HC200 Single Chip Micro-Computer, could be used to off-load Network Level software from the Host. The I/O acceleration processor in figure 1 is recommended, but not required.

The MK5025 may be operated in either full or half duplex mode. In half duplex mode, the RTS and CTS modem control pins are provided. In full duplex mode, these pins become user programmable I/O pins.

All signal pins on the MK5025 are TTL compatible. This has the advantage of making the MK5025 independent of the physical interface. As shown in Fig. 1, line drivers and receivers are used for electrical connection to the physical layer.

3.1 Functional Blocks

The MK5025 is made up of 8 functional blocks. These are shown in Figure 2.

3.1.1 Microcontroller

The microcontroller is the brain of the MK5025. It controls all of the other blocks and contains most of the protocol processing. All frame content processing as well as S and U frame processing and generation is performed by the microcontroller. All primitive processing and generation is also done here. The microcode ROM contains the control program for the microcontroller.

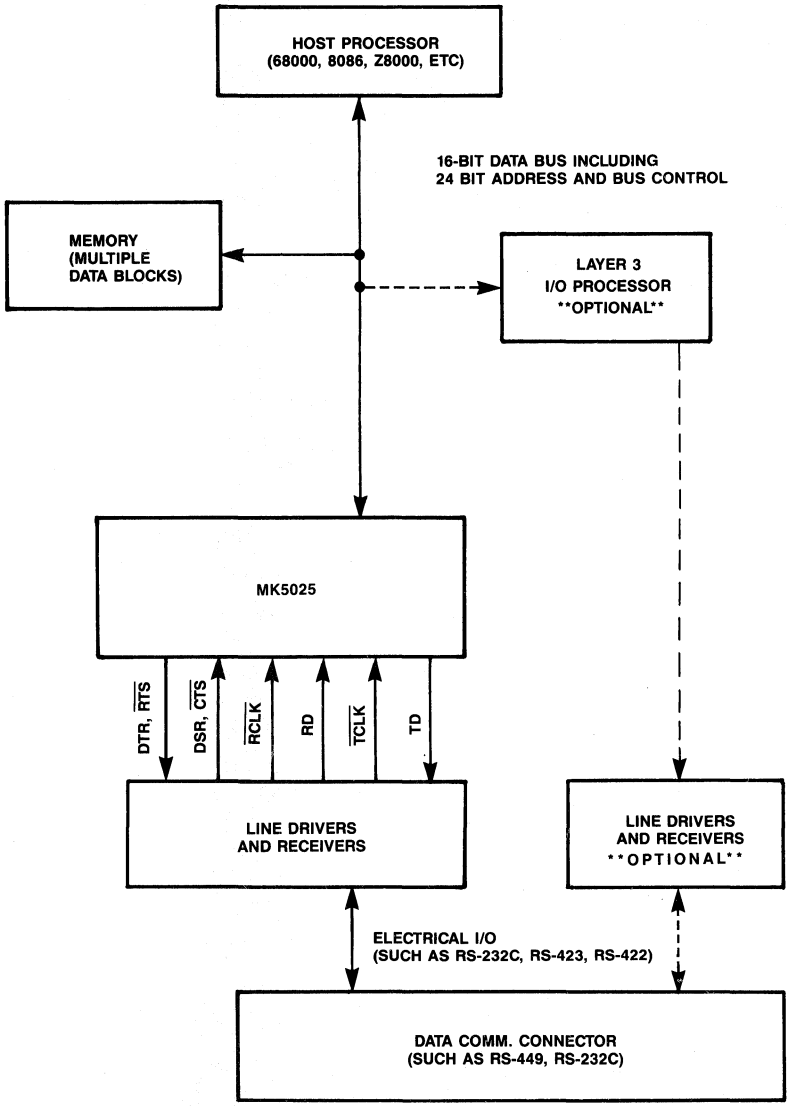


Figure 1. Possible System Configuration for the MK5025

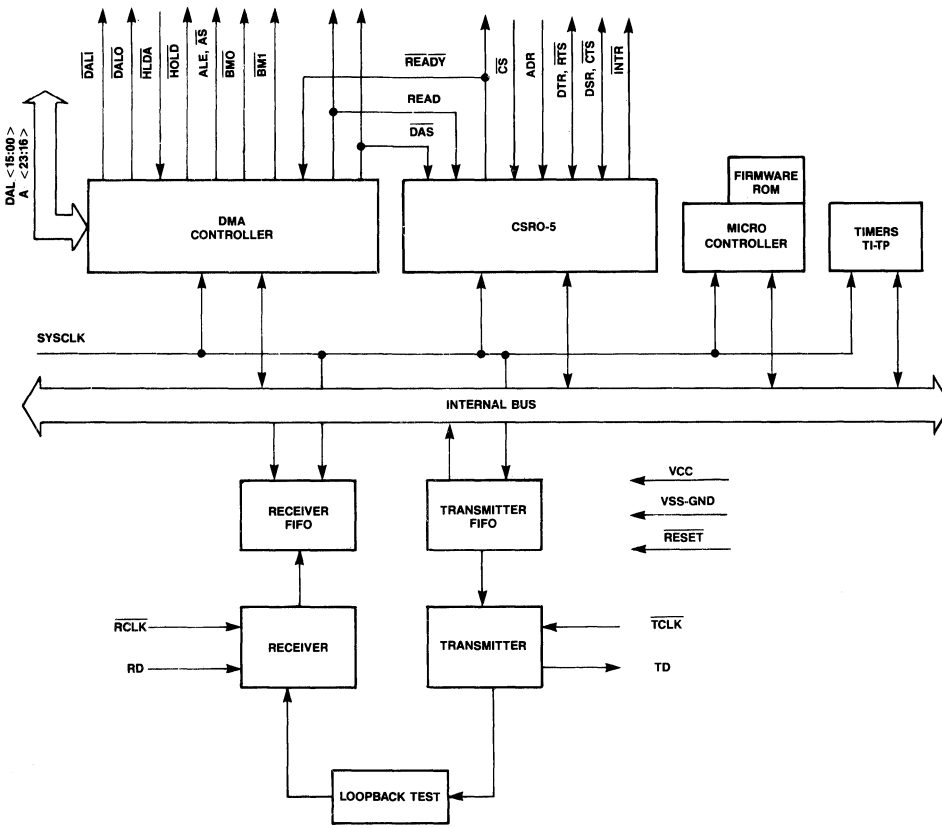


Figure 2. MK5025 Simplified Block Diagram

3.1.2 Receiver

Serial receive data comes into the Receiver (Figure 2). The Receiver is responsible for:

1. Leading and trailing flag detection.
2. Deletion of zeroes inserted for transparency.
3. Detection of idle and abort sequences.
4. Detection of good and bad FCS (Frame Check Sequence).
5. Monitoring Receiver FIFO status.
6. Detection of Receiver-Over-Run.
7. Odd byte detection.

   NOTE: If frames are received that have an odd number of bytes in the information field, the last byte of the frame is said to be an odd byte.

8. Detection of non-octet aligned frames, such frames are treated as invalid frames (see reference #5, section 2.3.5.3).

3.1.3 Transmitter

The Transmitter is responsible for:

1. Serialization of outgoing data.
2. Generating and appending the FCS.
3. Generation of interframe time-fill as either flags or idle.
4. Zero bit insertion for transparency.
5. Transmitter-Under-Run detection.
6. Transmission of odd byte.
7. RTS/CTS Control

3.1.4 Frame Check Sequence

The FCS on the transmitter or receiver may be either 16 bit or 32 bit, and is user selectable. For full duplex operation, both the receiver and transmitter have individual FCS computation circuits. The characteristics of the FCS are:

Transmitted Polarity: Inverted

Transmitted Order: High Order Bit First

Pre-set Value: All 1's

Polynominal 16 bit:
$X^{16} + X^{12} + X^5 + 1$

Remainder 16 bit (if received correctly):
high order bit-->0001 1101 0000 1111

Polynominal 32 bit:
$X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^{8} + X^{7} + X^{5} + X^{4} + X^{2} + X + 1$

Remainder 32 bit (if received correctly):
high order bit-->1100 0111 0000 0100
1101 1101 0111 1011

3.1.5 Receive FIFO

The Receive FIFO buffers the data received by the receiver. This performs two major functions. First, it resynchronizes the data from the receive clock to the system clock. Second, it allows the microcontroller time to finish whatever it may be doing before it has to process the received data.

The receive FIFO holds the data from the receiver without interrupting the microconroller until it contains enough data to reach the watermark level. This watermark level can be programmed in CSR4 to occur when the FIFO contains at least 2 bytes; 18 or more bytes; 34 or more bytes; or 50 or more bytes. This programmability, along with the programmable burst length of the DMA controller, enables the user to define how often and for how long the MK5025 must use the host bus. For more information, see Control/Status Register 4.

For example, if the watermark level is set at 34 bytes and the burst length is limited to 8 word transfers at a time, the MK5025 will request control of the host bus as soon as 34 bytes are received and again after every 16 subsequent bytes.

3.1.6 Transmit FIFO

The Transmit FIFO buffers the data to be transmitted by the MK5025. This also performs two major functions. First, it resynchronizes the data from the system clock to the transmit clock. Second, it allows the microcontroller and DMA controller to read data from the host's memory buffers in bursts; making both the MK5025 and the host bus more efficient.

The transmit FIFO has a watermark scheme similar to the one described for the receive FIFO above. The transmit FIFO will not interrupt the microcontroller for service until it empties enough to reach the watermark level. The watermark can be programmed in CSR4 as: any space available, 18 bytes of space available, 34 bytes of space available, or 50 bytes of space available.

3.1.7 DMA Controller

The MK5025 has an on-chip DMA Controller circuit. This allows it to access memory without requiring host software intervention. Whenever the MK5025 requires access to the host memory it will negotiate for mastership of the bus. Upon gaining control of the bus the MK5025 will begin transferring data to or from memory. The MK5025 will perform memory transfers until either it has nothing more to transfer, it has reached its DMA burst limit (user programmable), or the $\overline{\text{BUSREL}}$ pin is driven low. In any case it will complete all bus transfers before releasing bus mastership back to the host. If, during a memory transfer, the memory does not respond within 256 SCLK cycles, the MK5025 will release ownership of the bus immediately and the MERR bit will be set in CSR0. The DMA burst limit can be programmed by the user through CSR4. In 16 bit mode the limit can be set to 1 word, 8 words, or unlimited word transfers. In 8 bit mode, it can be set to 2 bytes, 16 bytes, or unlimited byte transfers. For high speed data lines (i.e. > 1 Mbps) a burst limit of 8 words, 16 bytes or unlimited is suggested to allow maximum throughput.

The byte ordering of the DMA transfers can be programmed to account for differences in processor architectures or host programming languages. Byte ordering can be programmed seperately for data and control information. Data information is defined as all contents of data buffers; control information is defined as anything else in the shared memory space (i.e. initialization block, descriptors, etc). For more information see section 4.1.2.5 on control status register 4.

3.1.8 Bus Slave Circuitry

The MK5025 contains a bank of internal control/status registers (CSR0-5) which can be accessed by the host as a peripheral. The host can read or write to these registers like any other bus slave. The contents of these registers and the bus signal timing is listed below.

3.2 Buffer Management Overview

Refer to Fig. 3.

3.2.1 The Initialization Block

Chip initialization information is located in a block of memory called the Initialization Block. The Initialization Block consists of 44 contiguous words of memory starting on a word boundary. This memory is assembled by the HOST or I/O acceleration processor, and is accessed by MK5025 during initialization. The Initialization Block is comprised of:

A. Mode of Operation.

B. Frame Address Values.

C. Timer Preset Values.

D. Location and size of Receive and Transmit Descriptor Rings.

E. Location and size of XID/TEST Buffers.

F. Location of status buffer.

G. Error Counters.

3.2.2 The Circular Queue

The basic organization of the buffer management is a circular queue of tasks in memory called descriptor rings. There are separate rings to describe the transmit and receive operations. Up to 128 buffers may be queued-up on a descriptor ring awaiting execution by the MK5025. The descriptor ring has a segment assigned to each buffer. Each segment holds a pointer for the starting address of the buffer, and holds a value for the length of the buffer in bytes.

Each segment also contains two control bits called OWNA and OWNB, which denote whether the MK5025, the HOST, or the I/O ACCELERATION PROCESSOR (if present) "owns" the buffer. For transmit, when the MK5025 owns the buffer, the MK5025 is allowed and commanded to transmit the buffer. When the MK5025 does not own the buffer, it will not transmit that buffer. For receive, when the MK5025 owns a buffer, it may place received data into that buffer. Conversely, when the MK5025 does not own a receive buffer, it will not place received data in that buffer.

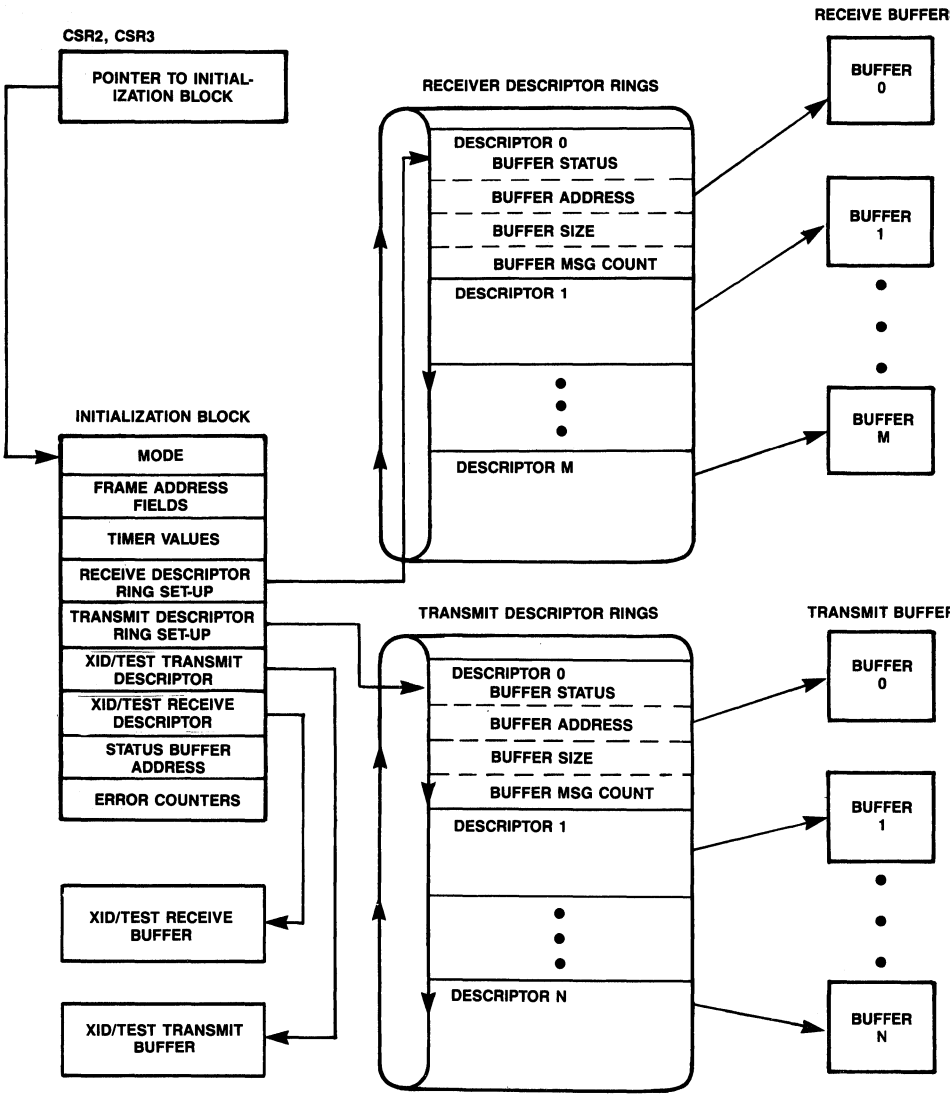


Figure 3. MK5025 Buffer Management

The MK5025 buffer management mechanism will handle frames which are longer than the length of an individual buffer. This is done by a chaining method which utilizes multiple buffers. The MK5025 tests the next segment in the descriptor ring in a "look ahead" manner. If the frames are too long for one buffer, the next buffer will be used after filling (or transmitting) the first buffer; that is, "chained". The MK5025 will then "look ahead" to the next buffer, and chain that buffer if necessary, and so on.

The operational parameters for the buffer management are defined by the user in the initialization block. The parameters defined include the basic mode of operation, the number of entries for the transmitter and receiver descriptor rings, frame Address field, and etc. The starting address for the Initialization, IADR, is defined in the CSR2 and CSR3 registers inside the MK5025.

3.2.3 Frame Format

The frame format used by the MK5025 is shown below. Each frame consists of a programmable number of leading flag patterns (01111110), an address field, a control field, an information field (not in all frames), an FCS of either 16 or 32 bits, and a trailing flag pattern. The number of leading flags is programmable through the Mode Register in the Initialization Block. Received frames may have only one flag between adjacent frames.

F	•••	F	A	C	I	FCS	F
8 bits		8	8/16	8/16	8*n	16/32	8

Transmitted First

3.2.4 The Command/Response Repertoire

The command/response repertoire of the MK5025 is shown in Tables Ia and Ib. This set conforms to the ISDN LAPD, which is a super-set of X.25 Link Level. The MK5025 will process the S and U frames shown in Table I, and will handle the A and C fields for all I and UI frames.

The definitions for the symbols for the frame types are:

Name	Definition
I	Information frame
UI	Unnumbered Information
RR	Receiver Ready
DISC	Disconnect
RNR	Receiver Not Ready
UA	Unnumbered Acknowledge
REJ	Reject
FRMR	Frame Reject
SABM	Set Asynchronous Balance Mode
DM	Disconnect Mode
XID	Exchange Identification
TEST	Link Test frame

Table Ia. MK5025 Command/Response Repertoire.
Modulo 8 Operation

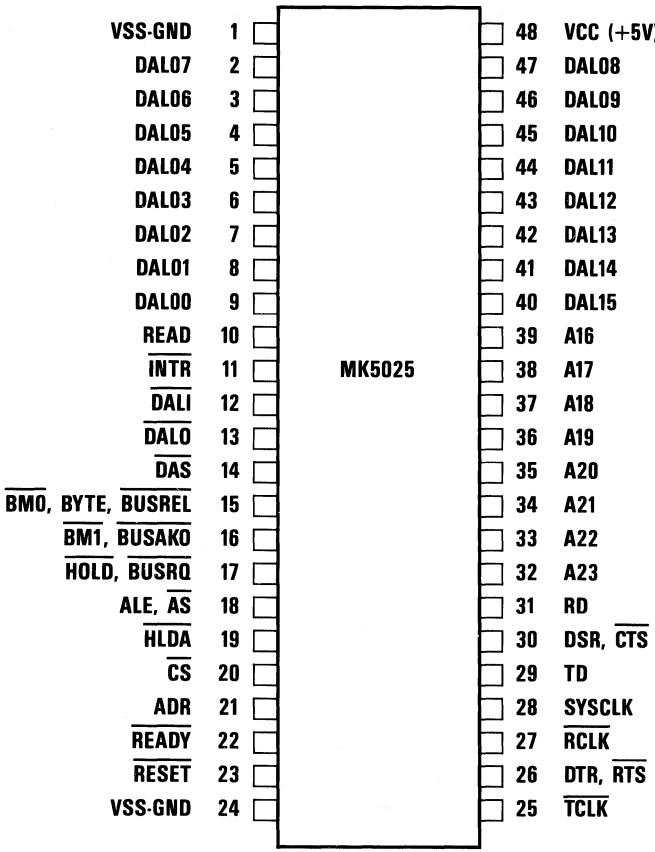
Format	Command	Resp	Encoding							
			1	2	3	4	5	6	7	8
Information Transfer	I		0	←	N(S)	→	P	←	N(R)	→
Supervisory	RR	RR	1	0	0	0	P/F	←	N(R)	→
	RNR	RNR	1	0	1	0	P/F	←	N(R)	→
	REJ	REJ	1	0	0	1	P/F	←	N(R)	→
Unnumbered	SABM		1	1	1	1	P	1	0	0
		DM	1	1	1	1	F	0	0	0
	*XID	*XID	1	1	1	1	P/F	1	0	1
	*UI	*UI	1	1	0	0	P/F	0	0	0
	DISC		1	1	0	0	P	0	1	0
		UA	1	1	0	0	F	1	1	0
		FRMR	1	1	1	0	F	0	0	1
	*TEST	*TEST	1	1	0	0	P/F	1	1	1

Table Ib. MK5025 Command/Response Repertoire.
Modulo 128 Operation.

Format	Command	Resp	Encoding									
			1	2	3	4	5	6	7	8	9	10-16
Information Transfer	I		0	———	———	———	N(S)	———	———	———	P	N(R)
Supervisory	RR	RR	1	0	0	0	0	0	0	0	P/F	N(R)
	RNR	RNR	1	0	1	0	0	0	0	0	P/F	N(R)
	REJ	REJ	1	0	0	1	0	0	0	0	P/F	N(R)
Unnumbered	SABME		1	1	1	1	P	1	1	0		
		DM	1	1	1	1	F	0	0	0		
	*XID	*XID	1	1	1	1	P/F	1	0	1		
	*UI	*UI	1	1	0	0	P/F	0	0	0		
	DISC		1	1	0	0	P	0	1	0		
		UA	1	1	0	0	F	1	1	0		
		FRMR	1	1	1	0	F	0	0	1		
	*TEST	*TEST	1	1	0	0	P/F	1	1	1		

* XID and UI Frames can be individually enabled for compatibility with X.32 and LAPD respectively. TEST frames are enabled with XID frames.

3.3 Pin Description



PIN DESCRIPTION

LEGEND:

I	Input only	3S	3-State
O	Output only	OD	Open Drain (no internal pull-up)
IO	Input/Output	SIGNAL	Active low signal, i.e., inverted

SIGNAL NAME	PIN(S)	TYPE	DESCRIPTION
DAL<7:00>	2-9	IO/3S	The time multiplexed Data/Address bus. During the address portion of the memory transfer, DAL<7:00> contains the lower 8 bits of the memory address. During the data portion of a memory transfer, DAL<7:00> contains the read or write data, depending on the type of transfer.
READ	10	IO/3S	READ indicates the type of operation that the bus controller is performing during a bus transaction. READ is driven by the MK5025 only while it is the BUS MASTER. READ is valid during the entire bus transaction and is tristated by the MK5025 at all other times. MK5025 as a Bus Slave READ = HIGH - Data is placed on the DAL lines by the chip. READ = LOW - Data is taken off the DAL lines by the chip. MK5025 as a Bus Master READ = HIGH - Data is taken off the DAL lines by the chip. READ = LOW - Data is placed on the DAL lines by the chip.
$\overline{INTR}$	11	O/OD	INTERRUPT is an attention interrupt line that indicates that one or more of the following CSR0 status flags is set: MISS, MERR, RINT, TINT or PINT. INTERRUPT is enabled by CSR0<09>, INEA=1.
$\overline{DALI}$	12	O/3S	DAL IN is an external bus transceiver control line. $\overline{DALI}$ is driven by the MK5025 only while it is the BUS MASTER. $\overline{DALI}$ is asserted by MK5025 when it reads from the DAL lines during the data portion of a READ transfer. $\overline{DALI}$ is not asserted during a WRITE transfer.
$\overline{DALO}$	13	O/3S	DAL OUT is an external bus transceiver control line. $\overline{DALO}$ is driven by the MK5025 only while it is the BUS MASTER. $\overline{DALO}$ is asserted by MK5025 when it drives the DAL lines during the address portion of a READ transfer or for the duration of a WRITE transfer.
$\overline{DAS}$	14	IO/3S	DATA STROBE defines the data portion of a bus transaction. By definition data is stable and valid at the low to high transition of $\overline{DAS}$. This signal is driven by the MK5025 while it is the BUS MASTER. During Bus Slave operations, this pin is used as an input. At all other times the signal is tristated.
$\overline{BM0}$ BYTE $\overline{BUSREL}$	15	IO/3S	I/O pins 15 and 16 are programmable through CSR4. If bit 06 of CRS4 is set to a one, pin 15 becomes input $\overline{BUSREL}$ and is used by the host to signal the MK5025 to terminate a DMA burst after the current bus transfer has completed. If bit 06 is clear then pin 15 is an output and behaves as described below for pin 16.
$\overline{BM1}$ $\overline{BUSAKO}$	16	O/3S	Pins 15 and 16 are programmable through bit 00 of CSR4 (BCON). If CSR4<00> BCON = 0, I/O PIN 15 = $\overline{BM0}$ (O/3S) I/O PIN 16 = $\overline{BM1}$ (O/3S)

SIGNAL NAME	PIN(S)	TYPE	DESCRIPTION

BYTE MASK<1:0> Indicates the byte(s) on the DAL to be read or written during this bus transition. MK5025 drives these lines only as a Bus Master. MK5025 ignores the BM lines when it is a Bus Slave.

Byte selection is done as outlined in the following table.

$\overline{BM1}$	$\overline{BM0}$	
LOW	LOW	ENTIRE WORD
LOW	HIGH	UPPER BYTE (DAL<15:08>)
HIGH	LOW	LOWER BYTE (DAL<07:00>)
HIGH	HIGH	NONE

If CSR4<00> BCON = 1,
I/O PIN 15 = BYTE (O/3S)
I/O PIN 16 = $\overline{BUSAKO}$ (O)

Byte selection is done using the BYTE line and DAL<00> latched during the address portion of the bus transaction. MK5025 drives BYTE only as a Bus Master and ignores it when a Bus Slave. Byte selection is done as outlined in the following table.

BYTE	DAL<00>	
LOW	LOW	ENTIRE WORD
LOW	HIGH	ILLEGAL CONDITION
HIGH	LOW	LOWER BYTE
HIGH	HIGH	UPPER BYTE

$\overline{BUSAKO}$ is a bus request daisy chain output. If MK5025 is not requesting the bus and it receives $\overline{HLDA}$, $\overline{BUSAKO}$ will be driven low. If MK5025 is requesting the bus when it receives $\overline{HLDA}$, $\overline{BUSAKO}$ will remain high.

$\overline{HOLD}$ / $\overline{BUSRQ}$ — 17 — IO/OD

Pin 17 is configured through bit 0 of CSR4.
If CSR4<00> BCON = 0
I/O PIN 17 = $\overline{HOLD}$

$\overline{HOLD}$ request is asserted by MK5025 when it requires a DMA cycle regardless of the previous state of the $\overline{HOLD}$ pin. $\overline{HOLD}$ is held low for the entire ensuring bus transaction.

If CSR4<00> BCON = 1
I/O PIN 17 = $\overline{BUSRQ}$

$\overline{BUSRQ}$ is asserted by the MK5025 when it requires a DMA cycle if the prior state of the $\overline{BUSRQ}$ pin was high. $\overline{BUSRQ}$ is held low for the entire ensuing bus transaction.

ALE / $\overline{AS}$ — 18 — O/3S

The active level of ADDRESS STROBE is programmable through CSR4. The address portion of a bus transfer occurs while this signal is at its asserted level. This signal is driven by the MK5025 while it is the BUS MASTER. At all other times, the signal is tristated.

If CSR4<01> ACON = 0
I/O PIN 18 = ALE

ADDRESS LATCH ENABLE is used to demultiplex the DAL lines and define the address portion of the transfer. As ALE, the signal transitions from high to low during the address portion of the transfer and remains low during the data portion.

SIGNAL NAME	PIN(S)	TYPE	DESCRIPTION
			If CSR4<01> ACON = 1, I/O PIN 18 = $\overline{AS}$ As $\overline{AS}$, the signal pulses low during the address portion of the bus transfer. The low to high transition of $\overline{AS}$ can be used by a slave device to strobe the address into a register.
$\overline{HLDA}$	19	I	HOLD ACKNOWLEDGE is the response to $\overline{HOLD}$. When HLDA is low in response to MK5025's assertion of $\overline{HOLD}$, the MK5025 is the Bus Master. $\overline{HLDA}$ should be disasserted ONLY after $\overline{HOLD}$ has been released by MK5025; otherwise the MK5025 will interpret the raising of $\overline{HLDA}$ as a memory error (see CSR0).
$\overline{CS}$	20	I	CHIP SELECT indicates, when low, that the MK5025 is the slave device for the data transfer. $\overline{CS}$ must be valid throughout the entire transaction.
ADR	21	I	ADDRESS selects the Register Address Port or the Register Data Port. It must be valid throughout the data portion of the transfer and is only used by the chip when $\overline{CS}$ is low. ADR — PORT LOW — REGISTER DATA PORT HIGH — REGISTER ADDRESS PORT
$\overline{READY}$	22	IO/OD	When the MK5025 is a Bus Master, $\overline{READY}$ is an asynchronous acknowledgement from the bus memory that memory will accept data in a WRITE cycle or that memory has put data on the DAL lines in a READ cycle. As a Bus Slave, the MK5025 asserts $\overline{READY}$ when it has put data on the DAL lines during a READ cycle or is about to take data from the DAL lines during a WRITE cycle. $\overline{READY}$ is a response to $\overline{DAS}$ and it will be negated after $\overline{DAS}$ is negated.
$\overline{RESET}$	23	I	$\overline{RESET}$ is the Bus signal that will cause MK5025 to cease operation, clear its internal logic and enter an idle state with the STOP bit of CSR0 set.
$\overline{TCLK}$	25	I	TRANSMIT CLOCK. A 1X clock input for transmitter timing. TD changes on the falling edge of $\overline{TCLK}$. The frequency of $\overline{TCLK}$ may be up to 7 Mbps.
DTR $\overline{RTS}$	26	IO	DATA TERMINAL READY, REQUEST TO SEND. Modem Control Pin. Pin 26 is configurable through CSR5. This pin can be programmed to behave as output $\overline{RTS}$ or as programmable IO pin DTR. If configured as $\overline{RTS}$, the MK5025 will assert this pin if it has data to send and throughout transmission of a frame.
$\overline{RCLK}$	27	I	RECEIVE CLOCK. A 1X clock input for receiver timing. RD is sampled on the rising edge of $\overline{RCLK}$. The frequency of $\overline{RCLK}$ may be up to 7 MHz.
SYSCLK	28	I	SYSTEM CLOCK. SYSTEM CLOCK. System clock used for internal timing of MK5025. SYSCLK should be a square wave, and be greater than 500 KHz and less than 10 MHz.
TD	29	O	TRANSMIT DATA. Transmit serial data output.
DSR $\overline{CTS}$	30	IO	DATA SET READY, CLEAR TO SEND. Modem Control Pin. Pin 30 is configurable through CSR5. This pin can be programmed to behave as input $\overline{CTS}$ or as programmable IO pin DSR. If configured as $\overline{CTS}$, the MK5025 will transmit all 1's while $\overline{CTS}$is high.

SIGNAL NAME	PIN(S)	TYPE	DESCRIPTION
RD	31	I	RECEIVE DATA. Received serial data input.
A<23:16>	32-39	O/3S	Address bits <23:16> used in conjunction with DAL<15:00> to produce a 24 bit address. MK5025 drives these lines only as a Bus Master.
DAL<15:08>	40-48	IO/3S	The time multiplexed Data/Address bus. For 16-bit operations, DAL <15:08> behaves similar to DAL<07:00> above for the high byte of data or the middle byte of the 24 bit address. For 8-bit operations, DAL<15:08> behaves similar to a <23:16> for the middle byte of the 24-bit address only.
VCC-GND	1,24		
VCC	48		Power Supply Pin. +5.0 VDC ±5%

SECTION 4
PROGRAMMING SPECIFICATION

This section defines the Control and Status Registers and the memory data structures required to program the MK5025.

4.1 Control and Status Registers

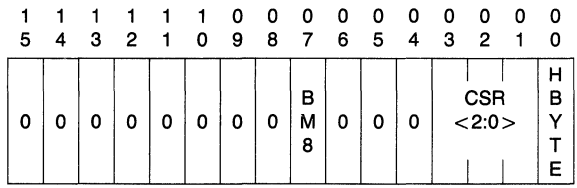
There are six Control and Status Registers (CSR's) resident within MK5025. The CSR's are accessed through two bus addressable ports, an address port (RAP), and a data port (RDP). Thus the MK5025 needs only two address locations in the system memory or IO map.

4.1.1 Accessing the Control and Status Registers

The CSR's are read (or written) in a two step operation. The address of the CSR is written into the address port (RAP) during a bus slave transaction. During a subsequent bus slave transaction, the data being read from (or written into) the data port (RDP) is read from (or written into) the CSR selected in the RAP. Once written, the address in RAP remains unchanged until rewritten. A control I/O pin (ADR) is provided to distinguish the address port from the data port.

ADR	Port
L	Register Data Port (RDP)
H	Register Address Port (RAP)

4.1.1.1 Register Address Port (RAP)

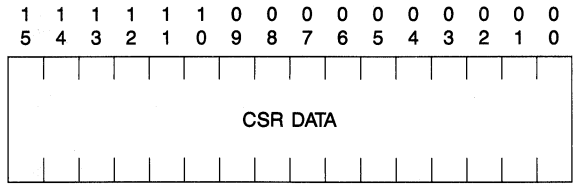


BIT	NAME	DESCRIPTION
15:08	RESERVED	Must be written as zeroes.
07	BM8	When set, places chip into 8 bit mode. CSR's, Init Block, and data transfers are all 8 bit transfers; this provides compatibility with 8 bit microprocessors. When clear, all transfers are 16 bit transfers. This bit must be set to the same value each time it is written, changing this bit during normal operation will achieve unexpected results. BM8 is READ/WRITE and cleared on Bus RESET.
06-04	RESERVED	Must be written as zeroes.
03:01	CSR<2:0>	CSR address select bits. READ/WRITE. Selects the CSR to be accessed through the RDP. RAP is cleared by Bus RESET.

CSR<2:0>	CSR Selected
0	CSR0
1	CSR1
2	CSR2
3	CSR3
4	CSR4
5	CSR5

00	HBYTE	Determines which byte is addressed for 8 bit operation. If set, the high byte of the register referred to by CSR<2:0> is addressed, otherwise the low byte is addressed. This bit is only meaningful for 8 bit operation and must be written as zero if BM8 = 0. HBYTE is READ/WRITE and cleared on Bus Reset.

4.1.1.2 Register Data Port (RDP)

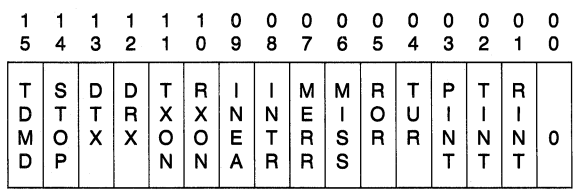


BIT	NAME	DESCRIPTION
15:00	CSR DATA	Writing data to the RDP loads data into the CSR selected by RAP. Reading the data from RDP reads the data from the CSR selected in RAP.

4.1.2 Control and Status Register Definition

4.1.2.1 Control and Status Register 0 (CSR0)

RAP<3:1> = 0



BIT	NAME	DESCRIPTION
15	TDMD	TRANSMIT DEMAND, when set, causes MK5025 to access the Transmit Descriptor Ring without waiting for the transmit polltime interval to elapse. TDMD need not be set to transmit a frame, it merely hastens MK5025's response to a Transmit Descriptor Ring entry insertion by the host. TDMD is WRITE WITH ONE ONLY and cleared by the MK5025 after it is used. It may read as a "1" for a short time after it is written because the MK5025 may have been busy when TDMD was set. It is also cleared by Bus RESET. Writing a "0" in this bit has no effect.
14	STOP	STOP, when set, indicates that MK5025 is operating in the STOPPED phase of operation. All external activity is disabled and internal logic is reset. MK5025 remains inactive except for primitive processing until a START primitive is issued. STOP IS READ ONLY and set by Bus RESET or a STOP primitive. Writing to this bit has no effect.
13	DTX	Transmitter Ring Disable prevents the MK5025 from further access to the Transmitter Descriptor Ring. No transmissions are attempted after finishing transmission of any frame in transmission at the time of DTX being set. DTX is READ/WRITE. TXON acknowledges changes to DTX, see below.
12	DRX	Receiver Ring Disable prevents the MK5025 from further accesss to the Receiver

Descriptor Ring. No received frames are accepted after finishing reception of any frame in reception at the time of DRX being set. If DRX is set while a data link is established the MK5025 will go into the local busy condition and will send a RNR response frame to the remote station. DRX is READ/WRITE. RXON acknowledges changes to DRX, see below.

11 TXON

TRANSMITTER ON indicates that the transmitter ring access is enabled. TXON is set as the START primitive is issued if the DTX bit is "0" or afterward as DTX is cleared. TXON is cleared upon recognition of DTX being set, by issuing a STOP primitive in CSR1, or by a Bus RESET. If TXON is clear, the host may modify the Transmit Descriptor Ring entries regardless of the state of the OWNA bits. TXON is READ ONLY; writing this bit has no effect.

10 RXON

RECEIVER ON indicates that the receiver ring access is enabled. RXON is set as the START primitive is issued if the DRX bit is "0" or afterward as DRX is cleared. RXON is cleared upon recognition of DRX being set, by sending a STOP primitive in CSR1, or by a Bus RESET. If RXON is clear, the host may modify the Receive Descriptor Ring entries regardless of the state of the OWNA bits. RXON is READ ONLY; writing this bit has no effect.

09 INEA

INTERRUPT ENABLE allows the $\overline{\text{INTR}}$ I/O pin to be driven low when the Interrupt Flag is set. If INEA = 1 the $\overline{\text{INTR}}$ I/O pin will be low if CSR0 <08> INTR is set. If INEA = 0 the $\overline{\text{INTR}}$ I/O pin will be high, regardless of the state of the Interrupt Flag. INEA is READ/WRITE, set by writing a "1" into this bit and is cleared by writing a "0" into this bit or by Bus RESET or by issuing a STOP primitive.

08 INTR

INTERRUPT FLAG indicates that one or more of the following interrupt causing conditions has occurred; MISS, MERR, RINT, TINT, PINT, TUR or ROR. If INEA = 1 and INTR = 1 the $\overline{\text{INTR}}$ I/O pin will be low. INTR is READ ONLY, writing this bit has no effect. INTR is cleared as the specific interrupting condition bits are cleared. INTR is also cleared by Bus RESET or by issuing a STOP primitive.

07 MERR

MEMORY ERROR sets when MK5025 is the Bus Master and has not received READY within 256 SYSCLKs (25.6 usec @ 10 MHz) after asserting the address on the DAL lines. A memory error is also caused by the deassertion of HLDA during a bus transaction. When a Memory Error is detected, the receiver and transmitter are turned off and an interrupt is generated if INEA = 1. MERR is READ/CLEAR ONLY and is set by the chip and cleared by writing a "1" into the bit. Writing a "0" has no effect. It is cleared by Bus RESET or by issuing a STOP primitive.

06 MISS

MISSED PACKET is set when the receiver loses a packet because it does not own a receive buffer and the fifo has overflowed, indicating loss of a frame. When MISS is set, an interrupt will be generated if INEA = 1. MISS is READ/CLEAR ONLY and is set by MK5025 and cleared by writing a "1" into the bit. Writing a "0" has no effect. It is also cleared by Bus RESET or by issuing a STOP primitive.

05 ROR

RECEIVER OVERRUN indicates that the Receiver FIFO was full when the receiver was ready to input data to the Receiver FIFO. The frame being received is lost but is recoverable according to the Link Level protocol. When ROR is set, an interrupt is generated if INEA = 1. ROR is READ/CLEAR ONLY and is set by MK5025 and cleared by writing a "1" into the bit. Writing a "0" has no effect. It is also cleared by Bus RESET or by issuing a STOP primitive.

04 TUR

TRANSMITTER OVERRUN indicates that the MK5025 has aborted a frame since data was late from memory. This condition is reached when the transmitter and transmitter FIFO both become empty while transmitting a frame. When TUR is set, an interrupt is generated if INEA = 1. TUR is READ/CLEAR ONLY and is set by MK5025 and cleared by writing a "1" into the bit. Writing a "0" has no effect. It is also cleared by Bus RESET or by issuing a STOP primitive.

03	PINT	PRIMITIVE INTERRUPT is set after the chip updates the primitive register either to issue a provider primitive or to accept a user primitive. When PINT is set, an interrupt is generated if INEA = 1. PINT is READ/CLEAR ONLY and is set by MK5025 and cleared by writing a "1" into the bit. Writing a "0" has no effect. It is also cleared by Bus RESET or by issuing a STOP primitive.
02	TINT	TRANSMITTER INTERRUPT is set after the chip updates an entry in the Transmit Descriptor Ring. This occurs when a transmitted frame has been acknowledged by the remote station. When TINT is set, an interrupt is generated if INEA = 1. TINT is READ/CLEAR ONLY and is set by MK5025 and cleared by writing a "1" into the bit. Writing a "0" has no effect. It is also cleared by Bus RESET or by issuing a STOP primitive.
01	RINT	RECEIVER INTERRUPT is set after MK5025 updates an entry in the Receive Descriptor Ring. This occurs when the MK5025 has received a correct frame from the remote station. When RINT is set, an interrupt is generated if INEA = 1. RINT is READ/CLEAR ONLY and is set by MK5025 and cleared by writing a "1" into the bit. Writing a "0" has no effect. It is cleared by Bus RESET or by issuing a STOP primitive.
00	0	This bit is READ ONLY and read always as a zero.

4.1.2.2 Control and Status Register 1 (CSR1)

RAP<3:1> = 1

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
UERR	UAV	0	0	UPRIM <3:0>				PLOST	PAV	PPARM	1:0	PPRIM <3:0>			

BIT	NAME	DESCRIPTION
15	UERR	USER PRIMITIVE ERROR is set by the MK5025 when a primitive issued by the user is in conflict with the current status of the link. UERR is READ/CLEAR ONLY and is set by MK5025 and cleared by writing a "1" into the bit. Writing a "0" in this bit has no effect. It is also cleared by Bus RESET.
14	UAV	USER PRIMITIVE AVAILABLE is set by the user after a primitive has been placed in UPRIM. It is cleared by the MK5025 after the primitive has been processed. This bit is also cleared by a Bus RESET.
13:12	0	Reserved, must be written as zeroes.
11:08	UPRIM	USER PRIMITIVE is written by the user to control the MK5025 link procedures. The following values are valid: 0 Stop - Instructs MK5025 to go into STOPPED Mode. All link activity is terminated and the STOP bit is set. Transmitter outputs all "1"s. All DMA activity ceases. 1 Start - Instructs MK5025 to exit STOPPED Mode and enter the Disconnected Phase. Descriptor Rings are reset. Transmitter begins outputting flags. Valid only in STOPPED Mode. 2 Init Request - Instructs MK5025 to read the initialization block. Valid only in STOPPED Mode and Disconnected Phase. This should be performed prior to the start primitive after a bus reset or powerup.

3 Trans - Instructs MK5025 to enter the Transparent phase of operation. Data frames are transmitted and received out of the descriptor rings but no protocol processing is done. Address and Control Fields are not prepended to the frames, but FCS processing works normally. If the PROM bit is set in CSR2 then no address filtering is performed on received frames. Transparent Mode may be exited only with a stop primitive or by bus reset.

4 Status Request - Instructs MK5025 to write the current link status into the STATUS buffer. Valid only if INIT primitive has previously been issued.

6 Connect request - Instructs MK5025 to attempt to establish a logical link with the remote site. Valid only in Disconnected Phase.

7 Connect Response - Indicates willingness to establish a logical link with the remote site. Valid only in Disconnected Phase after receiving a Connect Indication primitive.

8 Reset Request - Instructs MK5025 to attempt to reset the current logical link with the remote site. Invalid in STOPPED Mode and Disconnected Phase.

9 Reset Response - Indicates willingness to reset current logical link with remote site. Valid only after receiving a Reset Indication primitive.

10 XID Request - Requests MK5025 to send an XID command to the remote site. Data in the XID/TEST Transmit buffer is used for the Data Field. Invalid in STOPPED Mode.

11 XID Response - Requests MK5025 to send an XID response to the remote site. Data in the XID/TEST Transmit Buffer is used for the Data Field. Valid only after receiving an XID Indication primitive.

12 TEST Request - Requests MK5025 to send a TEST command to the remote site. Data in the XID/TEST Transmit Buffer is used for the Data Field. Invalid in STOPPED Mode.

13 TEST Response - Requests MK5025 to send a TEST response to the remote site. Data in the XID/TEST transmit buffer is used for the data field. Valid only after receiving a TEST indication primitive.

14 Disconnect Request - Requests MK5025 to disconnect the current logical link. Invalid in STOPPED Mode. A DM response with the F bit clear will be sent if the link is currently disconnected.

07 PLOST — PROVIDER PRIMITIVE LOST is set by MK5025 when a provider primitive cannot be issued because the PAV bit is still set from the previous provider primitive. PLOST is cleared when PAV is cleared and by a Bus RESET. Writing to this bit has no effect.

06 PAV — PROVIDER PRIMITIVE AVAILABLE is set by the MK5025 when a new provider primitive has been placed in PPRIM. PPRIM is READ/CLEAR ONLY and is set by the chip and cleared by writing a "1" to the bit or by Bus RESET.

05:04 PPARM

PROVIDER PARAMETER provides additional information about the reason for the receipt of a disconnect, reset or error indication primitive. This field is undefined for other provider primitives. Parameters are as follows:

PPARM	Disconnect Indication	Reset Indication	Error Indication
0	Remotely Initiated	Remotely Initiated	—
1	SABM Timeout	—	Timer Rec Timeout
2	FRMR Sent and DISC or DM Received	FRMR Sent and SABM/E Recvd	FRMR Received
3	T3 Timeout	—	Unsolicited UA or F bit Received

03:00 PPRIM

PROVIDER PRIMITIVE is written by MK5025 to inform the user of link control conditions. Valid Provider Primitives are as follows:

2 Init Confirmation - Indicates that the initialization has completed.

4 Error Indication - Indicates an error condition has occurred during the Information Transfer phase of operation that requires instruction by the Host for recovery. See PPARM for specific error conditions. Either a Reset Request or Disconnect Request primitive should be issued in UPRIM after receiving an Error Indication primitive.

6 Connect Indication - Indicates an attempt by the remote site to establish a logical link. Appropriate user responses are Connect Response and Disconnect Request.

7 Connect Confirmation - Indicates the success of a previous Connect Request by the user. A logical link is now established.

8 Reset Indication - Indicates an attempt by the remote site to reset the current logical link. Appropriate user responses are Reset Response and Disconnect Request.

9 Reset Confirmation - Indicates the success of a previous Reset Request by the user. The current logical link has now been reset.

10 XID Indication - Indicates the receipt of an XID command. The Data Field of the XID command is located in the XID/TEST Receive Buffer.

11 XID Confirmation - Indicates the receipt of an XID response. The Data field of the XID response is located in the XID/TEST Receive Buffer.

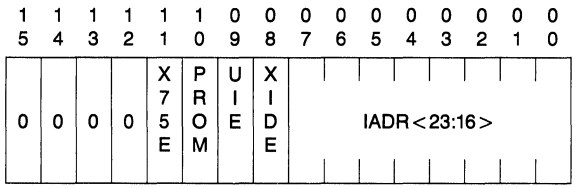
12 TEST Indication - Indicates the receipt of a TEST command. The Data Field of the TEST command is located in the XID/TEST Receive buffer.

13 TEST Confirmation - Indicates the receipt of a TEST response. The Data field of the TEST response is located in the XID/TEST Receive Buffer.

14 Disconnect Indication - Indicates a request by the remote site to disconnect the current logical link or the refusal of a previous Connect or Reset Request. The chip is now in the Disconnected Phase.

4.1.2.3 Control and Status Register 2 (CSR2)

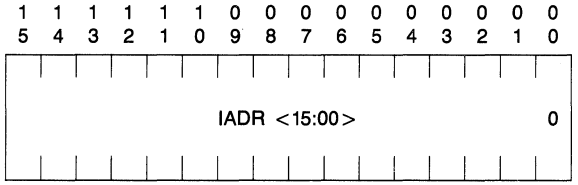
RAP<3:1> = 2



BIT	NAME	DESCRIPTION
15:12	0	Reserved, must be written as zeroes.
n	X75E	X.75 mode is enabled if this bit is set to 1; otherwise X.75 mode is enabled. This bit is READ/WRITE and cleared on Bus Reset.
10	PROM	Address filtering is disabled for transparent mode, if this bit is set. All uncorrupted incoming frames are placed in the Receive Descriptor Ring. This bit is READ/WRITE and cleared on bus reset.
09	UIE	UI frames are recognized only if this bit is set. If UIE = 0 all received UI frames will not be recognized. This bit is READ/WRITE and cleared on Bus Reset.
08	XIDE	XID frames are recognized only if this bit is set. If XIDE = 0 all received XID frames will not be recognized. This bit is READ/WRITE and cleared on Bus Reset.
07:00	IADR	The high order 8 bits of the address of the first word (lowest address) in the Initialization Block. IADR must be written by the Host prior to issuing an INIT primitive.

4.1.2.4 Control and Status Register 3 (CSR3)

RAP<3:1> = 3



BIT	NAME	DESCRIPTION
15:00	IADR	The low order 16 bits of the address of the first word (lowest address) in the Initialization Block. Must be written by the Host prior to issuing an INIT primitive. The Initialization Block must be on an even byte boundary.

4.1.2.5 Control and Status Register 4 (CRS4)

CSR4 allows redefinition of the bus master interface.

RAP<3:1> = 4

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	0	FWM <1:0>		0	BUSR	BSWPC	BURST	1:0	BSWPD	ACON	BCON

BIT	NAME	DESCRIPTION
15:10	0	Reserved, must be written as zeroes.
09:08	FWM	These bits define the FIFO watermarks. FIFO watermarks prevent the MK5025 from performing DMA transfers to/from the data buffers until the FIFOs contain a minimum amount of data or space for data. For receive data, data will only be transferred to the data buffers after the FIFO has at least N 16-bit words or an end of frame has been reached. Conversely, for transmit data, data will only be transferred from the data buffers when the transmit FIFO has room for at least N words of data. N is defined as follows:

FWM<1:0>	N
00	1 word
01	9 words
10	17 words
11	25 words

07	0	Reserved, must be written as zeroes.
06	BUSR	If this bit is set, pin 15 becomes input $\overline{\text{BUSREL}}$. If this bit is clear pin 15 is either $\overline{\text{BM0}}$ or BYTE depending on bit 00. For more information see the description for pin 15 earlier in this document.
05	BSWPC	This bit determines the byte ordering of all "non-data" DMA transfers. "Non-data" DMA transfers refers to any DMA transfers that access memory other than the data buffers themselves. This includes the Initialization Block, Descriptors, and Status Buffer. It has no effect on data DMA transfers. BSWPC allows MK5025 to operate with memory organizations that have bits <07:00> at even addresses with bits <15:08> at odd addresses or vice versa. With BSWPC = 1:

Address				Address			
XX0	0	•••	7	XX1	8	•••	15

This memory organization is used with the LSI 11 microprocessor and the 8086 microprocessor.

With BYTE SWAP = 0:

Address				Address			
XXO	8	•••	15	XX1	0	•••	7

This memory organization is used with the 68000 and Z8000 microprocessors. BSWP is Read/Write and cleared by BUS RESET.

04:03 BURST — This field determines the maximum number of data transfers performed each time control of the host bus is obtained.

BURST<1:0>	8 bit Mode	16 bit Mode
00	2 bytes	1 word
10	16 bytes	8 words
01	unlimited	unlimited

BURST is READ/WRITE and cleared on Bus RESET.

02 BSWPD — This bit determines the byte ordering of all data DMA transfers. Data transfers are those to or from a data buffer. BSWPD has no effect on non-data transfers. The effect of BSWPD on data transfers is the same as that of BSWPC on non-data transfers (see above).

01 ACON — ALE CONTROL defines the assertive state of Pin 18 when MK5025 is a Bus Master. ACON is READ/WRITE and cleared by Bus RESET.

ACON	Pin 18	Asserted
0	ALE	High
1	$\overline{AS}$	Low

00 BCON — BYTE CONTROL redefines the Byte Mask and Hold I/O pins. BCON is READ/WRITE and cleared by Bus RESET.

BCON	PIN 16	PIN 15	PIN 17
0	$\overline{BM\ 1}$	$\overline{BM\ 0}$	$\overline{HOLD}$
1	$\overline{BUSAKO}$	BYTE	$\overline{BUSRQ}$

4.1.2.6 Control and Status Register 5 (CSR5)

CSR5 facilitates control and monitoring of modem controls.

RAP<3:1> = 4

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	0	0	0	0	0	0	RTSEN	DTRD	DSRD	DTR	DSR

BIT	NAME	DESCRIPTION
15:05	0	Reserved, must be written as zeroes.
4	RTSEN	RTS/CTS ENABLE is a READ/WRITE bit used to configure pins 26 and 30. If this bit is set pin 26 becomes $\overline{RTS}$ and pin 30 becomes $\overline{DSR}$. $\overline{RTS}$ is driven low whenever the MK5025 has data to transmit and kept low during transmission. $\overline{RTS}$ will be driven high after the closing flag of a frame transmitted if either no other frames are in the FIFO or if the minimum frame spacing is higher than 2 (see Mode Register). The MK5025 will not begin transmission and TD will remain HIGH if $\overline{CTS}$ is high.
3	DTRD	DTR DIRECTION is a READ/WRITE bit used to control the direction of the DTR pin. If DTRD = 0, the DTR pin becomes an input pin and the DTR bit reflects the current value of the pin; if DTRD = 1, the DTR pin is an output pin controlled by the DTR bit below.
2	DSRD	DSR DIRECTION is a READ/WRITE bit used to control the direction of the DSR pin. If DSRD = 0, the DSR pin becomes an input pin and the DSR bit reflects the current value of the pin; if DSRD = 1, the DSR pin is an output pin controlled by the DSR bit below.
1	DTR	DATA TERMINAL READY is used to control or observe the DTR I/O pin depending on the value of DTRD. If DTRD = 0, this bit becomes READ ONLY and always equals the current value of the DTR pin. If DTRD = 1, this bit becomes READ/WRITE and any value written to this bit appears on the DTR pin.
0	DSR	DATA SET READY is used to control or observe the DSR I/O pin depending on the value of DSRD. If DSRD = 0, this bit becomes READ ONLY and always equals the current value of the DSR pin. If DSRD = 1, this bit becomes READ/WRITE and any value written to this bit appears on the DSR pin.

4.2 Initialization Block

MK5025 initialization includes the reading of the initialization block in memory to obtain the operating parameters. The Initialization Block is defined on the next page..

The Initialization Block is read by MK5025 when receiving an INIT primitive. During normal initialization the INIT should be sent prior to sending a START primitive. The user may re-issue the INIT primitive after a START, but received frames may be lost if care is not taken. An INIT cannot be issued while a link is connected; MK5025 will reject such an attempt.

Except for the Error Counters and XID/TEST Descriptor OWNA bits, the MK5025 will not write into the Initialization Block.

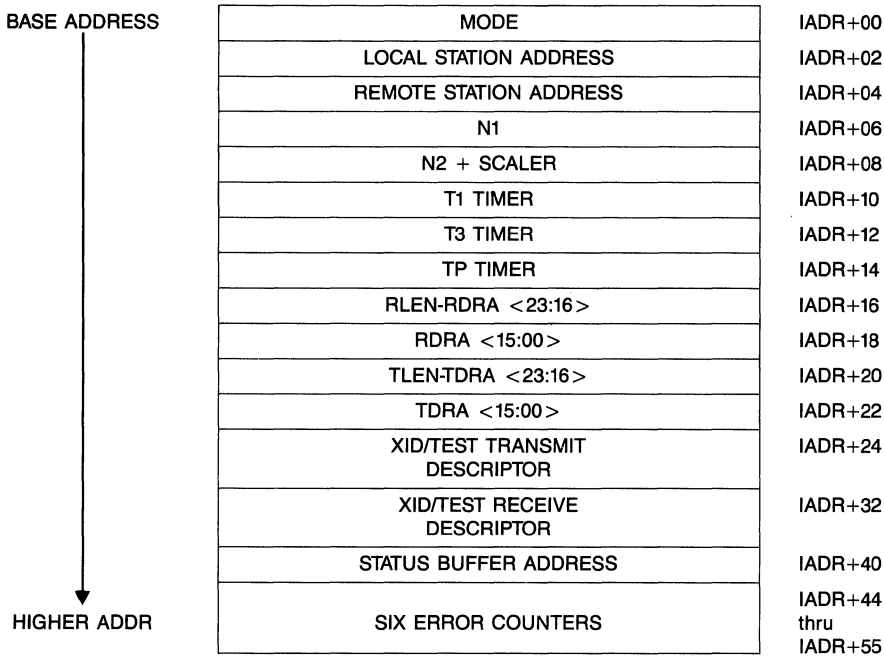
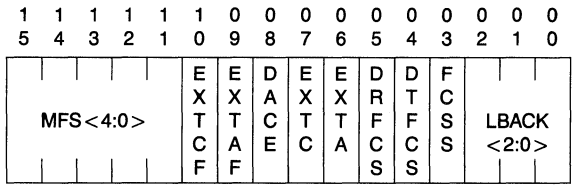


Figure 4. Initialization Block

4.2.1 Mode Register

The Mode Register allows alteration of the MK5025's operating parameters.



BIT	NAME	DESCRIPTION
15:11	MFS<4:0>	Minimum Frame Spacing defines the minimum number of flag sequences transmitted between adjacent frames transmitted by the MK5025. This only affects frames transmitted by the MK5025 and does not restrict the spacing of frames received by the MK5025. When using RTS/CTS control this field defines the number of flags transmitted at the beginning of the frame after $\overline{CTS}$ is driven low (minus one for the trailing flag). See following table for encoding of this field.

NUMBER OF FLAGS	MFS<4:0>	NUMBER OF FLAGS	MFS<4:0>
2	0	34	24
4	2	36	17
6	4	38	3
8	9	40	6
10	18	42	13
12	5	44	27
14	11	46	23
16	22	48	14
18	12	50	29
20	25	52	26
22	19	54	21
24	7	56	10
26	15	58	20
28	31	60	8
30	30	62	16
32	28		

10 EXTCF

Extended Control Force is useful only in transparent mode operation. If set along with EXTC, the receiver will assume the control field to be two bytes long regardless of the first two bits of the control field. See EXTC below.

09 EXTAF

Extended Address Force is useful only in transparent mode operation. If set along with EXTA, the receiver will assume the address field to be two bytes long regardless of the first bit of the address. See EXTA below.

08 DACE

Address and control field extraction are disabled when DACE is set. Address and control fields are treated as normal data. DACE must be written as "0" for normal operation in non-transparent mode.

07 EXTC

Extended Control Field is enabled when EXTC = 1. The control fields of all S and I frames become two octets in length, instead of one. The numbering for I frames becomes modulo 128, instead of modulo 8. The control field of U frames remains one byte in length.

06 EXTA

Extended address is enabled when EXTA is a one. The address field of all frames becomes 2 octets in length.

05 DRFCS

Disable Receiver FCS. When DRFCS = 0, the receiver will extract and check the FCS field at the end of each frame. When DRFCS = 1, the receiver continues to extract the last 16 or 32 bits of each frame, depending on FCSS, but no check is performed to determine whether the FCS is correct.

04 DTFCS

Disable Transmitter FCS. When DTFCS = 0, the transmitter will generate and append the FCS to each frame. When DTFCS = 1, the FCS logic is disabled, and no FCS is generated with transmitted frames.

Setting DTFCS = 1 is useful in loopback testing for checking the ability of the receiver to detect an incorrect FCS.

03 FCSS

FCS Select. When FCSS = 0, a 16 bit FCS is selected otherwise a 32-bit FCS is used.

02:00 LBACK Loopback Control puts the MK5025 into one of several loopback configurations.

LBACK	Description
0	Normal operation. No loopback.
4	Simple loopback. Receive data and clock are driven internally by transmit data and clock.
5	Clockless loopback. Receive data is driven internally by transmit data. Transmit and receive clocks are driven by SYSCLK divided by 8.
6	Silent loopback. Same as simple loopback with TD pin forced to all ones.
7	Silent Clockless loopback. Combination of Silent and Clockless loopbacks. Receive data is driven internally by transmit data, transmit and receive clocks are driven by SYSCLK divided by 8. TD pin is forced to all ones.

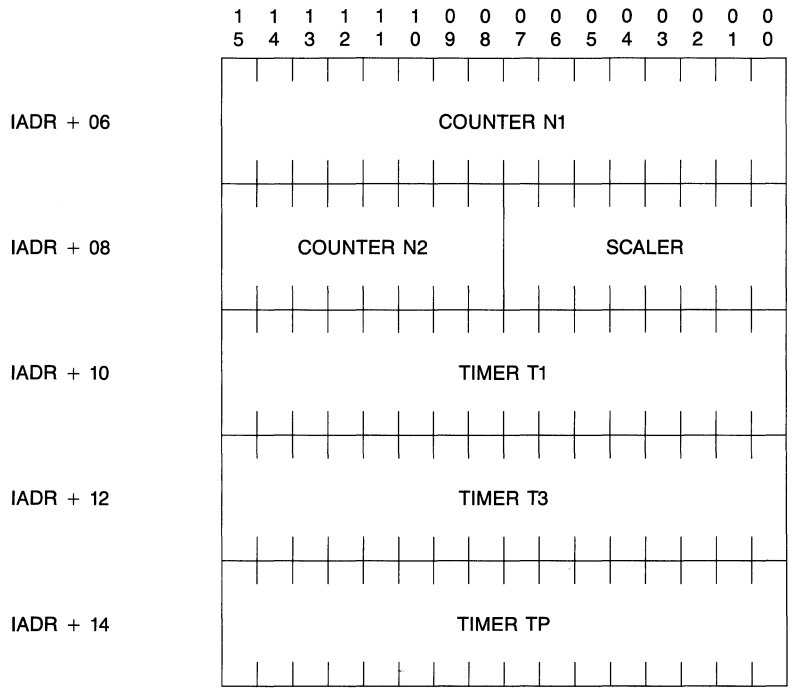
4.2.2 Station Addresses

The Local and Remote station addresses may be either one or two octets according to the EXTA control bit described in the MODE register. If extended address mode is selected bit 0 should be set to a zero for adherence to ADCCP/HDLC. If extended address mode is not selected, the command and response frame addresses should be located in the lower order byte of their respective fields.

4.2.3 Timers

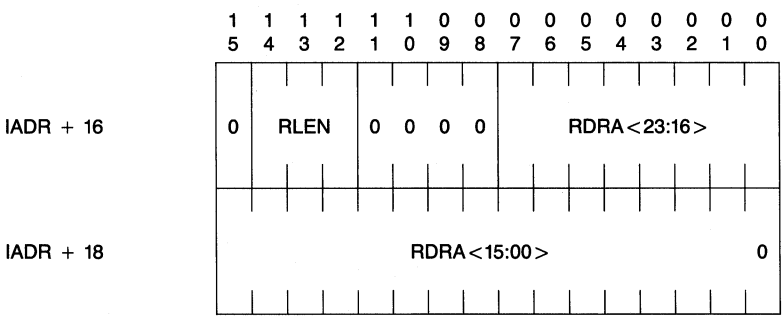
There are ten independent counter-timers. The lower 8 bits of IADR+08 are used as a scaler for T1, T3, and TP. The scaler is driven by a clock which is 1/32 of SYSCLK. N1 is a 16 bit counter and is used to count the number of bytes in an I-frame. N2 is an 8 bit counter.

The Host will write the period of N1, N2, T1, T2, T3, and TP into the Initialization Block.



TIMER	DESCRIPTION
N1	MAXIMUM FRAME LENGTH. This field must contain the two's complement of the maximum allowable frame length, in bytes. Any frame received that exceeds this count will be discarded.
N2	MAXIMUM RETRANSMISSION COUNT. This field must contain the two's complement of the maximum number of retransmissions that will be made following the expiration of T1.
SCALER	TIMER PRESCALER. Timers T1, T3, and TP are scaled by this number. The prescaler incremented once every 32 system clock pulses. When it reaches zero the timers are incremented and the prescaler is reset. This field is interpreted as the two's complement of the prescaler period. Note: a prescale value of one gives the smallest amount of scaling to the timers (64 clock pulses), zero gives the largest (8192 clock pulses).
T1	RETRANSMISSION TIMER. Link control frames will be retransmitted upon the expiration of the T1 timer if the appropriate response is not received. These frames will be retransmitted up to N2 (see above) times, at which time the link will be disconnected or reset by MK5025 according to the X.25 protocol. This field must contain the two's complement of the period of timer T1. The scaled (see SCALER) value of T1 should be made large enough to allow the remote station to receive the control frame and send its response.
T3	LINK IDLE TIMER. The link idle timer determines the amount of link idle time necessary to consider the link disconnected. This field must contain the two's complement of the period of timer T3. T3 is disabled if CSR5 RTSEN = 1 or if the MK5025 is in transparent mode.
TP	TRANSMIT POLLING TIMER. This scaled timer determines the length of time between transmit frame checks. Unless TDMD (see CSR0) is set or a frame is received on the link, no attempt to transmit a frame in the transmit descriptor ring is made until TP expires. At TP expiration all transmit frames in the transmit descriptor ring will be sent.

4.2.4 Receive Descriptor Ring Pointer

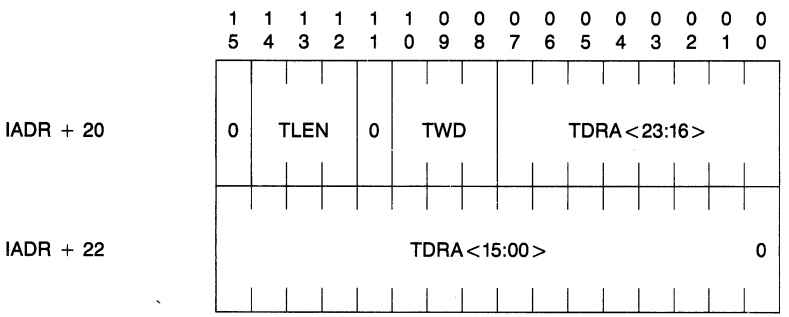


BIT	NAME	DESCRIPTION
15	0	Reserved, must be written as a zero.
14:12	RLEN	RECEIVE RING LENGTH is the number of entries in the Receive Ring expressed as a power of two.

RLEN	NUMBER OF ENTRIES
0	1
1	2
2	4
3	8
4	16
5	32
6	64
7	128

11:08	0	Reserved, must be written as zeroes.
07:00/ 15:00	RDRA	RECEIVE DESCRIPTOR RING ADDRESS is the base address of (lowest address) of the Receive Descriptor Ring. The Receive Ring must be aligned on a word boundary.

4.2.5 Transmit Descriptor Ring Pointer



BIT	NAME	DESCRIPTION
15	0	Reserved, must be written as a zero.
14:12	TLEN	TRANSIT RING LENGTH is the number of entires in the Transmit Ring expressed as a power of two.
11	0	Reserved, must be written as a zero.
10:08	TWD	TRANSMIT WINDOW is the window size of the Transmitter expressed as a power of two less one. TWD must be less than TLEN. TWD is the maximum number of I frames which may be transmitted without an acknowledgement. TWD is not allowed to be greater than 127.

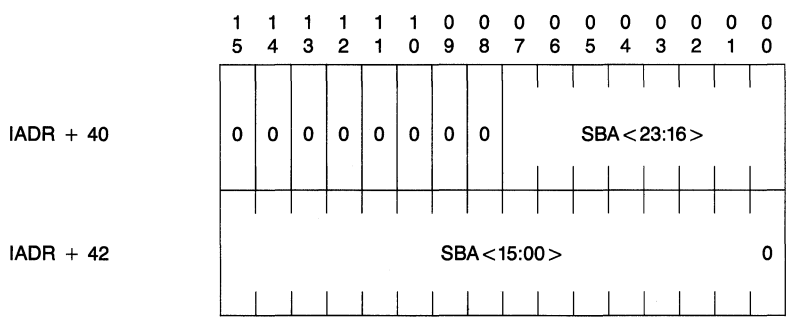
TLEN	NUMBER OF ENTRIES	TWD	WINDOW SIZE EXTC = 0	WINDOW SIZE EXTC = 1
0	1	0	NA	1
1	2	1	1	3
2	4	2	2	7
3	8	3	3	15
4	16	4	4	31
5	32	5	5	63
6	64	6	6	127
7	128	7	7	127

07:00/ 15:00 TDRA — TRANSMIT DESCRIPTOR RING ADDRESS is the base address of (lowest address) of the Transmit Descriptor Ring. The Transmit Ring must be aligned on a word boundary.

4.2.6 XID/TEST Descriptors

The XID/TEST Descriptors contain pointers to the buffers used to receive and transmit XID and TEST frames, as well as the buffer lengths. The exact format of these descriptors can be seen below under Receive and Transmit Message Descriptor Entry descriptions. They are used the same as other descriptors except that no data chaining takes place and only the OWNA bit is significant in RMD0 and TMD0.

4.2.7 Status Buffer Address



BIT	NAME	DESCRIPTION
15:08	0	Reserved, must be written as zeroes.
07:00 15:00	SBA	STATUS BUFFER ADDRESS points to a 3 word buffer into which link status information is placed upon the issuance of the STAT primitive by the HOST. The contents of the Status Buffer are described later in this document. The Status Buffer must begin on a word boundary.

4.2.8 Error Counters

Six locations in the initialization buffer are reserved for use as error counters which the MK5025 will increment. These are intended for use of the Host CPU for statistical analysis. The MK5025 will only increment the counters; it is up to the user to clear and preset these counters. The error counters are:

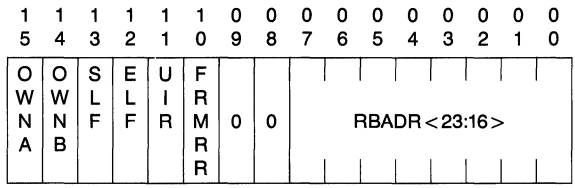
MEMORY ADDRESS	ERROR COUNTER
IADR + 44	Bad frames received - Bad FCS - Non-Octet Aligned
IADR + 46	Number of FRMR frames received
IADR + 48	Number of T1 timeouts
IADR + 50	Number of REJ frames received
IADR + 52	Number of REJ frames transmitted
IADR + 54	Frames shorter than minimum length received

4.3 Receive and Transmit Descriptor Rings

Each descriptor ring in memory is a 4 word entry. The following is the format of the receive and transmit descriptors.

4.3.1 Receive Message Descriptor Entry

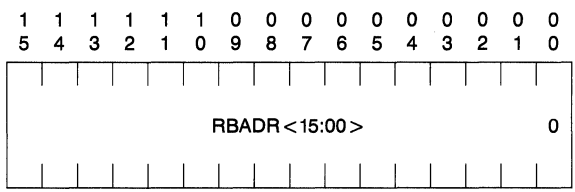
4.3.1.1 Receive Message Descriptor 0 (RMD0)



BIT	NAME	DESCRIPTION
15	OWNA	When this bit is a zero either the HOST or the I/O ACCELERATION PROCESSOR owns this descriptor. When this bit is a one the MK5025 owns this descriptor. The chip clears the OWNA bit after filling the buffer pointed to by the descriptor entry provided the received frame had a good FCS, N(r), and N(s). The Host sets the OWNA bit after emptying the buffer. Once the MK5025, Host, or I/O acceleration processor has relinquished ownership of a buffer, it may not change any field in the four words that comprise the descriptor entry.
14	OWNB	This bit determines whether the HOST or the SLAVE PROCESSOR owns the buffer when OWNA is a zero. The MK5025 never uses this bit. This bit is provided to facilitate use of an I/O acceleration processor.

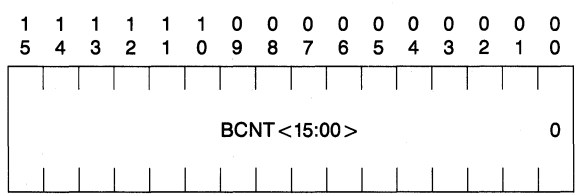
13	SLF	Start of Long Frame indicates that this is the first buffer used by MK5025 for this frame. It is used for data chaining buffers. SLF is set by the chip. NOTE: A "Long Frame" is any frame which needs data chaining. Usually this will be an I frame, but it could also be a UI or FRMR frame.
12	ELF	End of Long Frame indicates that this the last buffer used by MK5025 for this frame. It is used for data chaining buffers. If both SLF and ELF were set the frame would fit into one buffer and no data chaining would be required. ELF is set by the MK5025.
11	UIR	UI Frame Received indicates that a UI frame has been received and is stored in this buffer.
10	FRMRR	FRMR Received indicates that the I-field of a FRMR is stored in the buffer referenced by this Message Descriptor.
09:08	0	Reserved, must be written as zeroes.
07:00	RBADR	The High Order 8 address bits of the buffer pointed to by this descriptor. This field is written by the Host and unchanged by MK5025.

4.3.1.2 Receive Message Descriptor 1 (RMD1)



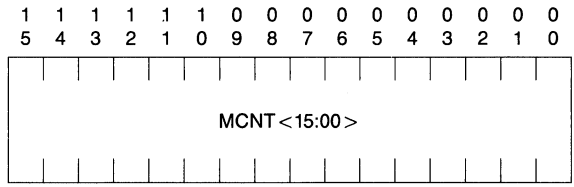
BIT	NAME	DESCRIPTION
15:00	RBADR	The low order 16 address bits of the receive buffer pointed to by this descriptor. RBADR is written by the Host CPU and unchanged by MK5025. The receive buffers must be word aligned.

4.3.1.3 Receive Message Descriptor 2 (RMD2)



BIT	NAME	DESCRIPTION
15:00	BCNT	Buffer Byte Count is the length of the buffer pointed to by this descriptor expressed in two's complement. This field is written to by the Host and unchanged by MK5025. Buffer size must be even.

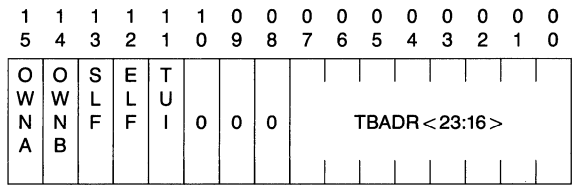
4.3.1.4 Receive Message Descriptor 3 (RMD3)



BIT	NAME	DESCRIPTION
15:00	MCNT	Message Byte Count is the length, in bytes, of the contents of the buffer expressed in two's complement. If ELF = 0, MCNT will equal the two's complement of BCNT since the MK5025 will fill a buffer before chaining to the next descriptor.

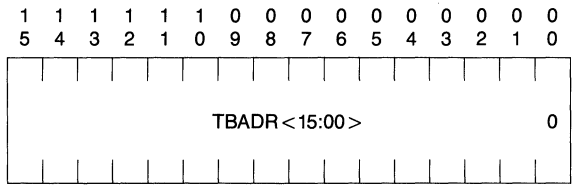
4.3.2 Transmit Message Descriptor Entry

4.3.2.1 Transmit Message Descriptor 0 (TMD0)



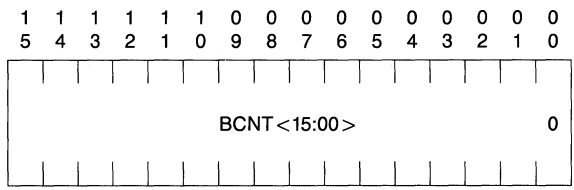
BIT	NAME	DESCRIPTION
15	OWNA	When this bit is a zero either the HOST or the SLAVE PROCESSOR owns this descriptor. When this bit is a one the MK5025 owns this descriptor. The host should set the OWNA bit after filling the buffer pointed to by the descriptor entry. The MK5025 releases the descriptor after transmitting the buffer and receiving the proper acknowledgement from the remote station. After the MK5025, Host, or I/O acceleration processor has relinquished ownership of a buffer, it may not change any field in the four words that comprise the descriptor entry.
14	OWNB	This bit determines whether the HOST or the I/O ACCELERATION PROCESSOR owns the buffer when OWNA is a zero. The MK5025 never uses this bit. This bit is provided to facilitate use of an I/O acceleration processor.
13	SLF	Start of Long Frame indicates that this is the first buffer used by MK5025 for this frame. It is used for data chaining buffers. SLF is set by the Host. NOTE: A "Long Frame" is any frame which needs data chaining. Usually this will be an I frame, but it could also be a UI frame or others.
12	ELF	End of Long Frame indicates that this the last buffer used by MK5027 for this frame. It is used for data chaining buffers. If both SLF and ELF were set the frame would fit into one buffer and no data chaining would be required. ELF is set by the Host.
11	TUI	Transmit a UI frame indicates that a UI frame is to be transmitted from the transmit buffer instead of a normal I frame. This bit must also be set for anything transmitted while the MK5025 is in Transparent Mode.
10:08	0	Reserved, must be written as zeroes.
07:00	TBADR	The High Order 8 address bits of the buffer pointed to by this descriptor. This field is written by the Host and unchanged by MK5025.

4.3.2.2 Transmit Message Descriptor 1 (TMD1)



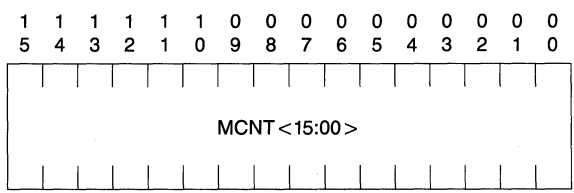
BIT	NAME	DESCRIPTION
15:00	TBADR	The Low Order 16 address bits of the buffer pointed to by this descriptor. TBADR is written by the Host and unchanged by MK5025. The least significant bit is zero since the descriptor must be word aligned.

4.3.2.3 Transmit Message Descriptor 2 (TMD2)



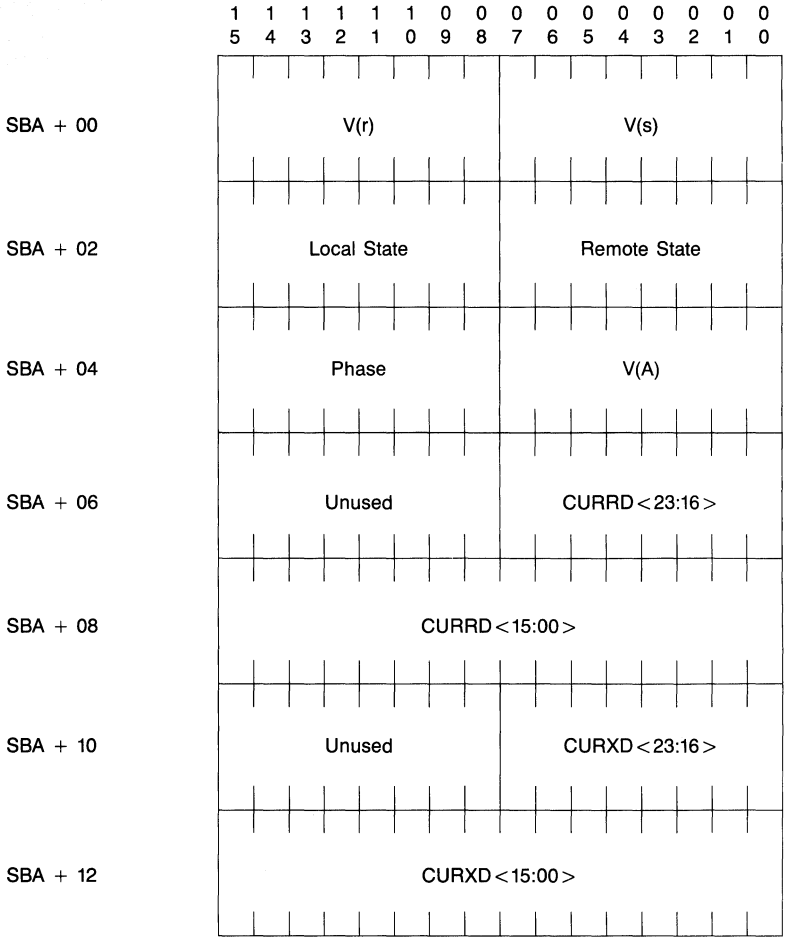
BIT	NAME	DESCRIPTION
15:00	BCNT	Buffer Byte Count is the usable length, in bytes, of the buffer pointed to by this descriptor in two's complement. This field is not used by the MK5025.

4.3.2.4 Transmit Message Descriptor 3 (TMD3)



BIT	NAME	DESCRIPTION
15:00	MCNT	Message byte count is the length, in bytes, of the contents of the buffer associated with this descriptor expressed as a two's complement.

4.3.3 Status Buffer



FIELD	DESCRIPTION
V(r)	Current value of the Receive Count Variable. 0 <= V(r) <= 7 for non-extended control; 0<= V(r) <= 127 for extended control.
V(s)	Current value of the Transmit Count Variable. 0 <= V(s) <= 7 for non-extended control; 0<= V(s) <= 127 for extended control.
Local State	Current state of local station.

Value	Description
0	Normal Data Transfer state
1	Local Busy state
2	REJ sent state
3	DISC sent state
4	Normal Disconnected state
5	SABM/E sent for link connection
6	FRMR sent state
7	SABM/E sent for link reset

Remote State

Current state of remote station.

Value	Description
0	Normal Data Transfer state
1	Remote Busy state

Phase

Current phase of operation.

Value	Description
−1	Stopped Mode
0	Information Transfer phase
1	Disconnected phase
2	Resetting phase
3	Transparent Data Transfer phase

V(A)

Current value of Transmit Acknowledge Count.. This field contains the value of the N(r) of the most recently received S or I frame. The modulo difference between V(A) and V(s) determines the number of outstanding I frames that have not been acknowledged by the remote station.

CURRD<23:00>

Current Receive Descriptor. This pointer indicates the position of the descriptor for the next receive buffer to be filled.

CURRXD<23:00>

Current Transmit Descriptor. This pointer indicates the position of the descriptor for the next transmit buffer to be transmitted.

4.4 Data Link Services

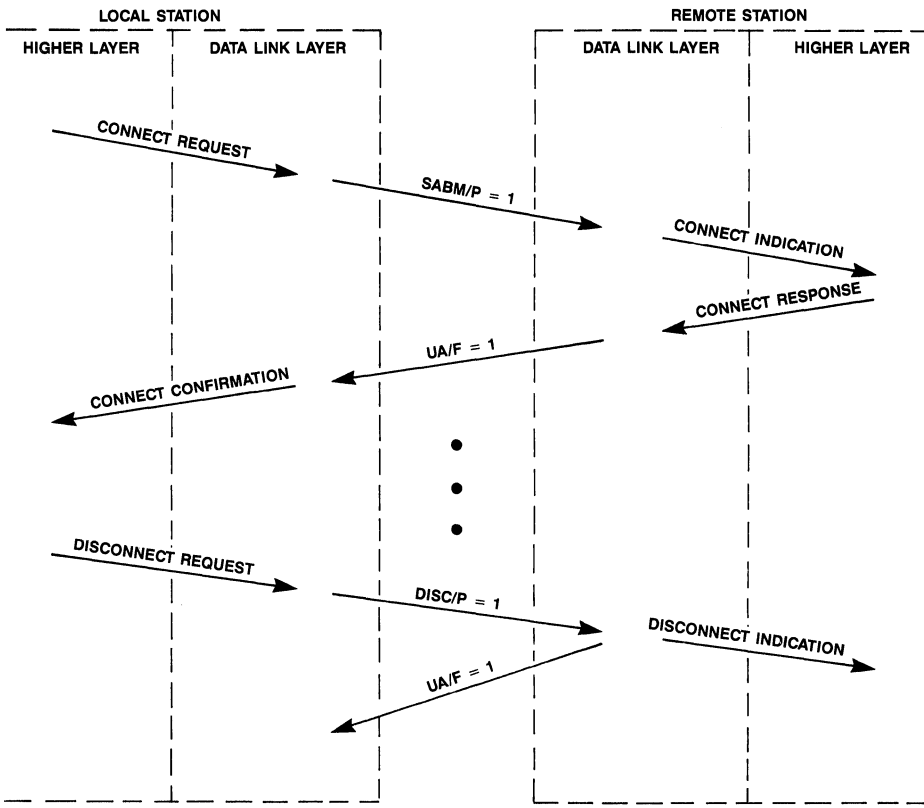
The MK5025 is consistent with the ISO Data Link Service Definition in providing services to the HOST. The following section is a brief description of this interface.

All link oriented services are provided through the exchange of Data Link Service Primitives. These primitives provide both confirmed and unconfirmed services to the HOST. Each primitive falls into one of the following categories:

1. Link Establishment (Connection)
2. Link Resetting
3. Link Disconnection
4. Data Transfer

A primitive is also one of the following types:

1. Request
2. Response
3. Indication
4. Confirmation



Example of Confirmed and Unconfirmed Data Link Services

Requests and Responses are issued by the HOST and Indications and Confirmations are issued by the MK5025.

Responses and Confirmations are not used for unconfirmed exchanges. Only the link disconnection service is unconfirmed.

A Request will be issued by the HOST when a service is required. An Indication will be issued by the MK5025 when the remote system is attempting to change the data link status. A Response is issued by the HOST when receiving an indication for a confirmed service. A confirmation is issued by the MK5025 when the remote system has responded to a previously requested service.

In the MK5025, primitives are exchanged two ways: through the CSR1 and through the OWN bits in the descriptor rings. Connection, disconnection, and link reset primitives are exchanged through CSR1. Data primitives are handled transparently by the OWN bit handshaking in the Descriptor Rings.

Eight additional primitives have been included in the MK5025 to handle services not mentioned in the ISO Data Link Service definition. These primitives include:

1. STOP - Disables the MK5025 from link operation.

2. INIT - Instructs the MK5025 to read the initialization block.

3. START - Enables the MK5025 for link operation.

4. TRANS - Enables the MK5025 for transparent operation.

5. ERROR - Indicates the occurence of a link error requiring higher level action.

6. STAT - Instructs the MK5025 to write chip status in the status buffer.

7. XID - Confirmed exchange of identification (X.32 mode only).

8. TEST - Provides a full remote loopback test facility.

For examples of the use of primitives, see the section on detailed programming procedures below.

4.5 Detailed Programming Procedures

4.5.1 Initialization

The following procedures should be followed to initialize the MK5025:

1. Setup bus control information in CSR4.

2. Setup Initialization Block and Descriptor Rings and load the address of the initialization block in CSR's 2 and 3.

3. Issue the INIT primitive through CSR1 instructing the MK5025 to read the initialization block information.

4. Wait for INIT Confirmation primitive from the MK5025.

5. Issue the START Primitive through CSR1 to enable the MK5025 for link operation.

6. Enable interrupts in CSR0 if desired.

4.5.2 Active Link Setup

1. Issue the Connect Request primitive through CSR1. The MK5025 will attempt to establish a logical link.

2. Wait for a Connect Confirm primitive from the MK5025.

3. If a Connect Confirm primitive is received, a link has been established.

4. If a Disconnect Indication primitive is received, the MK5025 has been unable to establish a link. The reason will be in the PPARM field of CSR1.

4.5.3 Passive Link Setup

The following procedures should be followed to passively establish a link:

1. Issue a Disconnect Request primitive. A DM frame with F bit clear will be sent to the remote station requesting link setup. This step is optional.

2. Wait for a Connect Indication primitive from the MK5025.

3. If a Connect Indication primitive is received, issue a Connect Response primitive to indicate willingness to establish the link. The link is now established.

4. If no Connect Indication primitive is received, the remote site is not trying to actively setup a link.

4.5.4 Refusing Link Setup

The following procedure should be followed when refusing link establshment:

1. A Connect Indication will be received indicating a request by the remote station to establish a link.
2. Issue a Disconnect Request to refuse the link establishment request.

4.5.5 Sending Data

The following procedure should be followed to send a data frame:

1. Wait for OWNA bit of current transmit descriptor to be cleared, if not already.
2. Fill buffer associated with current transmit descriptor with data to be sent.
3. Repeat steps 1 and 2 for next buffer if chaining is necessary, setting SLF and ELF appropriately.
4. Set the OWNA bit for each descriptor used.
5. Go on to next descriptor. these OWNA bits will be cleared when the data has been sucessfully sent and acknowledged.

4.5.6 Receiving Data

The following procedure should be followed when receiving a data frame:

1. Make sure that the OWNA bit of the current receive descriptor is clear.
2. Read data out of buffer associated with current receive descriptor.
3. Set the OWNA bit of current descriptor.
4. If ELF bit of current descriptor is clear, go on to next descriptor and repeat above steps appending data from each buffer until a descriptor with the ELF bit set is reached.

4.5.7 Link Disconnection

The following procedure should be followed to disconnect an established link:

1. Issue the Disconnect Request primitive to the MK5025. The MK5025 will disconnect the link.

4.5.8 Link Reset

The following procedure should be followed to reset an established link:

1. Issue a Reset Request primitive to the MK5025.
2. Wait for a Reset Confirm primitive from the MK5025.
3. If a Reset Confirm primitive is received, the link has been reset.
4. If a Disconnect Indication is received, the MK5025 was unable to reset and has disconnected. The reason for failure is in the PPARM field of CSR1. Link connection procedures must now be performed to re-establish the link.

4.5.9 Receiving Link Reset

The following procedure should be followed when receiving a request for link reset:

1. A Reset Indication will be received from the MK5025 indicating the remote station has requested a link resetting.

2. At this time the host may wish to remove any unacknowledged frames in the Transmit Descriptor Ring to avoid possible duplication at reset.

3. If able to reset, issue a reset response to indicate willingness to reset the link.

4. If unable to reset, issue a Disconnect Request to disconnect the link.

4.5.10 Receiving FRMR frame

The following procedure should be followed when receiving a FRMR:

1. An Error Indication will be received from MK5025 indicating an error condition. PPARM will indicate a FRMR frame has been received. The I-field of the FRMR has been placed in the next Receive Descriptor.

2. If able to reset, issue a Reset Request to MK5025 and wait for either a Reset Indication or a Disconnect Indication as described above for Link Reset.

3. If unable to reset, issue a Disconnect Request to disconnect the current link. Link setup procedures should now be performed to re-establish a link.

4.5.11 Exchanging Identification

The following procedure should be followed to exchange identification with the remote:

1. XIDE in CSR3 must be set prior to any identification exchange.

2. Place identification information in the XID/TEST Transmit Buffer.

3. Issue an XID Request primitive.

4. If an XID Confirm primitive is received, the identication exchange has been performed and the remote response is located in the XID/TEST receive buffer.

4. If a Disconnect Indication is received, the identification exchange was unsuccessful.

4.5.12 Receiving an identification request

The following procedure should be performed when receiving a request for identification:

1. An XID Indication primitive will be received from the MK5025 to indicate the request for identification. The remote identification information will be located in the XID/TEST receive buffer.

2. To respond, place identification information in the XID/TEST send buffer and issue an XID Response primitive.

3. To refuse, issue a Disconnect Request primitive.

Note: An XID Indication will only be issued of the XIDE bit in CSR3 has been set. Otherwise, all identification requests will automatically be refused and XID frames will not be recognized.

4.5.13 Disabling the MK5025

The following procedure should be followed to disable the MK5025:

1. Issue the STOP primitive. This will disable the MK5025 from receiving or transmitting. The TD pin will be held high while the MK5025 is in stopped mode. The STOP bit in CSR0 will be set and interrupts disabled. If a link is currently established, data may be lost.

4.5.14 Re-enabling the MK5025

The same procedure should be followed for re-enabling the MK5025 as was used to initialize upon power-up. If the Initialization Block and the hardware configuration have not changed then steps 1 thru 3 may be omitted.

SECTION 5
MK5025 ELECTRICAL SPECIFICATION

ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias . . . . . −25°C to +100°C
Storage Temperature . . . . . −65°C to +150°C
Voltage on Any Pin with Respect to Ground . . . . . −0.5 V to V_{CC} +0.5 V
Power Dissipation . . . . . 0.50 W

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

T_A=0°C to 70°C, V_{CC} = +5 V ±5 percent unless otherwise specified.

SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{IL}		−0.5		+0.8	V
V_{IH}		+2.0		V_{CC} +0.5	V
V_{OL}	@ I_{OL} = 3.2 mA			+0.5	V
V_{OH}	@ I_{OH} = −0.4 mA	+2.4			V
I_{IL}	@ V_{in} = 0.4 to V_{CC}			±10	μA
I_{CC}	T_{SCT} = 100 ns		50		mA

CAPACITANCE

Frequency = 1 MHz

SYMBOL	CONDITIONS	MIN	MAX	UNITS
C_{IN}			10	pf
C_{OUT}			10	pf
C_{IO}			20	pf

AC TIMING SPECIFICATIONS

T_A = 0°C to 70°C, V_{CC} = +5 V ±5 percent, unless otherwise specified.

NO.	SIGNAL	SYMBOL	PARAMETER	TEST CONDITIONS	MIN ns	TYP ns	MAX ns
1	SYSCLK	T_{SCT}	SYSCLK period		100		
2	SYSCLK	T_{SCL}	SYSCLK low time		45		
3	SYSCLK	T_{SCH}	SYSCLK high time		45		
4	SYSCLK	T_{SCR}	Rise time of SYSCLK		0		8
5	SYSCLK	T_{SCF}	Fall time of SYSCLK		0		8
6	$\overline{TCLK}$	T_{TCT}	$\overline{TCLK}$ period		140		
7	$\overline{TCLK}$	T_{TCL}	$\overline{TCLK}$ low time		63		
8	$\overline{TCLK}$	T_{TCH}	$\overline{TCLK}$ high time		63		
9	$\overline{TCLK}$	T_{TCR}	Rise time of $\overline{TCLK}$		0		8
10	$\overline{TCLK}$	T_{TCF}	Fall time of $\overline{TCLK}$		0		8
11	TD	T_{TDP}	TD data propagation delay after the falling edge of $\overline{TCLK}$	C_L = 50 pF			40
12	TD	T_{TDH}	TD data hold time after the falling edge of $\overline{TCLK}$	C_L = 50 pF	5		

AC TIMING SPECIFICATIONS

T_A = 0°C to 70°C, V_{CC} = +5 V ±5 percent, unless otherwise specified.

NO.	SIGNAL	SYMBOL	PARAMETER	TEST CONDITIONS	MIN ns	TYP ns	MAX ns
13	$\overline{RCLK}$	T_{RCT}	$\overline{RCLK}$ period		140		
14	$\overline{RCLK}$	T_{RCH}	$\overline{RCLK}$ high time		63		
15	$\overline{RCLK}$	T_{RCL}	$\overline{RCLK}$ low time		63		
16	$\overline{RCLK}$	T_{RCR}	Rise time of $\overline{RCLK}$		0		8
17	$\overline{RCLK}$	T_{RCF}	Fall time of $\overline{RCLK}$		0		8
18	RD	T_{RDR}	RD data rise time		0		8
19	RD	T_{RDF}	RD data fall time		0		8
20	RD	T_{RDH}	RD hold time after rising edge of $\overline{RCLK}$		5		
21	RD	T_{RDS}	RD setup time prior to rising edge of $\overline{RCLK}$		30		
22	A/DAL	T_{DOFF}	Bus Master driver disable after rising edge of $\overline{HOLD}$		0		50
23	A/DAL	T_{DON}	Bus Master driver enable after falling edge of $\overline{HLDA}$	T_{SCT} = 100 nS	0		200
24	$\overline{HLDA}$	T_{HHA}	Delay to falling edge of $\overline{HLDA}$ from falling edge of $\overline{HOLD}$ (Bus Master)		0		
25	$\overline{RESET}$	T_{RW}	$\overline{RESET}$ pulse width		30		
26	A/DAL	T_{CYCLE}	Read/write, address/data cycle time	T_{SCT} = 100 nS	600		
27	A	T_{XAS}	Address setup time to falling edge of ALE		100		
28	A	T_{XAH}	Address hold time after the rising edge of $\overline{DAS}$		50		
29	DAL	T_{AS}	Address setup time to the falling edge of ALE		75		
30	DAL	T_{AH}	Address hold time after the falling edge of ALE		20		
31	DAL	T_{RDAS}	Data setup time to the rising edge of $\overline{DAS}$ (Bus master read)		55		
32	DAL	T_{RDAH}	Data hold time after the rising edge of $\overline{DAS}$ (Bus master read)		0		
33	DAL	T_{DDAS}	Data setup time to the falling edge of $\overline{DAS}$ (Bus master write)		0		
34	DAL	T_{WDS}	Data setup time to the rising edge of $\overline{DAS}$ (Bus master write)		250		
35	DAL	T_{WDH}	Data hold time after the rising edge of $\overline{DAS}$ (Bus master write)		35		
36	DAL	T_{SRDH}	Data hold time after the rising edge of $\overline{DAS}$ (Bus slave read)	T_{SCT} = 100 nS	0		35
37	DAL	T_{SWDH}	Data hold time after the rising edge of $\overline{DAS}$ (Bus slave write)		0		
38	DAL	T_{SWDS}	Data setup time to the falling edge of $\overline{DAS}$ (Bus slave write)		0		
39	ALE	T_{ALEW}	ALE width high		110		

AC TIMING SPECIFICATIONS

T_A = 0°C to 70°C, V_{CC} = +5 V ±5 percent, unless otherwise specified.

NO.	SIGNAL	SYMBOL	PARAMETER	TEST CONDITIONS	MIN ns	TYP ns	MAX ns
40	ALE	T_{DALE}	Delay from rising edge of $\overline{DAS}$ to the rising edge of ALE		70		
41	$\overline{DAS}$	T_{DSW}	$\overline{DAS}$ width low		200		
42	$\overline{DAS}$	T_{ADAS}	Delay from the falling edge of ALE to the falling edge of $\overline{DAS}$		80		
43	$\overline{DAS}$	T_{RIDF}	Delay from the rising edge of $\overline{DALO}$ to the falling edge of $\overline{DAS}$ (Bus master read)		35		
44	$\overline{DAS}$	T_{RDYS}	Delay from the falling edge of $\overline{READY}$ to the rising edge of $\overline{DAS}$	T_{ARYD}=300 nS T_{SCT}=100 nS	120		200
45	$\overline{DALI}$	T_{ROIF}	Delay from the rising edge of $\overline{DALO}$ to the falling edge of $\overline{DALI}$ (Bus master read)		70		
46	$\overline{DALI}$	T_{RIS}	$\overline{DALI}$ setup time to the rising edge of $\overline{DAS}$ (Bus master read)		150		
47	$\overline{DALI}$	T_{RIH}	$\overline{DALI}$ hold time after the rising edge of $\overline{DAS}$ (Bus master read)		0		
48	$\overline{DALI}$	T_{RIOF}	Delay from the rising edge of $\overline{DALI}$ to the falling edge of $\overline{DALO}$ (Bus master read)		70		
49	$\overline{DALO}$	T_{OS}	$\overline{DALO}$ setup time to the falling edge of ALE (Bus master read)		110		
50	$\overline{DALO}$	T_{ROH}	$\overline{DALO}$ hold time after the falling edge of ALE (Bus master read)		35		
51	$\overline{DALO}$	T_{WDSI}	Delay from the rising edge of $\overline{DAS}$ to the rising edge of $\overline{DALO}$ (Bus master write)		50		
52	$\overline{CS}$	T_{CSH}	$\overline{CS}$ hold time after the rising edge of $\overline{DAS}$ (Bus slave)		0		
53	$\overline{CS}$	T_{CSS}	$\overline{CS}$ setup time to the falling edge of $\overline{DAS}$ (Bus slave)		0		
54	ADR	T_{SAH}	ADR hold time after the rising edge of $\overline{DAS}$ (Bus slave)		0		
55	ADR	T_{SAS}	ADR setup time to the falling edge of $\overline{DAS}$ (Bus slave)		0		
56	$\overline{READY}$	T_{ARYD}	Delay from the falling edge of ALE to the falling edge $\overline{READY}$ to insure a minimum bus cycle time (600 nS)	T_{SCT} = 100 nS			150
57	$\overline{READY}$	T_{SRDS}	Data setup time to the falling edge of $\overline{READY}$ (Bus slave read)		75		
58	$\overline{READY}$	T_{RDYH}	$\overline{READY}$ hold time after the rising edge of $\overline{DAS}$ (Bus master)		0		
59	$\overline{READY}$	T_{SRYH}	$\overline{READY}$ hold time after the rising edge of $\overline{DAS}$ (Bus slave)	T_{SCT} = 100 nS	0		35
60	READ	T_{SRH}	READ hold time after the rising edge of $\overline{DAS}$ (Bus slave)		0		
61	READ	T_{SRS}	READ setup time to the falling edge of $\overline{DAS}$ (Bus slave)		0		
62	$\overline{READY}$	T_{RDYD}	Delay from falling edge of $\overline{DAS}$ to falling edge of $\overline{READY}$ (Bus slave read)	T_{SCT} = 100 nS		200	

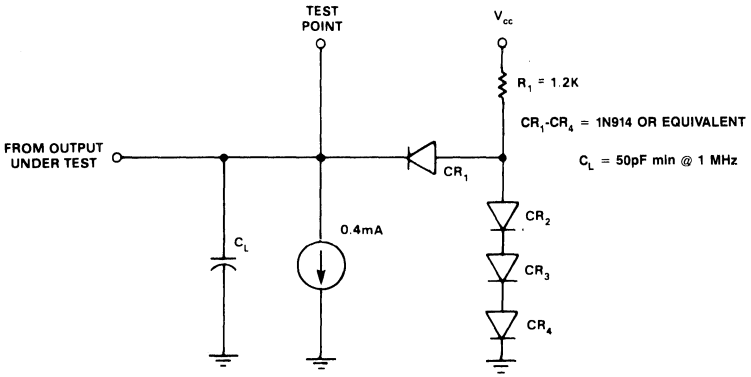
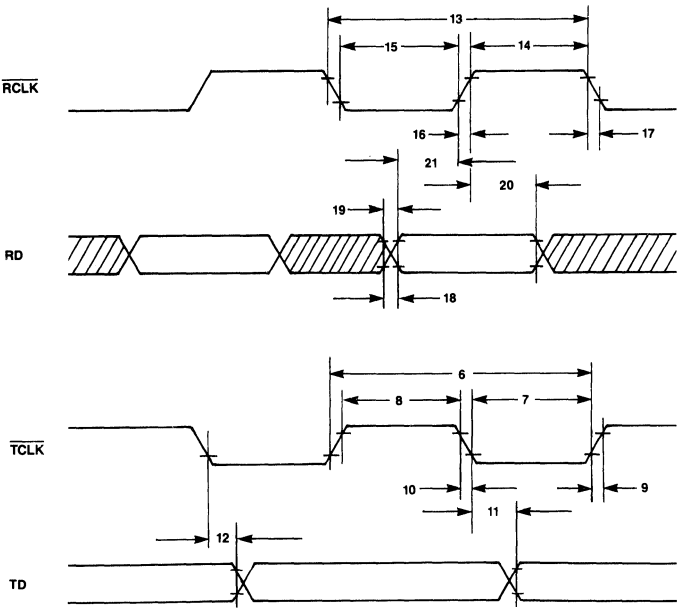


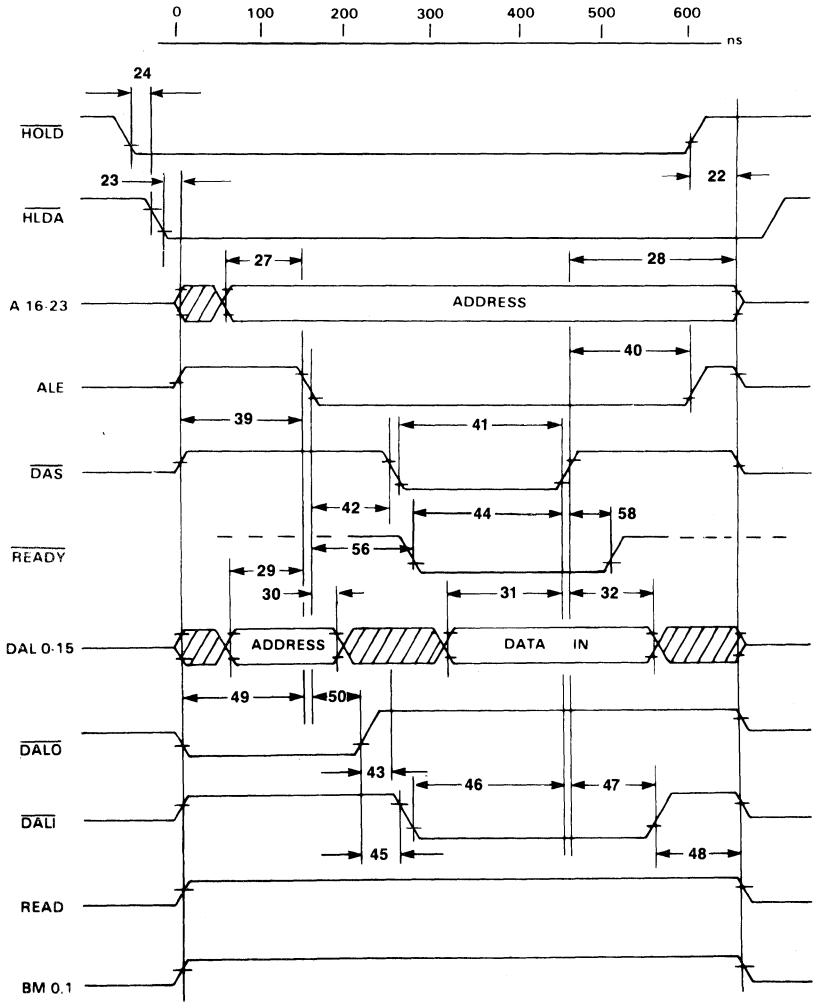
Figure 5. Output Load Diagram



TIMING MEASUREMENTS ARE MADE AT THE FOLLOWING VOLTAGES, UNLESS OTHERWISE SPECIFIED:

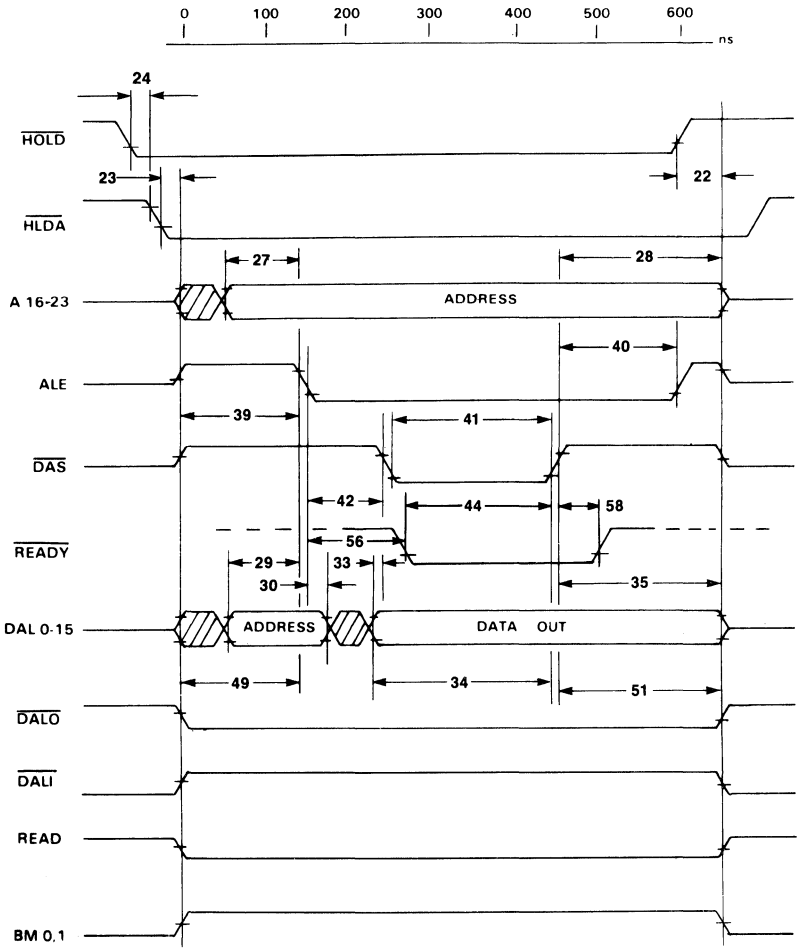
	"1"	"0"
OUTPUT	2.0 V	0.8 V
INPUT	2.0 V	0.8 V
FLOAT	10% V_{OH}	90% V_{OL}

Figure 6. MK5025 Serial Link Timing Diagram



NOTE: The Bus Master cycle time will increase from a minimum of 600 ns in 100 ns steps until the slave device returns READY.

Figure 7. MK5025 Bus Master Timing Diagram (Read)



NOTE: The Bus Master cycle time will increase from a minimum of 600 ns in 100 ns steps until the slave device returns READY.

Figure 8. MK5025 Bus Master Timing Diagram (Write)

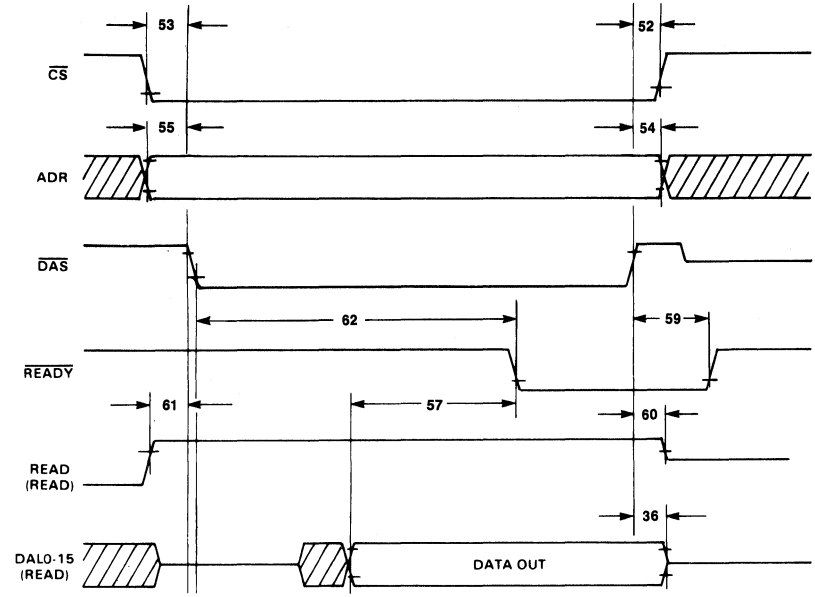


Figure 9. MK5025 Bus Slave Timing Diagram (Read)

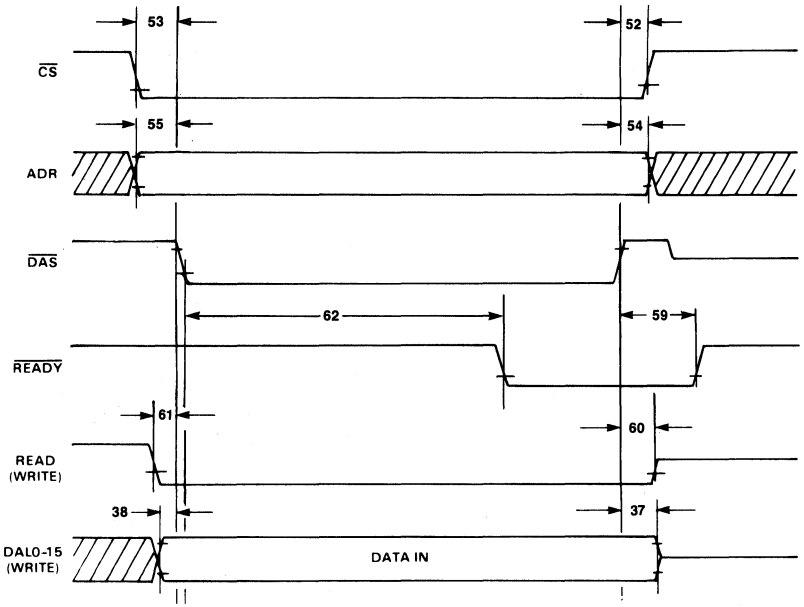


Figure 10. MK5025 Bus Slave Timing Diagram (Write)

SECTION 6
REFERENCE DOCUMENTS

The following documents are applicable to the use of the MK5025.

1. Information processing systems - Open Systems Interconnection - Basic Reference Model, ISO 7498.
2. High-level Data Link Control (HDLC), ISO 3309.
3. Data Communication High-level data link control procedures - Consolidation of elements of procedure, ISO 4335.
4. Advanced Data Communication Control Procedures (ADCCP), ANSI X3.66.
5. CCITT Recommendation X.25.
6. CCITT Recommendation X.32.
7. CCITT Recommendation X.75.
8. Data Communication - Description of the 1984 X.25 LAPB - Compatible DTE Link Procedures, ISO 7776.
9. Minimal User-network Signaling Specification for the ISDN Primary Rate Interface, ANSI T1D1/86-288.

THOMSON COMPONENTS MOSTEK

MK68590 (P,N)

LOCAL AREA NETWORK CONTROLLER FOR ETHERNET

COMMUNICATIONS PRODUCTS

FEATURES

- ☐ 100% compatible with Ethernet and IEEE 802.3 specifications
- ☐ Data packets moved by block transfers over a processor bus (on-board DMA controller 24-bit linear address space)
- ☐ Buffer management
- ☐ Packet framing
- ☐ Preamble and Cyclic Redundancy Check (CRC) insertion
- ☐ Preamble stripping and CRC verification
- ☐ General 16-bit microprocessor bus interface compatible with popular processors (68000, 8086, Z8000, LSI-11)
- ☐ Cable fault detection
- ☐ Multicast logical address filtration
- ☐ Collision handling and retry
- ☐ Scaled N-channel MOS VLSI technology
- ☐ 48-pin DIP
- ☐ Single 5-volt power supply
- ☐ Single phase TTL level clock
- ☐ All inputs and outputs TTL compatible
- ☐ Completely compatible with companion Serial Interface Adapter (SIA) chip MK68591/2.

DESCRIPTION

The MK68590-LANCE™ (Local Area Network Controller for Ethernet) is a 48-pin VLSI device that simplifies the interfacing of a microcomputer or a minicomputer to an Ethernet Local Area Network. This chip operates in a local environment that includes a closely coupled memory and microprocessor. The LANCE uses scaled N-channel MOS technology and is compatible with several microprocessors.

LANCE is a trademark of Thomson Components - Mostek Corporation.

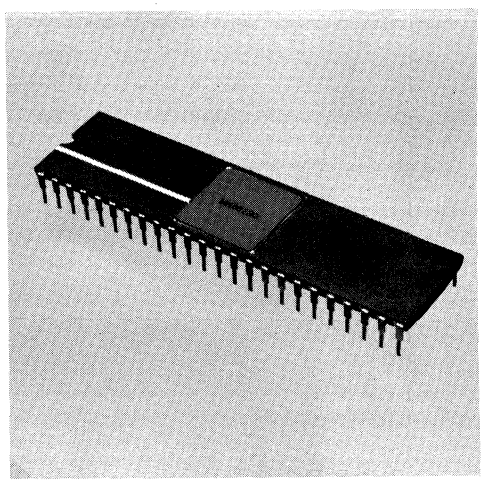


Figure 1. MK68590

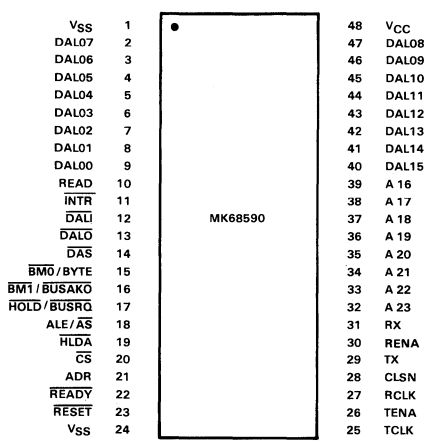


Figure 2. LANCE Pin Assignment

PIN DESCRIPTION

DAL00-DAL15
(Data/Address Bus)
Input/Output Three State. The time multiplexed Address/Data bus. These lines will be driven as a bus master and as a bus slave.

READ
Input/Output Three State. Indicates the type of operation to be performed in the current bus cycle. When it is a bus master, LANCE drives this signal.

LANCE as bus slave:
High - The chip places data on the DAL lines.
Low - The chip takes data off the DAL lines.
LANCE as bus master:
High - The chip takes data off the DAL lines.
Low - The chip places data on the DAL lines.

$\overline{\text{INTR}}$
(Interrupt)
Output Open Drain. When enabled, an attention signal that indicates the occurrence of one or more of the following events: a message reception or transmission has completed or an error has occurred during the transaction; the initialization procedure has completed; or a memory error has been encountered. Setting INEA in CSR0 (bit 06) enables $\overline{\text{INTR}}$.

$\overline{\text{DALI}}$
(Data/Address Line In)
Output Three State. An external bus transceiver control line. When LANCE is a bus master and reads from the DAL lines, $\overline{\text{DALI}}$ is asserted during the data portion of the transfer.

$\overline{\text{DALO}}$
(Data/Address Line Out)
Output Three State. An external bus transceiver control line. When LANCE is a bus master and drives the DAL lines, $\overline{\text{DALO}}$ is asserted during the address portion of a read transfer or for the duration of a write transfer.

$\overline{\text{DAS}}$
(Data/Strobe)
Input/Output Three State. Defines the data portion of the bus transaction. DAS is driven only as a bus master.

$\overline{\text{BM0}}$, $\overline{\text{BM1}}$ or BYTE, $\overline{\text{BUSAKO}}$
(Byte Mask)
Output Three State. Pins 15 and 16 are programmable through bit (00) of CSR3 (known as BCON). Asserting $\overline{\text{RESET}}$ clears CSR3.

f BCON = 0
PIN 16 = $\overline{\text{BM1}}$ (Output Three State)
PIN 15 = $\overline{\text{BM0}}$ (Output Three State)

BM0, BM1 Byte Mask. Indicates the byte(s) of a bus transaction to be read or written. The BM lines are ignored as a bus slave and assume word transfers only. The LANCE drives the BM lines only when it is a bus master. Byte selection occurs as follows:

$\overline{\text{BM1}}$	$\overline{\text{BM0}}$	
Low	Low	Whole Word
Low	High	Byte of DAL 08 - DAL 15
High	Low	Byte of DAL 00 - DAL 07
High	High	None

If BCON = 1
PIN 16 = $\overline{\text{BUSAKO}}$ (Output)
PIN 15 = BYTE (Output Three State)

BYTE. An alternate byte selection line. Byte selection occurs when the BYTE and DAL (00) lines are latched during the address portion of the bus transaction. BYTE, $\overline{\text{BM0}}$ and $\overline{\text{BM1}}$ are ignored when LANCE is a bus slave. There are two modes of ordering bytes depending on bit (02) of CSR3, (known as BSWP). This programmable ordering of upper and lower bytes when using BYTE and DAL (00) as selection signals is required to make the ordering compatible with various 16-bit microprocessors.

BSWP = 0		BSWP = 1		
BYTE	DAL(00)	BYTE	DAL(00)	
Low	Low	Low	Low	Whole Word
Low	High	Low	High	Illegal Condition
High	High	High	Low	Upper Byte
High	Low	High	High	Lower Byte

$\overline{\text{BUSAKO}}$. The DMA daisy chain output.

$\overline{\text{HOLD}}$/$\overline{\text{BUSRQ}}$
(Bus Hold Request)
Input/Output Open Drain. LANCE asserts this signal when it requires access to memory. $\overline{\text{HOLD}}$ is held low for the entire bus transaction. This bit is programmable through bit (00) of CSR3 (known as BCON). In the daisy chain DMA mode (BCON = 1) $\overline{\text{BUSRQ}}$ is asserted only if $\overline{\text{BUSRQ}}$ is inactive prior to assertion. Bit (00) of CSR3 is cleared when $\overline{\text{RESET}}$ is asserted.

CSR3(00) BCON = 0
PIN 17 = $\overline{\text{HOLD}}$ (Output Open Drain)
CSR3(00) BCON = 1
PIN 17 = $\overline{\text{BUSRQ}}$ (Output Open Drain)
$\overline{\text{BUSRQ}}$ will be asserted only if PIN 17 is high prior to assertion.

ALE/$\overline{\text{AS}}$
(Address Latch Enable)
Output Three State. Used to demultiplex the DAL lines and define the address portion of the bus cycle. This

pin is programmable through bit (01) of CSR3. As ALE, the signal transitions from high to low at the end of the address portion of the bus the address portion of the bus transaction and remains low during the entire data portion of the transaction. As $\overline{AS}$, the signal transitions from low to high at the end of the address portion of the bus transaction and remains high throughout the entire data portion of the transaction. The LANCE drives the ALE/$\overline{AS}$ line only as a bus master.

CSR3(01) ACON = 0
PIN 18 = ALE
CSR3(01) ACON = 1
PIN 18 = $\overline{AS}$

$\overline{HLDA}$
(Bus Hold Acknowledge)
Input. A response to $\overline{HOLD}$ indicating that the LANCE is the Bus Master. $\overline{HLDA}$ stops its response when $\overline{HOLD}$ ends its assertion.

$\overline{CS}$
(Chip Select)
Input. When asserted, $\overline{CS}$ indicates LANCE is the slave device of the data transfer. $\overline{CS}$ must be valid throughout the data portion of the bus cycle.

ADR
(Register Address Port Select)
Input. When $\overline{CS}$ is asserted, ADR indicates which of the two register ports is selected. ADR must be valid throughout the data portion of the bus cycle.

ADR	PORT
Low	Register Data Port
High	Register Address Port

$\overline{READY}$
Input/Output Open Drain. When the LANCE is a bus master, $\overline{READY}$ is an asynchronous acknowledgement from external memory that will complete the data transfer. As a bus slave, the chip asserts $\overline{READY}$ when it has put data on the bus, or is about to take data off the bus. $\overline{READY}$ is a response to $\overline{DAS}$. $\overline{READY}$ negates after $\overline{DAS}$ negates. Note: If $\overline{DAS}$ or $\overline{CS}$ deassert prior to the assertion of $\overline{READY}$, $\overline{READY}$ cannot assert.

$\overline{RESET}$
Input. Bus reset signal. Causes LANCE to cease operation and to enter an idle state.

TLCK
(Transmit Clock)
Input. Normally a free-running 10 MHz clock (crystal-controlled within 0.01% accuracy).

TENA
(Transmit Enable)
Output. Transmit Output Stream Enable. A level asserted with the transmit output bit stream, TX, to enable the external transmit logic.

RCLK
(Receive Clock)
Input. Normally a 10 MHz square wave synchronized to the receive data and present only while receiving an input bit stream.

CLSN
(Collision)
Input. A logical input that indicates that a collision is occurring on the channel.

TX
(Transmit)
Output. Transmit output bit stream.

RENA
(Receive Enable)
Input. A logical input that indicates the presence of data on the channel.

RX
(Receive)
Input. Receive input bit stream.

A16-A23
(High-Order Address Bus)
Output Three State. The additional address bits necessary to extend the DAL lines to produce a 24-bit address. These lines will be driven only as a bus master.

VCC
Power supply pin. +5 VDC ±5 percent. It is recommended that a power supply filter be used between V_{CC} (Pin 48) and V_{SS} (Pins 1 and 24). This filter should consist of two capacitors in parallel having the values of 10 μF and .047 μF respectively.

VSS
Ground. 0 VDC.

FUNCTIONAL CAPABILITIES

The LANCE interfaces to a microprocessor bus characterized by time-multiplexed address and data lines. Typically, data transfers are 16 bits wide but byte transfers occur if the buffer memory address boundaries are odd. The address bus is 24 bits wide.

The Ethernet packet format consists of 64-bit preamble, a 48-bit destination address, a 48-bit source address, a 16-bit type field, and from a 46 to 1500 byte data field terminated with a 32-bit CRC. The packets' variable widths accommodate both short-status command and terminal traffic packets and long data packets to printers and disks (1024-byte disk sectors, for example). Packets are spaced a minimum of 9.6 μsec apart to allow one node enough time to receive back-to-back packets.

The LANCE operates in a minimal configuration that requires close coupling between local memory and a processor. The local memory provides packet buffering for the chip and serves as a communication link between chip and processor. During initialization, the control processor loads the starting address of the initialization block plus the operating mode of the chip via two ports that can access four control registers into LANCE. The host processor talks directly to LANCE only during this initial phase. All further communications are handled via a Direct Memory Access (DMA) machine under microword control contained within LANCE. Figure 3 shows a block diagram of the LANCE and SIA device used to create an Ethernet interface for a computer system.

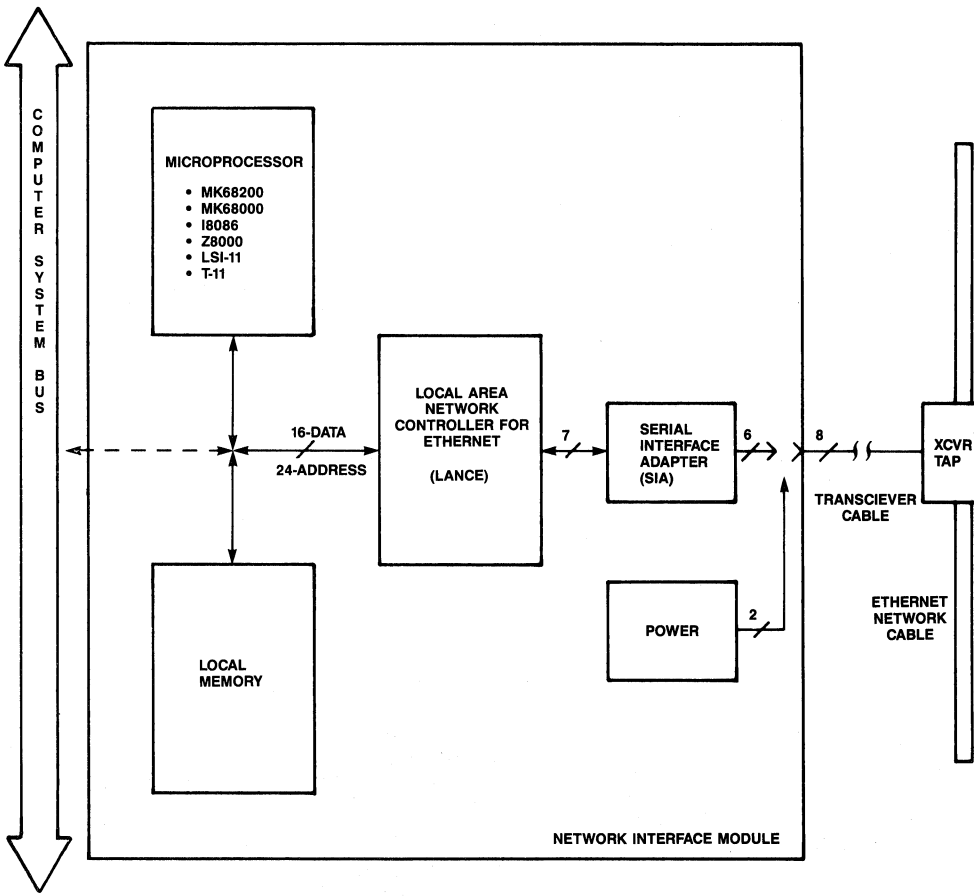


Figure 3. Ethernet Local Area Network System Block Diagram

FUNCTIONAL DESCRIPTION

SERIAL DATA HANDLING

LANCE provides the Ethernet interface as follows. In the transmit mode (since there is only one transmission path, Ethernet is a half duplex system), the LANCE reads data from a transmit buffer by using DMA and appends the preamble, sync pattern (two ones after alternating ones and zeros in the preamble), and calculates and appends the complement of the 32-bit CRC. In the receive mode, the destination address, source address, type, data, and CRC fields are transferred to memory via DMA cycles. The CRC is calculated as data and transmitted CRC is received. At the end of the packet, if this calculated CRC does not agree with a constant, an error bit is set in RDM1 of the receiver descriptor ring. In the receive mode, LANCE accepts packets under four modes of operation. The first mode is a full comparison of the 48-bit destination address in the packet with the node address that was programmed into the LANCE during an initialization cycle. There are two types of logical addresses. One is a group type mask where the 48-bit address in the packet is put through a hash filter in order to map the 48-bit physical addresses into 1 of 64 logical groups. This mode can be useful if simultaneously sending packets to all of one type of a device on the network. (i.e., send a packet to all file servers or all printer servers). The second logical address is a multicast address where all nodes on the network receive the packet. The last receive mode of operation is the so called "promiscuous mode" in which a node will accept all packets on the cable regardless of their destination address.

COLLISION DETECTION AND IMPLEMENTATION

The Ethernet CSMA/CD network access algorithm is implemented completely within LANCE. In addition to listening for a clear network cable before transmitting, Ethernet handles collisions in a predetermined way. Should two transmitters attempt to seize the network cable at the same time, they will collide, and the data on the network cable will be garbled. LANCE is constantly monitoring the Collision (CLSN) pin. This signal is generated by the transceiver when the signal level on the network cable indicates the presence of signals from two or more transmitters. If LANCE is transmitting when CLSN is asserted, it will continue to transmit the preamble (collisions normally occur while the preamble is being transmitted), then will "jam" the network for 32 bit times (3.2 microseconds). This jamming ensures that all nodes have enough time to detect the collision. The transmitting nodes then delay a random amount of time according to the "truncated binary backoff" algorithm defined in the Ethernet specification to minimize the probability of the colliding nodes having multiple collisions with each other. After 16 abortive attempts to transmit a packet, LANCE will report a RTRY error due to excessive collisions and step over the transmitter buffer. During reception, the detection of a collision causes that reception to be aborted. Depending on when the collision occurred, LANCE will treat this packet as an error packet if the packet has an address mismatch, as a runt packet (a packet that has less than 64 bytes), or as a legal length packet with a CRC error.

Fatal error reporting is provided by LANCE through a microprocessor interrupt and error flags in CSR0. These Fatal Error conditions are the following:

1.) Collision Error - The failure of the transceiver to send a collision message or, heartbeat at the conclusion of a normal transmission.

2.) Transmitter on longer than 1518 bytes.

3.) Missed Packet - LANCE failed to receiver transmitted packet.

4.) Memory Error - Failure of a memory transaction to complete within 25.6 μS.

Additional errors are reported through bits in the descriptor rings (on a buffer by buffer basis). Receive error conditions include framing, CRC and buffer errors, and overflow. Transmit descriptor rings have error bits indicating buffer, underflow, late collision, and loss of carrier. Additionally, transmit descriptor rings have a bit indicating that the transmitter has unsuccessfully tried to transmit over a busy communication link.

Transmit descriptor rings also have ten bits reserved for a Time Domain Reflectometry counter (TDR). On the occurrance of a collision, the value in the TDR will give the number of system clocks until the collision, which can be used to determine the distance to the fault.

BUFFER MANAGEMENT

A key feature of the LANCE and its DMA channel is the flexibility and speed of communication between the LANCE and the host microprocessor through common memory locations. The basic organization of the buffer management is a circular queue of tasks in memory called descriptor rings, as shown in Figure 4. These rings control both transmit and receive operations. Up to 128 tasks may be queued on a descriptor ring for execution by the LANCE. Each entry in a descriptor ring holds a pointer to a data memory buffer and an entry for the data buffer length. Data buffers can be chained or cascaded to handle a long packet in multiple data buffer areas. The LANCE searches the descriptor rings to determine the next empty buffer. This enables it to chain buffers together or to handle back-to-back packets. As each buffer is filled, an "own" bit is reset, signaling the host processor to empty this buffer.

MICROPROCESSOR INTERFACE

The parallel interface of LANCE has been designed to be "friendly", or easy to interface, to many popular 16-bit microprocessors. These microprocessors include the MK68000, Z8000, 8086, LSI-11, T-11, and MK68200 (the MK68200 is a 16-bit single chip microcomputer produced by Mostek, the architecture of which is modeled after the MK68000). LANCE has a wide 24-bit linear address space when in the Buster Master Mode, allowing it to DMA the entire address space of the above microprocessors. LANCE uses no segmentation or paging methods. As such, LANCE addressing is closest to MK68000 addressing, but is compatible with the other microprocessors. When LANCE is a bus master, a programmable mode of operation allows byte addressing, either by employing a Byte/Word control signal (much like that used on the 8086 or the Z8000) or by using an Upper Data Strobe/Lower Data Strobe much like that used on the MK68000, LSI-11 and MK68200 microprocessors. A programmable polarity on the Address Strobe signal eliminates the need for external logic. LANCE interfaces with multiplexed and demultiplexed data busses and features control signals for address/data bus transceivers.

After the initialization routine, packet reception or transmission, transmitter timeout error, a missed packet, or memory error, LANCE generates an interrupt to the host microprocessor.

The cause of the interrupt is ascertained by reading CSR0. Bit (06) of CSR0, INEA, enables or disables interrupts to the microprocessor. In a polling mode, BIT (07) of CSR0 is sampled to determine when an interrupt causing condition occurred.

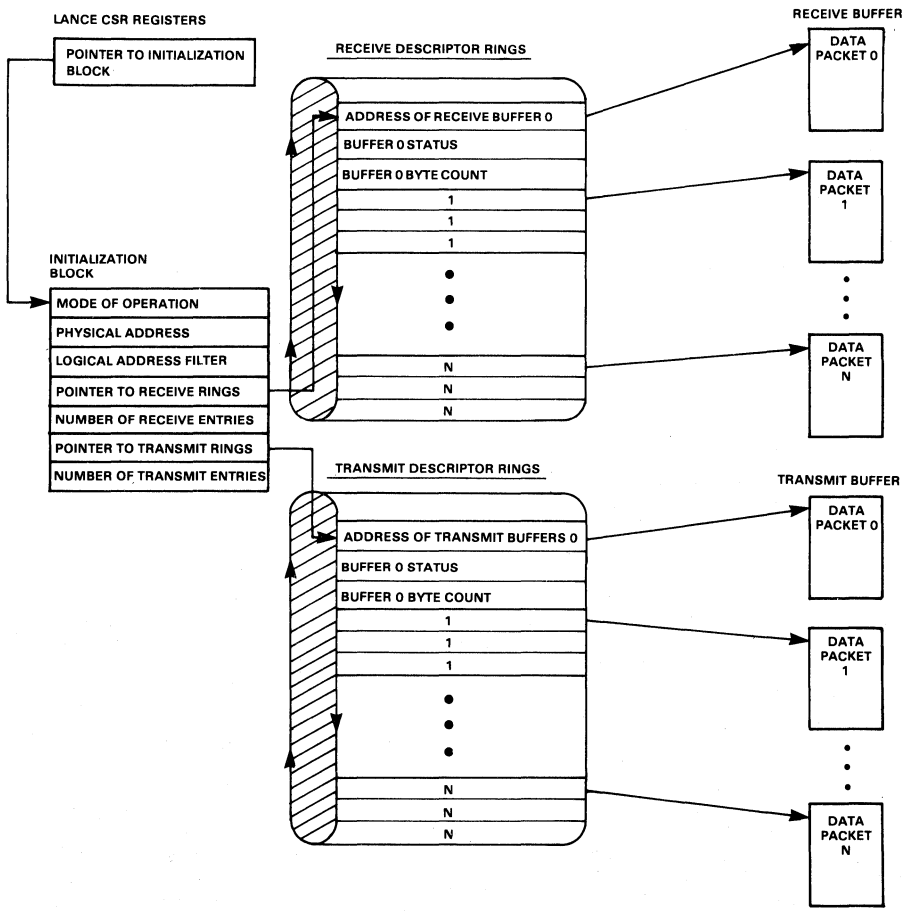


Figure 4. LANCE Memory Management

LANCE INTERFACE DESCRIPTION

ALE, $\overline{DAS}$ and $\overline{READY}$ time all data transfers from the LANCE in the Bus Master mode. The automatic adjustment of the LANCE cycle by the $\overline{READY}$ signal allows synchronization with variable cycle time memory due either to memory refresh or to dual port access. Bus cycles are a minimum of 600 ns long and can be increased in 100 ns increments.

READ SEQUENCE

At the beginning of a read cycle, valid addresses are placed on DAL00-DAL15 and A16-A21. The BYTE Mask signals ($\overline{BM0}$ and $\overline{BM1}$) become valid at the beginning of this cycle as does READ, indicating the type of cycle. The trailing edge of ALE or $\overline{AS}$ strobes the addresses A0-A15 into the external latches. Approximately 100 ns later, DAL00-DAL15 go into a three state mode. There is a 50 ns delay to allow for transceiver turnaround, then DAS falls low to signal the beginning of the data portion of the cycle. At this point in the cycle, the LANCE stalls waiting for the memory device to assert $\overline{READY}$. Upon assertion of $\overline{READY}$, $\overline{DAS}$ makes a transition from a zero to a one, latching memory data. ($\overline{DAS}$ is low for a minimum of 200 ns).

The bus transceiver controls, $\overline{DALI}$ and $\overline{DALO}$, control the bus transceivers. DALI signals to strobe data toward the LANCE and DALO signals to strobe data or addresses away from the LANCE. During a read cycle, $\overline{DALO}$ goes inactive before $\overline{DALI}$ goes active to avoid "spiking" of bus transceivers.

WRITE SEQUENCE

The write cycle begins exactly like a read cycle with the READ line remaining inactive. After ALE or $\overline{AS}$ pulse, the DAL00-DAL15 change from addresses to data. $\overline{DAS}$ goes active when the DAL00-DAL15 are stable. This data remains valid on the bus until the memory device asserts $\overline{READY}$. At this point, $\overline{DAS}$ goes inactive, latching data into the memory device. Data is held for 75 ns after the negation of $\overline{DAS}$.

LANCE INTERFACE DESCRIPTION — BUS SLAVE MODE

The LANCE enters the Bus Slave Mode whenever $\overline{CS}$ becomes active. This mode must be entered whenever writing or reading the four status control registers (CSR0, CSR1, CSR2, and CSR3) and the register address pointer (RAP). RAP and CSR0 may be read or written to at any time, but the LANCE must be stopped (CSR0 bit 02) when CSR1, CSR2, or CSR3 is to be written to or read.

MK68590 ELECTRICAL SPECIFICATION

ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias ..... −25°C to +125°C
Storage Temperature ..... −65°C to +150°C
Voltage on Any Pin with Respect to Ground ..... −0.3 V to +7 V
Power Dissipation ..... 2.0 W

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

T_A=0°C to 70°C, V_{CC} = +5 V ±5 percent unless otherwise specified.

SYMBOL	PARAMETER	MIN	MAX	UNITS
V_{IL}		−0.5	+0.8	V
V_{IH}		+2.0	V_{CC} +0.5	V
V_{OL}	@ I_{OL} = 3.2 mA		+0.5	V
V_{OH}	@ I_{OH} = −0.4 mA	+2.4		V
I_{IL}	@ V_{in} = 0.4 to V_{CC}		±10	μA

CAPACITANCE

F=1 MHz

SYMBOL	PARAMETER	MIN	MAX	UNITS
C_{IN}			10	pf
C_{OUT}			10	pf
C_{IO}			20	pf

AC TIMING SPECIFICATIONS

T_A = 0°C to 70°C, V_{CC} = +5 V ±5 percent, unless otherwise specified.

NO.	SIGNAL	SYMBOL	PARAMETER	TEST CONDITIONS	MIN (ns)	TYP (ns)	MAX (ns)
1	TCLK	T_{TCT}	TCLK period		99		101
2	TCLK	T_{TCL}	TCLK low time		45		55
3	TCLK	T_{TCH}	TCLK high time		45		55
4	TCLK	T_{TCR}	Rise time of TCLK		0		8
5	TCLK	T_{TCF}	Fall time of TCLK		0		8
6	TENA	T_{TEP}	TENA propagation delay after the rising edge of TCLK	CL = 50 pf			75
7	TENA	T_{TEH}	TENA hold time after the rising edge of TCLK	CL = 50 pf	5		

AC TIMING SPECIFICATIONS (Continued)

T_A = 0°C to 70°C, V_{CC} = +5 V ±5 percent, unless otherwise specified.

NO.	SIGNAL	SYMBOL	PARAMETER	TEST CONDITIONS	MIN (ns)	TYP (ns)	MAX (ns)
8	TX	T_{TDP}	TX data propagation delay after the rising edge of TCLK	CL=50 pf			75
9	TX	T_{TDH}	TX data hold time after the rising edge of TCLK	CL=50 pf	5		
10	RCLK	T_{RCT}	RCLK period		85		118
11	RCLK	T_{RCH}	RCLK high time		38		
12	RCLK	T_{RCL}	RCLK low time		38		
13	RCLK	T_{RCR}	Rise time of RCLK		0		8
14	RCLK	T_{RCF}	Fall time of RCLK		0		8
15	RX	T_{RDR}	RX data rise time		0		8
16	RX	T_{RDF}	RX data fall time		0		8
17	RX	T_{RDH}	RX data hold time (RCLK to RX data change)		5		
18	RX	T_{RDS} (See Note)	RX data setup time (RX data stable to the rising edge of RCLK)		See Note		
19	RENA	T_{DPL}	RENA low time		120		
20	RENA	T_{RENH}	RENA hold time after rising edge of RCLR		40		
21	CLSN	T_{CPH}	CLSN high time		80		
22	A/DAL	T_{DOFF}	Bus master driver disable after rising edge of $\overline{HOLD}$		0		50
23	A/DAL	T_{DON}	Bus master driver enable after falling edge of $\overline{HLDA}$		0		150
24	$\overline{HLDA}$	T_{HHA}	Delay to falling edge of $\overline{HLDA}$ from falling edge of $\overline{HOLD}$ (bus master)		0		
25	$\overline{RESET}$	T_{RW}	$\overline{RESET}$ pulse width low		200		
26	A/DAL	T_{CYCLE}	Read/write, address/data cycle time		600		
27	A	T_{XAS}	Address setup time to the falling edge of ALE		75		
28	A	T_{XAH}	Address hold time after the rising edge of $\overline{DAS}$		35		
29	DAL	T_{AS}	Address setup time to the falling edge of ALE		75		
30	DAL	T_{AH}	Address hold time after the falling edge of ALE		35		
31	DAL	T_{RDAS}	Data setup time to the rising edge of $\overline{DAS}$ (bus master read)		50		

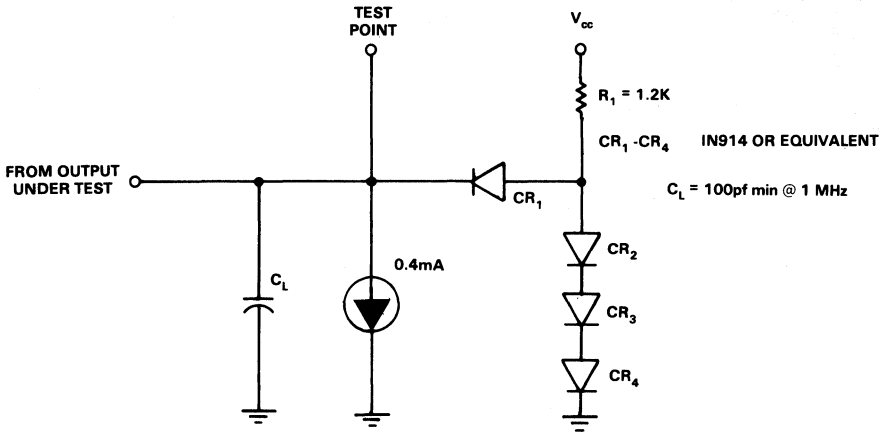
NOTE: $T_{RDS\ (min)} = T_{RCT} - 25$ ns. Therefore, T_{RCT} = 100 ns when $T_{RDS\ (min)}$ = 75 ns.

AC TIMING SPECIFICATIONS (Continued)
T_A = 0°C to 70°C, V_{CC} = +5 V ±5 percent, unless otherwise specified.

NO.	SIGNAL	SYMBOL	PARAMETER	TEST CONDITIONS	MIN (ns)	TYP (ns)	MAX (ns)
32	DAL	T_{RDAH}	Data hold time after the rising edge of $\overline{DAS}$ (bus master read)		0		
33	DAL	T_{DDAS}	Data setup time to the falling edge of $\overline{DAS}$ (bus master write)		0		
34	DAL	T_{WDS}	Data setup time to the rising edge of $\overline{DAS}$ (bus master write)		200		
35	DAL	T_{WDH}	Data hold time after the rising edge of $\overline{DAS}$ (bus master write)		35		
36	DAL	T_{SDO1}	Data driver delay after the falling edge of $\overline{DAS}$ (bus slave read)	(CSR 0,3, RAP)		400	
37	DAL	T_{SDO2}	Data driver delay after the falling edge of $\overline{DAS}$ (bus slave read)	(CSR 1,2)		1200	
38	DAL	T_{SRDH}	Data hold time after the rising edge of $\overline{DAS}$ (bus slave read)		0		35
39	DAL	T_{SWDH}	Data hold time after the rising edge of $\overline{DAS}$ (bus slave write)		0		
40	DAL	T_{SWDS}	Data setup time to the falling edge of $\overline{DAS}$ (bus slave write)		0		
41	ALE	T_{ALEW}	ALE width high		120		150
42	ALE	T_{DALE}	Delay from rising edge of $\overline{DAS}$ to the rising edge of ALE		70		
43	$\overline{DAS}$	T_{DSW}	$\overline{DAS}$ width low		200		
44	$\overline{DAS}$	T_{ADAS}	Delay from the falling edge of ALE to the falling edge of $\overline{DAS}$		80		130
45	$\overline{DAS}$	T_{RIDF}	Delay from the rising edge of $\overline{DALO}$ to the falling edge of $\overline{DAS}$ (bus master read)		15		
46	$\overline{DAS}$	T_{RDYS}	Delay from the falling edge of $\overline{READY}$ to the rising edge of $\overline{DAS}$	Taryd= 300 ns	75		250
47	$\overline{DALI}$	T_{ROIF}	Delay from the rising edge of $\overline{DALO}$ to the falling edge of $\overline{DALI}$ (bus master read)		15		
48	$\overline{DALI}$	T_{RIS}	$\overline{DALI}$ setup time to the rising edge of $\overline{DAS}$ (bus master read)		135		
49	$\overline{DALI}$	T_{RIH}	$\overline{DALI}$ hold time after the rising edge of $\overline{DAS}$ (bus master read)		0		
50	$\overline{DALI}$	T_{RIOF}	Delay from the rising edge of $\overline{DALI}$ to the falling edge of $\overline{DALO}$ (bus master read)		55		
51	$\overline{DALO}$	T_{OS}	$\overline{DALO}$ setup time to the falling edge of ALE (bus master read)		110		
52	$\overline{DALO}$	T_{ROH}	$\overline{DALO}$ hold time after the falling edge of ALE (bus master read)		35		
53	$\overline{DALO}$	T_{WDSI}	Delay from the rising edge of $\overline{DAS}$ to the rising edge of $\overline{DALO}$ (bus master write)		35		

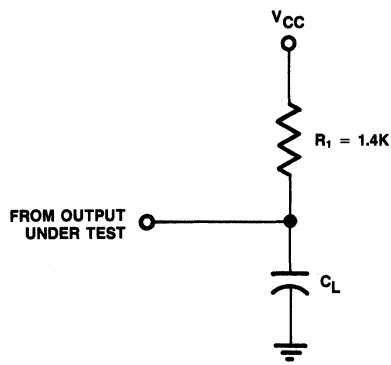
AC TIMING SPECIFICATIONS (Continued)
T_A = 0°C to 70°C, V_{CC} = +5 V ±5 percent, unless otherwise specified.

NO.	SIGNAL	SYMBOL	PARAMETER	TEST CONDITIONS	MIN (ns)	TYP (ns)	MAX (ns)
54	$\overline{CS}$	T_{CSH}	$\overline{CS}$ hold time after the rising edge of $\overline{DAS}$ (Bus slave)		0		
55	$\overline{CS}$	T_{CSS}	$\overline{CS}$ setup time to the falling edge of $\overline{DAS}$ (Bus slave)		0		
56	ADR	T_{SAH}	ADR hold time after the rising edge of $\overline{DAS}$ (Bus slave)		0		
57	ADR	T_{SAS}	ADR setup time to the falling edge of $\overline{DAS}$ (Bus slave)		0		
58	$\overline{READY}$	T_{ARYD}	Delay from the falling edge of ALE to the falling edge of $\overline{READY}$ to insure a minimum bus cycle time (600 ns)				80
59	$\overline{READY}$	T_{SRDS}	Data setup time to the falling edge of $\overline{READY}$ (Bus slave read)		75		
60	$\overline{READY}$	T_{RDYH}	$\overline{READY}$ hold time after the rising edge of $\overline{DAS}$ (Bus master)		0		
61	$\overline{READY}$	T_{SRO1}	$\overline{READY}$ driver turn on after the falling edge of $\overline{DAS}$ (Bus slave)	(CSR 0,3, RAP)		600	
62	$\overline{READY}$	T_{SRO2}	$\overline{READY}$ driver turn on after the falling edge of $\overline{DAS}$ (Bus slave)	(CSR 1,2)		1400	
63	$\overline{READY}$	T_{SRYH}	$\overline{READY}$ hold time after the rising edge of $\overline{DAS}$ (Bus slave)		0		35
64	READ	T_{SRH}	READ hold time after the rising edge of $\overline{DAS}$ (Bus slave)		0		
65	READ	T_{SRS}	READ setup time to the falling edge of $\overline{DAS}$ (Bus slave)		0		



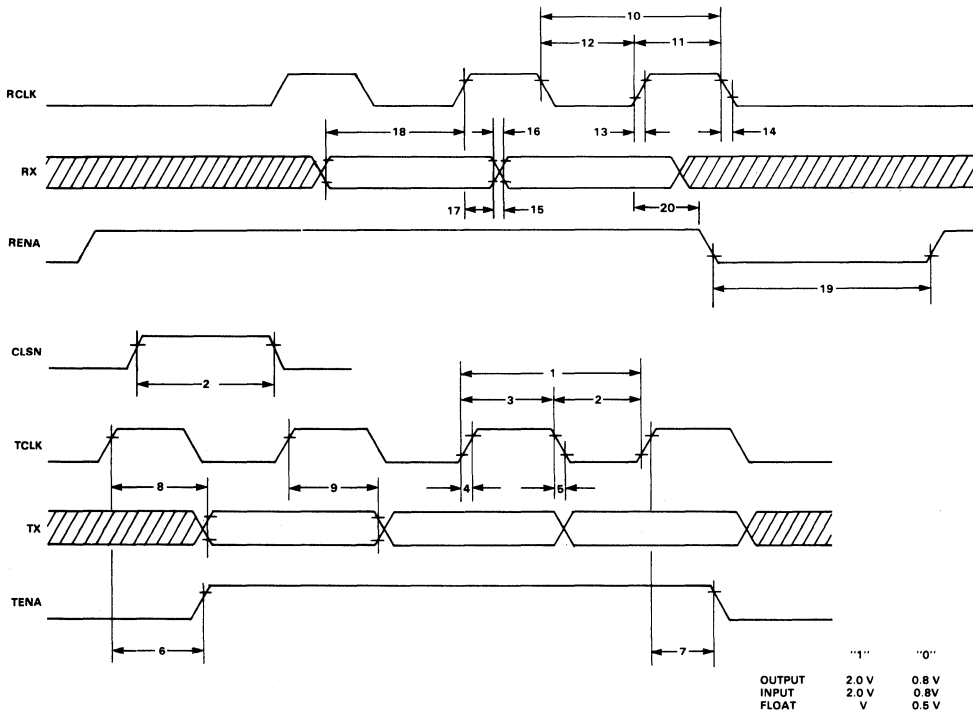
NOTE: This load is used on DAL00 through DAL15, READ, DALI, DALO, DAS, BM0, BM1, ALE/AS, A16 through A23, TENA, and TX.

Figure 5. Output Load Diagram



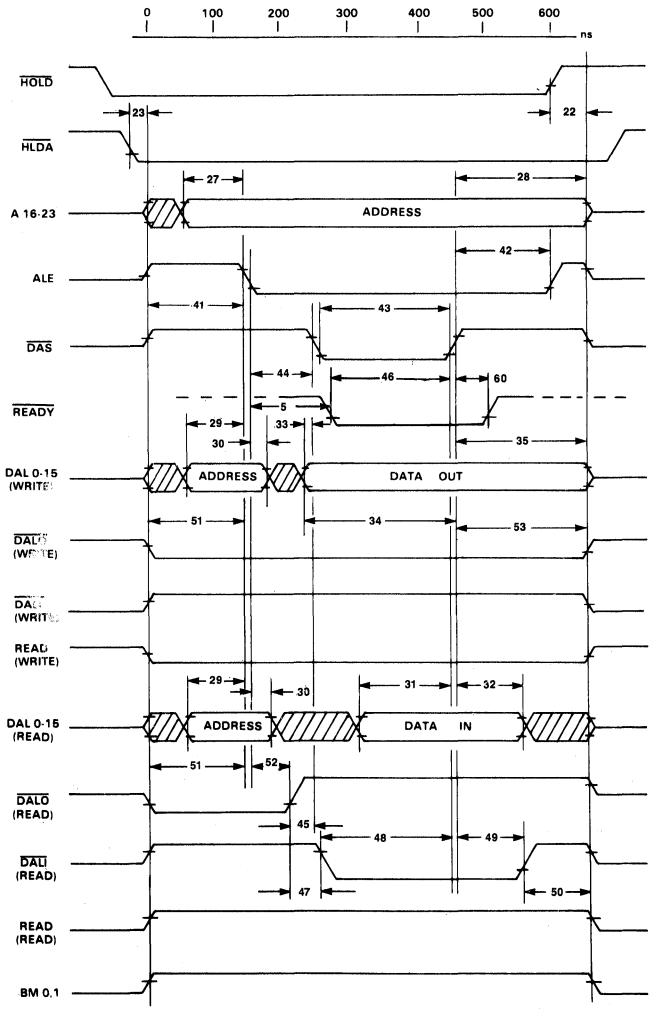
NOTE: This load is used on open drain outputs $\overline{\text{INTR}}$, HOLD/BUSRQ, and $\overline{\text{READY}}$.

Figure 6. Open Drain Output Load Diagram.



NOTE: Timing measurements are made at the following voltages unless otherwise specified.

Figure 7. Serial Link Timing Diagram - SIA Interface Signals



NOTE: The Bus Master cycle time will increase from a minimum of 600 ns in 100 ns steps until the slave device returns $\overline{\text{READY}}$.

Figure 8. LANCE Bus Master Timing Diagram

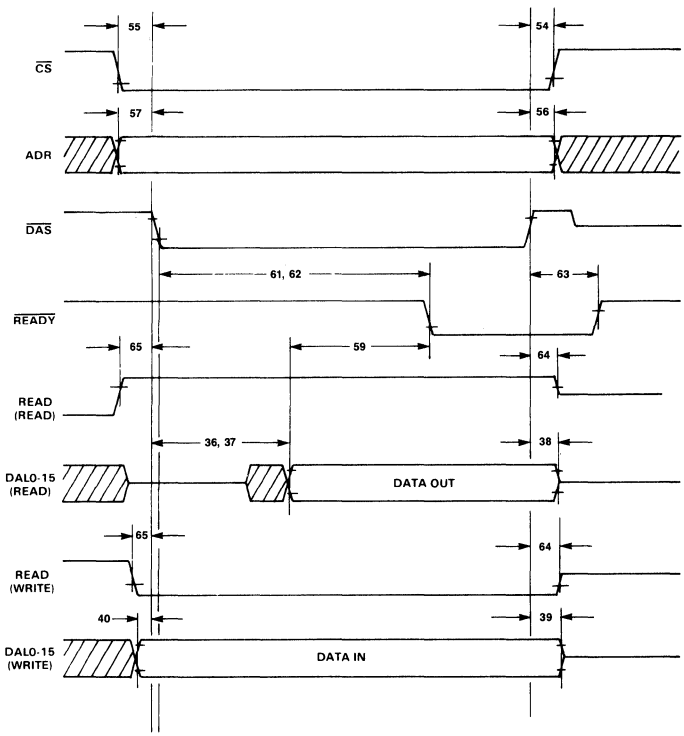


Figure 9. LANCE Bus Slave Timing Diagram

THOMSON
COMPONENTS

MOSTEK

TECHNICAL
MANUAL

MK68590
CONTROLLER FOR ETHERNET LOCAL AREA NETWORK

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CHAPTER 1
GENERAL DESCRIPTION

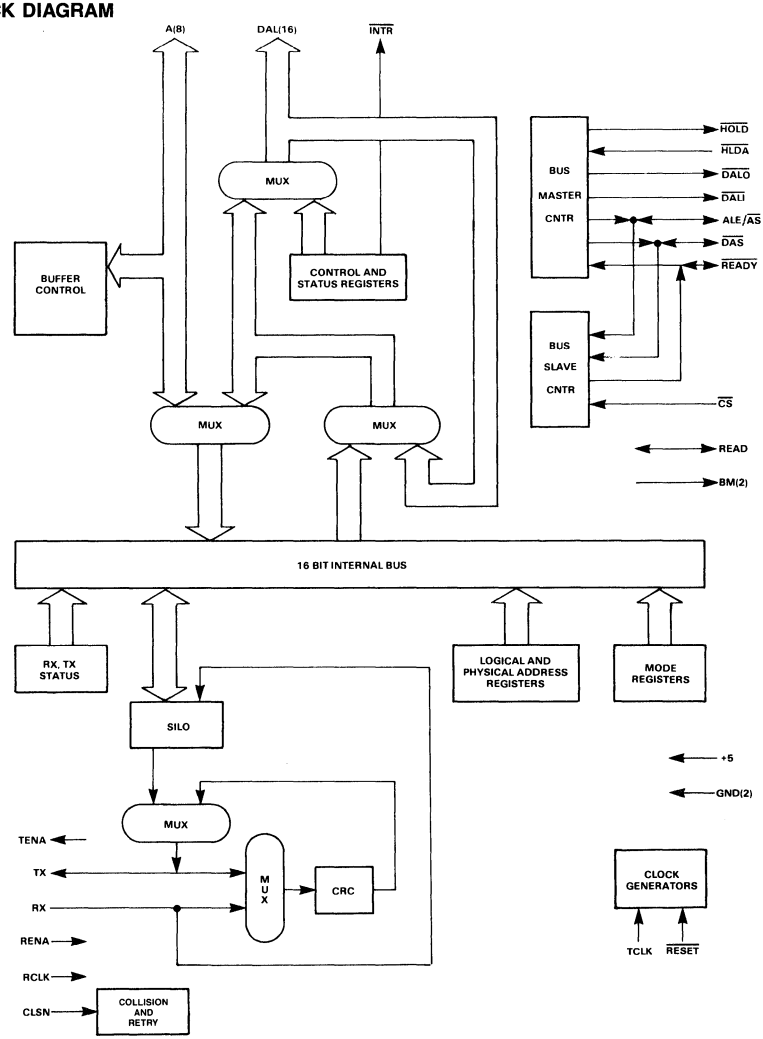
1.0 INTRODUCTION

1.1 OVERVIEW

The MK68590 LANCE (Local Area Network Controller for Ethernet) is a 48-pin VLSI device designed to simplify greatly the interfacing of a microcomputer or a minicomputer to an Ethernet Local Area Network. This chip is intended to operate in a local environment that includes a closely coupled memory and microprocessor. The LANCE uses scaled N-channel MOS technology and is compatible with several microprocessors. A block diagram of the chip is shown in Figure 1.

LANCE is a trademark of Mostek Corporation.

LANCE BLOCK DIAGRAM
Figure 1

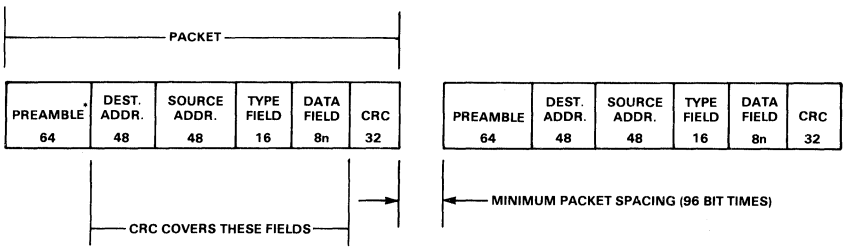


1.2 FUNCTIONAL CAPABILITIES

The Local Area Network Controller for Ethernet (LANCE) interfaces to a microprocessor bus characterized by time multiplexed address and data lines. Typically, data transfers are 16 bits wide, but byte transfers occur if the buffer memory address boundaries are odd. The address bus is 24 bits wide.

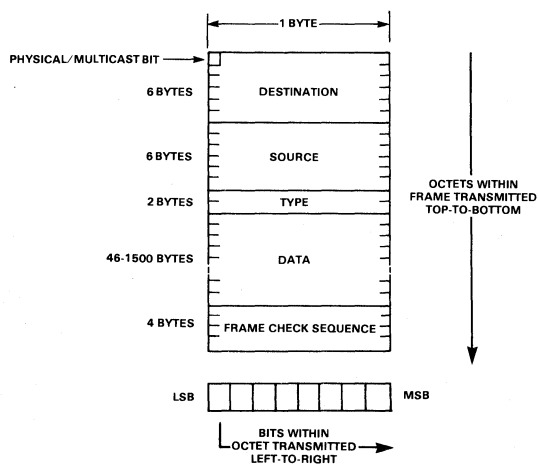
The Ethernet packet format consists of a 64-bit preamble, a 48-bit destination address, a 48-bit source address, a 16-bit type field, and a 46 to 1500 byte data field terminated with a 32-bit CRC as shown in Figure 2 and Figure 3. The variable widths of the packets accommodate both short status, command and terminal traffic packets, and long data packets to printers and disks (1024 byte disk sectors for example). Packets are spaced a minimum of 9.6 μsec apart to allow one node time enough to receive back-to-back packets.

ETHERNET AND LANCE PACKET FORMAT
Figure 2



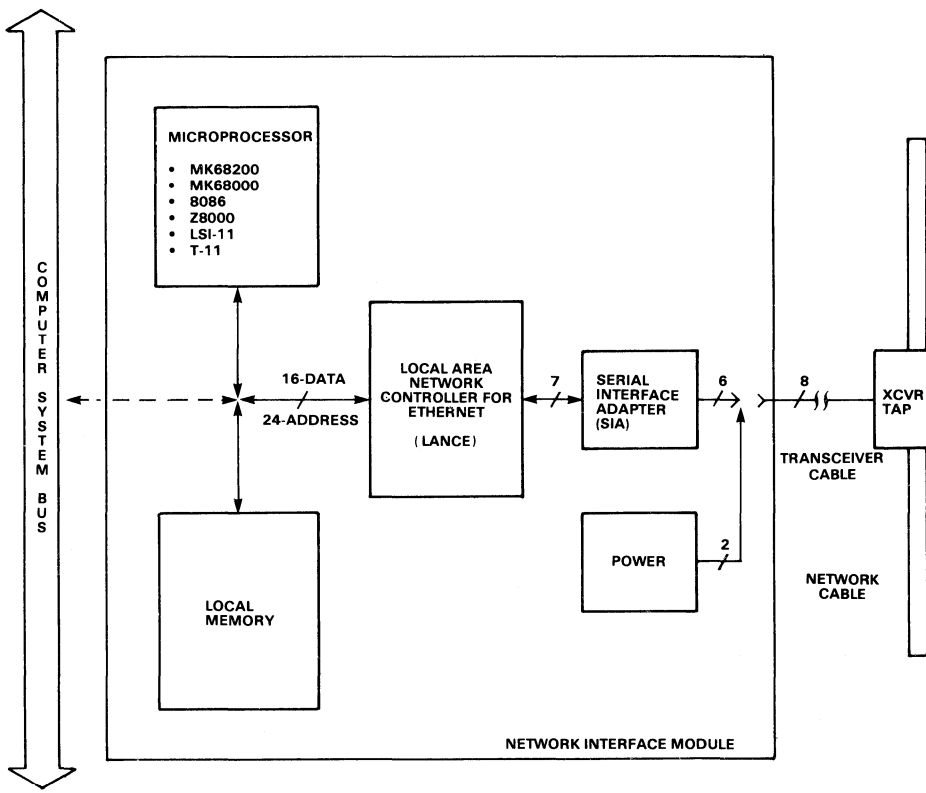
*Last Byte is Start of Frame Synchronization Byte--10101011

ETHERNET AND LANCE PACKET BIT TRANSMISSION SEQUENCE
Figure 3



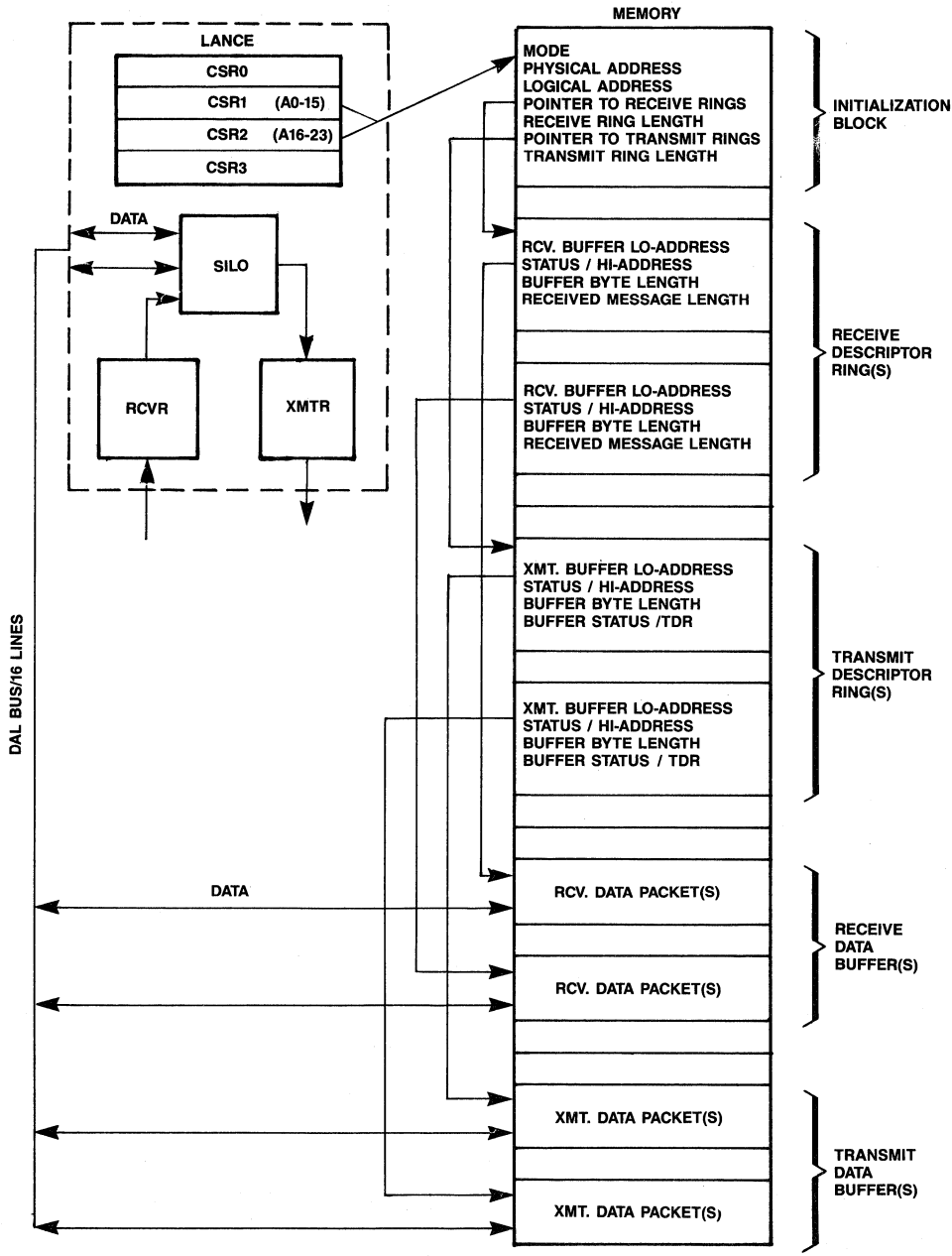
The LANCE is intended to operate in a minimal configuration that requires close coupling between local memory and a processor. Figure 5 shows the relationship between the chip and local memory. The local memory provides packet buffering for the chip and serves as a communication link between the chip and the processor. During initialization, the control processor loads into LANCE the starting address of the initialization block plus the operating mode of the chip via two control registers. It is only during this initial phase that the host processor talks directly to LANCE. All further communications are handled via a DMA machine under microword control contained within the LANCE. Figure 4 is a block diagram of the LANCE and SIA device used to create an Ethernet interface for a computer system.

ETHERNET LOCAL AREA NETWORK SYSTEM BLOCK DIAGRAM
Figure 4



LANCE CONCEPTUAL VIEW

Figure 5



1.3 FUNCTIONAL DESCRIPTION

1.3.1 SERIAL DATA HANDLING

The basic operation of the chip set to provide the Ethernet interface is as follows. In the transmit mode (since there is only one transmission path, Ethernet is a half duplex system), the LANCE reads data from a transmit buffer by using Direct Memory Access (DMA) and appends the preamble, sync pattern (two ones after alternating ones and zeros in the preamble), and calculates and appends the complement of the 32-bit CRC. The first eight words of the transmit buffer must contain the destination address, source address, and type field as detailed in the Ethernet specification. In the receive mode, the destination address, source address, type, data, and CRC fields are transferred to memory via DMA cycles. The CRC is calculated as the data and transmitted CRC are received. At the end of the packet, if this calculated CRC does not agree with a constant, an error bit is set and in RMD1 of the receiver descriptor rings. In the receive mode, packets will be accepted by the LANCE under four modes of operation. The first mode is a full comparison of the 48-bit destination address in the packet with the node address that was programmed into the LANCE during an initialization cycle. There are two types of logical address. One is a group type mask where the 48-bit address in the packet is put through a hash filter in order to map the 48-bit physical addresses into 1 of 64 logical groups. This mode can be useful if sending packets to all of one type of a device simultaneously or the network (i.e. sending a packet to all file servers or all printer servers). The second logical address is the broadcast address where all nodes on the network receive the packet. The last receive mode of operation is the so called "promiscuous mode" in which a node will accept all packets on the network cable regardless of their destination address.

1.3.2 COLLISION DETECTION AND IMPLEMENTATION

The Ethernet CSMA/CD network access algorithm is implemented completely within the LANCE. In addition to listening for a clear network cable before transmitting, Ethernet handles collisions in a predetermined way. Should two transmitters attempt to seize the network cable at the same time, they will collide, and the data on the network cable will be garbled. LANCE is constantly monitoring the CLSN (Collision) pin. This signal is generated by the transceiver when the signal level on the network cable indicates the presence of signals from two or more transmitters. If LANCE is transmitting when CLSN is asserted, it will continue to transmit the preamble, (normally collisions will occur while the preamble is being transmitted) then will "jam" the network for 32 bit times (3.2 microseconds). This jamming ensures that all nodes have enough time to detect the collision. The transmitting nodes then delay a random amount of time according to the "truncated binary backoff" algorithm defined in the Ethernet specification to minimize the probability of the colliding nodes having multiple collisions with each other. After 16 abortive attempts to transmit a packet, LANCE will report a RTRY error due to excessive collisions and step over the transmit buffer. During reception, the detection of a collision causes that reception to be aborted. Depending on when the collision occurred, LANCE will treat this packet as an error packet if the packet has an address mismatch, as a runt packet (a packet that has less than 64 bytes), or as a legal length packet with a CRC error. Extensive error reporting is provided by the LANCE through a microprocessor interrupt and error bits in a status register. The following are the significant error conditions: CRC error on received data; transmitter on longer than 1518 bytes; missed packet error (meaning a packet on the network cable was missed because there were no empty buffers in memory), and memory error, in which the memory did not respond (handshake) to a memory cycle request.

1.3.3 BUFFER MANAGEMENT

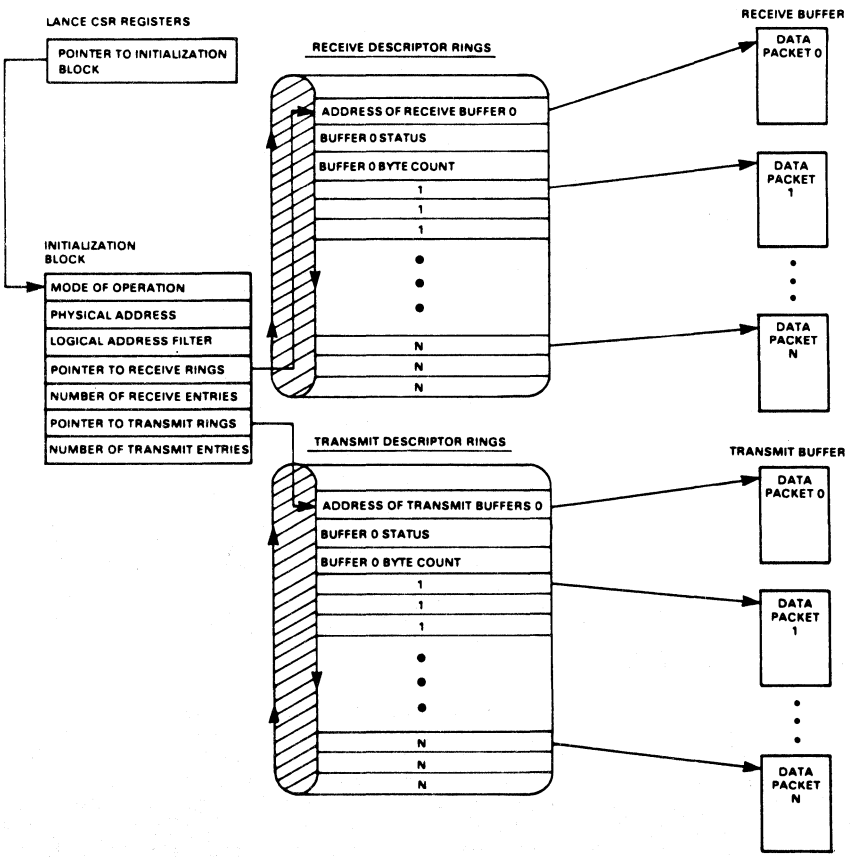
A key feature of the LANCE and its on board DMA channel is the flexibility and speed of communication between the LANCE and the host microprocessor through common memory locations. The basic organization of the buffer management is a circular queue of tasks in memory called descriptor rings, as shown in Figure 6. There are separate descriptor rings to describe transmit and receive operations. Up to 128 tasks may be queued up on a descriptor ring awaiting execution by the LANCE. Each entry in a descriptor ring holds a pointer to a data memory buffer and an entry for the length of the data buffer. Data buffers can be chained or cascaded in order to handle a long packet in multiple data buffer areas. The LANCE searches the descriptor

rings in a "look ahead manner" to determine the next empty buffer in order to chain buffers together or to handle back to back packets. As each buffer is filled, an "own" bit is reset, signaling the host processor to empty this buffer. The minimum buffer size is 64 bytes for receive buffers and 100 bytes for transmit buffers.

1.3.4 MICROPROCESSOR INTERFACE

The parallel interface of the LANCE has been designed to be "friendly" or easy to interface to a variety of popular 16-bit microprocessors. These microprocessors include the following: MK68000, Z8000, 8086, LSI-11, T-11, and MK68200. (The MK68200 is a 16-bit single chip microcomputer being sampled by Mostek with an architecture modeled after the MK68000). The LANCE has a wide 24-bit linear address space when it is in the Bus Master Mode, allowing it to DMA directly into the entire address space of the above microprocessors. No segmentation or paging methods are used within the LANCE, and as such the addressing is closest to that used by the MK68000 but is compatible with the others. When the LANCE is a bus master, a programmable mode of operation allows byte addressing either by employing a Byte/Word control signal, much like that used on the 8086 or the Z8000, or by using an Upper Data Strobe/Lower Data strobe much like that used on the MK68000, LSI-11, and MK68200 microprocessors. A program-

LANCE MEMORY MANAGEMENT
Figure 6

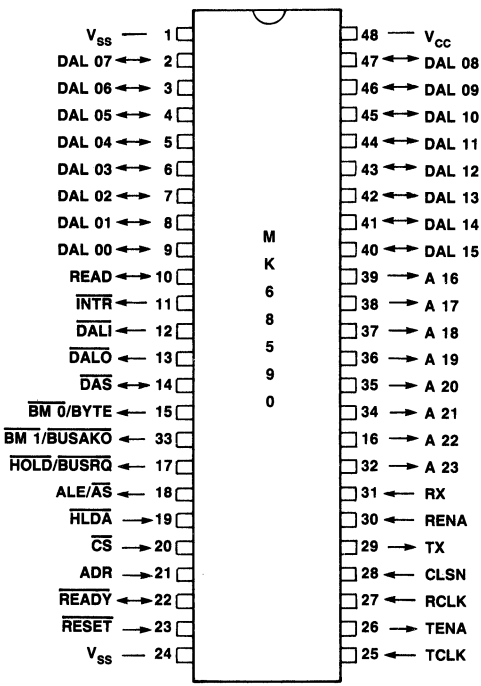


mable polarity on the Address Strobe signal eliminates the need for external logic. The LANCE interfaces with both multiplexed and demultiplexed data buses and features control signals for address/data bus transceivers.

Interrupts to the microprocessor are generated by the LANCE upon completion of its initialization routine, the reception of a packet, the transmission of a packet, transmitter timeout error, a missed packet, or a memory error.

The cause of the interrupt is ascertained by reading the control status register (CSR0). Bit (06) of CSR0, INEA, enables or disables interrupts to the microprocessor. In a polling mode, BIT (07) of CSR0 is sampled to determine when an interrupt causing condition occurred.

LANCE PIN ASSIGNMENT
Figure 7



1.3.5 PIN DESCRIPTION

DAL00-DAL15
(Data/Address Bus)
Input/Output Tri-State. Pins 2-9 and 40-47. The time multiplexed Address/Data bus. During the address portion of a memory transfer, DAL <15:00> contains the lower 16 bits of the memory address. The upper 8 bits of address are contained in A <23:16>. During the data portion of a memory transfer, DAL <15:00> contains the read or write data, depending on the type of transfer. The LANCE drives these lines both as a Bus Master and as a Bus Slave.

READ
Input/Output Tri-State. Pin 10. Read indicates the type of operation the bus controller is performing during a bus transaction. When it is a Bus Master, LANCE drives READ. Read is valid during the entire bus transaction and is tri-stated at all other times.

LANCE as Bus Slave:
High - The chip places data on the DAL lines.
Low - The chip takes data off the DAL lines.
LANCE as Bus Master:
High - The chip takes data off the DAL lines.
Low - The chip places data on the DAL lines.

$\overline{\text{INTR}}$
(Interrupt)
Output Open Drain. Pin 11. INTERRUPT is an attention interrupt line that indicates that one or more of the following CSR0 status flags is set: BABL, MISS, MERR, RINT, TINT OR IDON. Interrupt is enabled by CSR0 <6>, INEA = 1.

$\overline{\text{DALI}}$
(Data/Address Line In)
Output Tri-State. Pin 12. DAL IN is an external bus transceiver control line. LANCE drives $\overline{\text{DALI}}$ only while it is the Bus Master. When LANCE reads the DAL lines during the data portion of a READ transfer, $\overline{\text{DALI}}$ is asserted. $\overline{\text{DALI}}$ is not asserted during a WRITE transfer.

$\overline{\text{DALO}}$
(Data/Address Line Out)
Output Tri-State. Pin 13. DAL OUT is an external bus transceiver control line. LANCE drives $\overline{\text{DALO}}$ only when it is a Bus Master. When LANCE drives the DAL lines during the address portion of a READ transfer or for the duration of a WRITE transfer, $\overline{\text{DALO}}$ is asserted.

$\overline{\text{DAS}}$
(Data/Strobe)
Input/Output Tri-State. Pin 14. Data Strobe defines the data portion of the bus transaction. By definition, data is stable and valid at the low to high transition of $\overline{\text{DAS}}$. When it is the Bus Master, LANCE drives this signal. At all other times, the signal is tri-stated.

$\overline{\text{BM0}}$, $\overline{\text{BM1}}$ or BYTE, $\overline{\text{BUSAK0}}$
(Byte Mask)
Output Tri-State. Pins 15 and 16 are programmable through CSR3.

CSR3<00> BCON = 0
PIN 15 = $\overline{\text{BM0}}$ (Output Tri-State)
PIN 16 = $\overline{\text{BM1}}$ (Output Tri-State)
Byte Mask <1:0> Indicates the byte(s) on the DAL to be read or written during this bus transaction. LANCE drives these lines only as a Bus Master. LANCE ignores the BM lines when it is a Bus Slave and assumes word transfers. Byte selection follows:

$\overline{\text{BM1}}$	$\overline{\text{BM0}}$	
LOW	LOW	Whole Word
LOW	HIGH	Byte <DAL 15:08>
HIGH	LOW	Byte <DAL 07:00>
HIGH	HIGH	None

CSR3<00> BCON = 1
PIN 15 = BYTE (Output Tri-State)
PIN 16 = $\overline{\text{BUSAKO}}$ (Output)

Byte selection occurs by using the BYTE line and DAL <00> latched during the address portion of the bus transaction. LANCE drives BYTE only as a Bus Master and ignores it when operating as a Bus Slave. Byte selection occurs as follows:

BYTE	DAL<00>	(During Address Portion)
LOW	LOW	WHOLE WORD
LOW	HIGH	ILLEGAL CONDITION
HIGH	LOW	LOWER BYTE
HIGH	HIGH	UPPER BYTE

$\overline{\text{BUSAKO}}$ is a bus request daisy chain output. If LANCE is not requesting the bus and it receives $\overline{\text{HLDA}}$, $\overline{\text{BUSAKO}}$ is driven low. If LANCE is requesting the bus when it receives $\overline{\text{HLDA}}$, $\overline{\text{BUSAKO}}$ remains high.

$\overline{\text{HOLD}}$/$\overline{\text{BUSRQ}}$
(Bus Hold Request)

Input/Output Open Drain. Pin 17. This pin is programmable through CSR3.

CSR3<00> BCON = 0
PIN 17 = $\overline{\text{HOLD}}$

LANCE asserts the $\overline{\text{HOLD}}$ request when it requires a DMA cycle regardless of the $\overline{\text{HOLD}}$ pin state. $\overline{\text{HOLD}}$ is held LOW for the entire bus transaction.

CSR3<00> BCON = 1
PIN 17 = $\overline{\text{BUSRQ}}$

LANCE asserts $\overline{\text{BUSRQ}}$ when it requires a DMA cycle if the prior state of the $\overline{\text{BUSRQ}}$ pin was high. $\overline{\text{BUSRQ}}$ is held low for the entire bus transaction.

ALE/$\overline{\text{AS}}$
(Address Latch Enable)

Output Tri-State. Pin 18. The active level of Address Strobe is programmable through CSR3. The address portion of a bus transfer occurs while this signal is at its asserted level. LANCE drives this signal while it is the Bus Master. At all other times, the signal is tri-stated.

CSR3<01> ACON = 0
PIN 18 = ALE

Address Latch Enable is used to demultiplex the DAL lines and define the address portion of the transfer. As ALE, the signal transitions from high to low during the address portion of the transfer and remains low during the data portion. A slave device can use ALE to control a latch on the bus address lines. When ALE is high, the latch should be open and when ALE goes low, the latch should be closed.

CSR3<01> ACON = 1
PIN 18 = AS

As AS, the signal pulses low during the address portion of the bus transfer. The low to high transition of AS can be used by a slave device to strobe the address into a register.

$\overline{\text{HLDA}}$
(Hold Acknowledge)

Input. Pin 19. Hold Acknowledge is the response to $\overline{\text{HOLD}}$. When $\overline{\text{HLDA}}$ is low in response to LANCE's assertion of $\overline{\text{HOLD}}$, the LANCE is the Bus Master. $\overline{\text{HLDA}}$ should be deasserted after LANCE releases $\overline{\text{HOLD}}$.

$\overline{CS}$
(Chip Select)
Input. Pin 20. When low, $\overline{CS}$ indicates LANCE is the slave device for the data transfer. $\overline{CS}$ must be valid throughout the data portion of the transaction.

ADR
(Register Address Port Select)
Input. Pin 21. Address selects the Register Address Port or the Register Data Port. It must be valid throughout the data portion of the transfer and the chip only uses it when $\overline{CS}$ is low.

ADR	PORT
LOW	Register Data Port
HIGH	Register Address Port

$\overline{READY}$
Input/Output Open Drain. Pin 22. When LANCE is a Bus Master, $\overline{READY}$ is an asynchronous acknowledgement from the bus memory that memory will accept data in a WRITE cycle or that memory has put data on the DAL lines in a READ cycle. As a Bus Slave, LANCE asserts $\overline{READY}$ when it has put data on the DAL lines during a READ cycle or is about to take data off the DAL lines during a WRITE cycle. $\overline{READY}$ is a response to $\overline{DAS}$ and is negated after $\overline{DAS}$ is negated. $\overline{CS}$ and $\overline{DAS}$ must remain asserted until $\overline{READY}$ is asserted or $\overline{READY}$ will not be asserted.

$\overline{RESET}$
(Bus Reset Signal.)
Input. Pin 23. Causes LANCE to cease operation, clear its internal logic and enter an idle state with the STOP bit of CSR0 set.

TLCK
(Transmit Clock)
Input. Pin 25. A crystal-controlled 10 MHz clock. This clock is the primary LANCE clock as well as the Transmit clock. (A 0.01 % clock as specified in the Ethernet Specification.)

TENA
(Transmit Enable)
Output. Pin 26. A high level signal asserted with the transmit output serial bit stream, TX, to enable the external transmit logic.

RCLK
(Receive Clock)
Input. Pin 27. The 10 MHz clock that is synchronous with the received data and is used for transferring the received data into the LANCE.

CLSN
Collision)
Input. Pin 28. A logical input that indicates, when high, that a collision is occurring on the channel.

TX
(Transmit)
Output. Pin 29. Transmit Output Bit Stream.

RENA
(Receive Enable)
Input. Pin 30. A logical input that indicates, when high, the presence of data on the channel.

RX
(Receive)
Input. Pin 31. The input for the serial receive data. The data is synchronous with the receive clock.

A16-A23
(High-Order Address Bus)
Output, Three State pins 32 thru 39. Address bits <23:16> used in conjunction with DAL <15:00> to produce a 24-bit address. LANCE drives these lines only as a Bus Master.

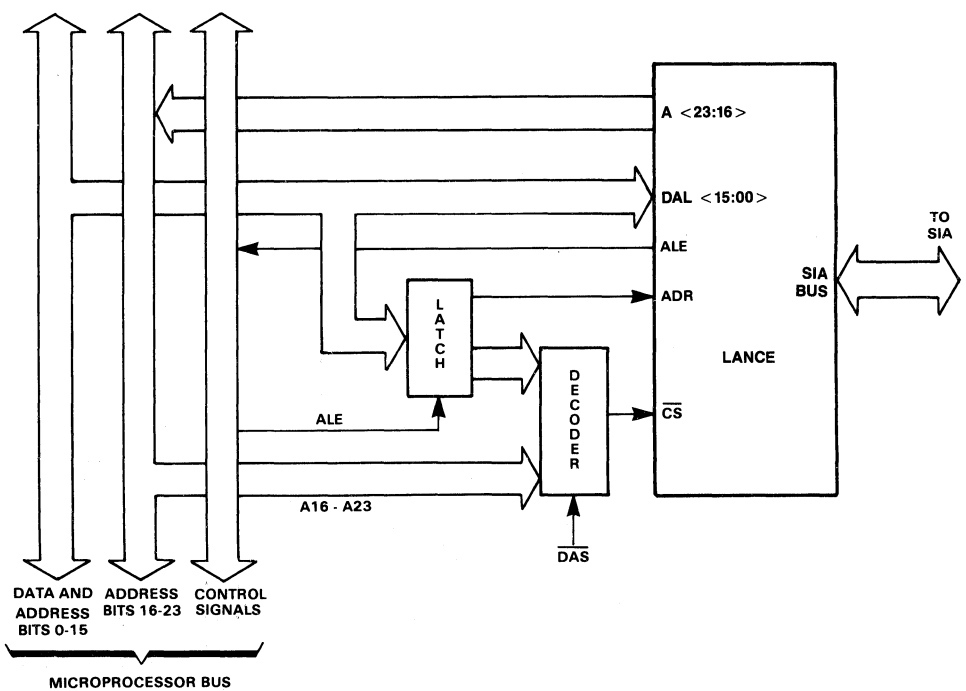
V_{CC}
Power supply pin 48. +5 VDC ±5%. It is recommended that a power supply filter be used between V_{CC} (Pin 48) and V_{SS} (Pins 1 and 24). This filter should consist of two capacitors in parallel having the values of 10μF and .047μF respectively.

V_{SS}
Ground pins 1 and 24. 0 VDC

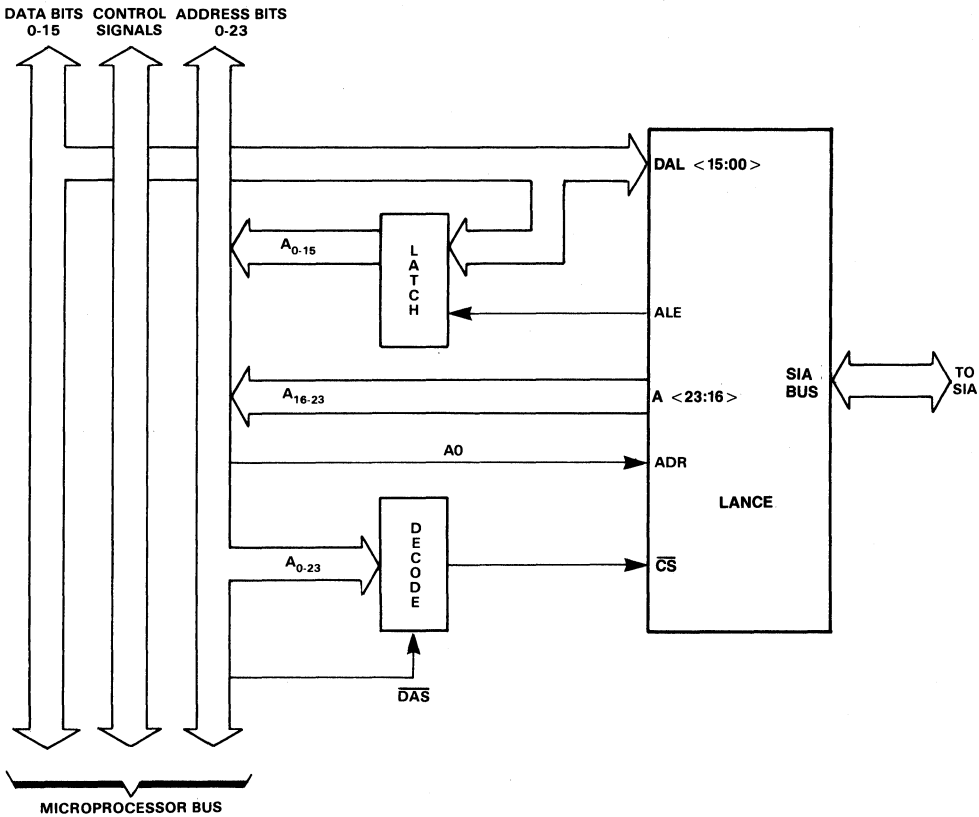
1.3.6 LANCE INTERFACE DESCRIPTION--BUS MASTER MODE

All data transfers from the LANCE in the Bus Master mode are timed by ALE, $\overline{DAS}$, and $\overline{READY}$. The automatic adjustment of the LANCE cycle by the $\overline{READY}$ signal allows synchronization with variable cycle time memory due either to memory refresh or to dual port access. Bus cycles are a minimum of 600 nsec in length and can be increased in 100 nsec increments. Figure 8 and Figure 9 show generalized interfaces to both multiplexed and demultiplexed bus microprocessors, and Figure 10, the Bus Master Timing modes.

MULTIPLEXED BUS INTERFACE
Figure 8



DEMULTIPLEXED BUS INTERFACE
Figure 9

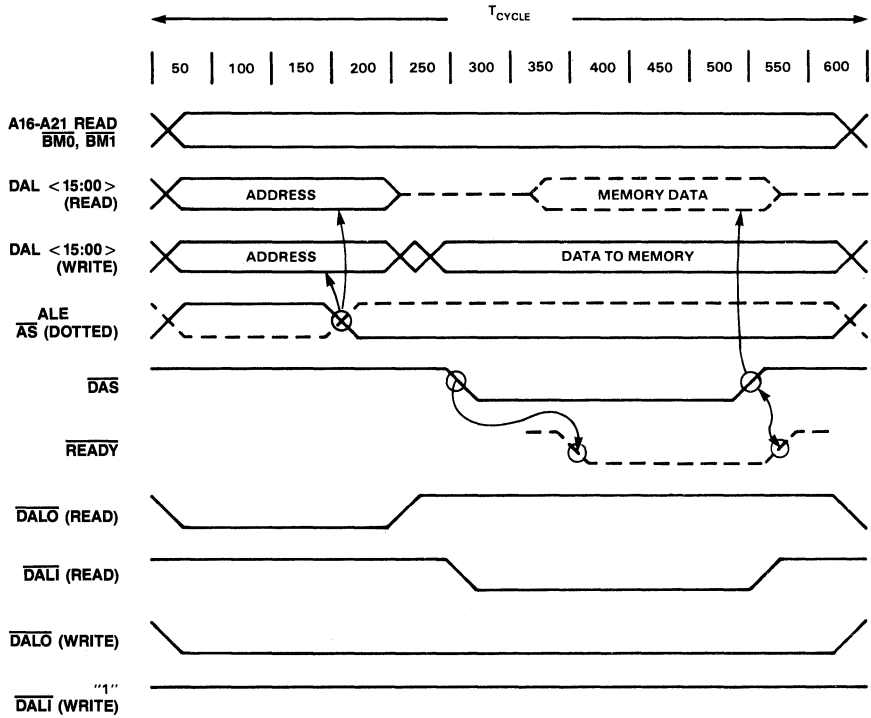


1.3.6.1 READ SEQUENCE

At the beginning of a read cycle, valid addresses are placed on DAL <15:00> and A <23:16>. The BYTE Mask signals ($\overline{BM0}$ and $\overline{BM1}$) become valid at the beginning of this cycle as does READ, indicating the type of cycle. The trailing edge of ALE or $\overline{AS}$ is used to strobe in the addresses A <15:00> into the external latches. Approximately a hundred nanoseconds later, DAL <15:00> go into a tristate mode. There is a fifty nanosecond delay to allow for transceiver turnaround, then $\overline{DAS}$ falls low to signal the beginning of the data portion of the cycle. At this point in the cycle, the LANCE waits for the memory device to assert $\overline{READY}$. Upon assertion of $\overline{READY}$, $\overline{DAS}$ makes a transition from a zero to a one, latching memory data. ($\overline{DAS}$) is low for a minimum of 200 nsec).

The bus transceiver controls, $\overline{DALI}$ and $\overline{DALO}$, are used to control the bus transceivers. The $\overline{DALI}$ signal is used to strobe data toward the LANCE and the $\overline{DALO}$ signal is used to strobe data or addresses away from the LANCE. During a read cycle, $\overline{DALO}$ goes inactive before $\overline{DALI}$ goes active to avoid the "spiking" of the bus transceivers.

BUS MASTER TIMING
Figure 10



1.3.6.2 WRITE SEQUENCE

The write cycle begins exactly like a read cycle with the READ line remaining inactive. After ALE or AS pulse, the DAL <15:00> change from addresses to data. DAS goes active when the DAL <15:00> lines are stable. This data will remain valid on the bus until the memory device asserts READY. At this point, DAS goes inactive latching data into the memory device. Data is held for 75 nanoseconds after the deassertion of DAS.

1.3.7 LANCE INTERFACE DESCRIPTION--BUS SLAVE MODE

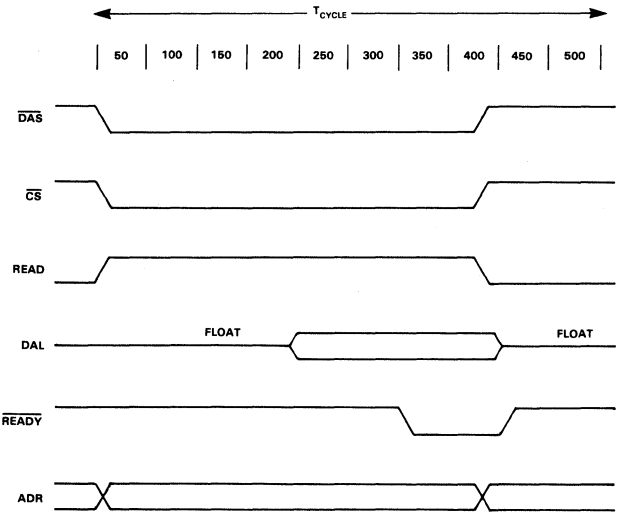
The LANCE enters the Bus Slave Mode whenever CS becomes active. This mode must be entered whenever writing or reading the four status control registers (CSR0, CSR1, CSR2, and CSR3) and the register address pointer (RAP). RAP and CSR0 may be read or written to at any time, but the LANCE must be stopped for CSR1, CSR2, and CSR3 to be written to or read.

1.3.7.1 READ SEQUENCE

CS, READ, and DAS are asserted at the beginning of a read cycle. ADR also must be valid at this time. (If ADR is a "1", the contents of RAP are placed on the DAL lines. Otherwise the contents of the CSR register addressed by RAP are placed on the DAL lines.) After the data on the DAL lines become valid, LANCE asserts READY. CS, READ, DAS, and ADR must remain stable throughout the read cycle. Refer to Figure 11.

BUS SLAVE READ TIMING FOR CSR0, RAP, AND CSR3

Figure 11



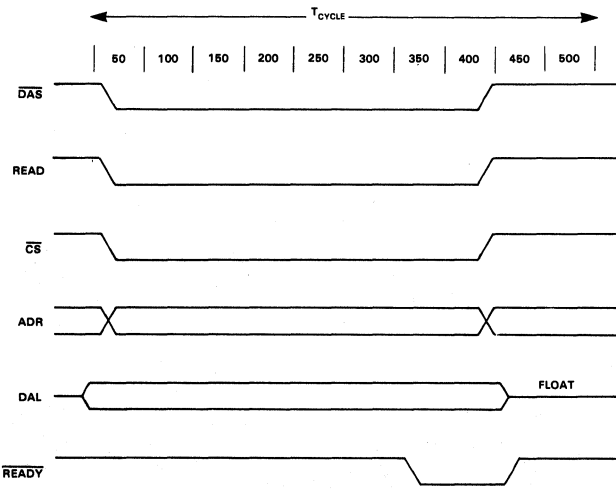
Timing for CSR1 and CSR2 are similar but the DELAY to READY becomes 1250 instead of 350 μs.

1.3.7.2 WRITE SEQUENCE

This cycle is similar to the read cycle, except that during this cycle, READ is not asserted. The DAL buffers are tristated which configures these lines as inputs. The assertion of READY by LANCE indicates to the memory device that the data on the DAL lines has been stored by LANCE in its appropriate CSR register. CS, READ, DAS, ADR, and DAL <15:00> must remain stable throughout the write cycle. Refer to Figure 12.

BUS SLAVE WRITE TIMING FOR CSR0, RAP, AND CSR3

Figure 12



Timing for CSR1 and CSR 2 are similar but the DELAY to READY becomes 1250 instead of 350 μs.

1.3.7.3 REFERENCE DOCUMENTS

The following documents provide a good overview and background for Ethernet. They can be requested from:

Ethernet
Xerox Office Systems Division
Dept. A
3333 Coyote Hills Rd.
Palo Alto, CA 94304

1. The Ethernet, a Local Area Network, Data Link Layer and Physical Layer Specifications--Version 2.0, November 1982.

2. John F. Shoch, An Annotated Bibliography on Local Computer Networks, October 1979.

3. The Ethernet Local Network: Three Reports, February 1980.

4. Internet Transport Protocols, Xerox System Integration Standard, December 1981.

5. Courier: The Remote Procedure Call Protocol, Xerox System Integration Standard, December 1981.

CHAPTER 2
PROGRAMMING SPECIFICATIONS

2.0 INTRODUCTION

2.1 PROGRAMMING SPECIFICATIONS

This section defines the Control and Status Registers and the memory data structures required to program the LANCE Ethernet Protocol Controller.

2.2 PROGRAMMING THE LANCE

The LANCE is designed to operate in an environment that includes close coupling with a local memory and a microprocessor (HOST). The LANCE is programmed by a combination of registers and data structures resident within the LANCE and in memory. There are four Control and Status Registers (CSR's) within the LANCE which are programmed by the HOST device. Once enabled, the LANCE has the ability to access external buffer memory locations to acquire additional operating parameters. LANCE has the ability to do independent buffer management as well as transfer data packets to and from an Ethernet. There are three memory structures accessed by LANCE, as follows:

1. Initialization Block - 12 words in contiguous memory starting on a word boundary. The initialization block is assembled by the HOST, and is accessed by LANCE. The initialization block contains the operating parameters necessary for device operation. The initialization block is comprised of:

    1. Mode of Operation (1 Word)
    2. Physical Address (3 Words)
    3. Logical Address Mask (4 Words)
    4. Location of Receive and Transmit Descriptor Rings (2 Words)
    5. Number of Entries in Receive and Transmit Descriptor Rings (2 Words)

2. Receive and Transmit Descriptor Rings - Two ring structures, one each for incoming and outgoing packets. Each entry in the rings is 4 words long. Each entry must start on a quadword boundary. The Descriptor Rings are comprised of:

    1. The address of a data buffer.
    2. The length of that buffer.
    3. Status information associated with the buffer.

3. Data Buffers - Contiguous portions of memory reserved for packet buffering. Data buffers may begin on arbitrary byte boundaries.

In general, the programming sequence of LANCE may be summarized as:

1. Programming the LANCE CSR's by a HOST device to locate an initialization block in memory.
2. LANCE loading itself with the information contained within the initialization block.
3. LANCE accessing the Descriptor Rings for packet handling.

2.3 CONTROL AND STATUS REGISTERS

There are four Control and Status Registers (CSR's) resident within LANCE. The CSR's are accessed through two bus addressable ports, an address port (RAP), and a data port (RDP).

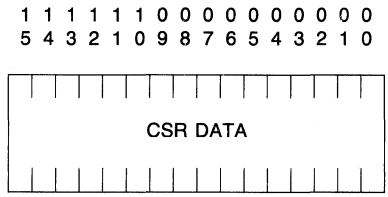
2.3.1 ACCESSING THE CONTROL AND STATUS REGISTERS

The CSR's are read (or written) in a two step operation. The address of the CSR is written into

the address port (RAP) during a bus slave transaction. During a subsequent bus slave transaction, the data being read from (or written into) the data port (RDP) is read from (or written into) the CSR selected in the RAP. Once written, the address in RAP remains unchanged until rewritten. A discrete control input pin (ADR) is provided to distinguish the address port from the data port.

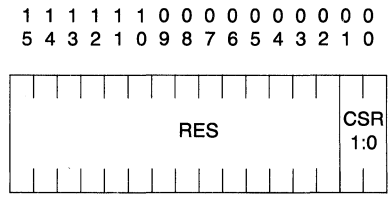
ADR Pin	Port
L	REGISTER DATA PORT (RDP)
H	REGISTER ADDRESS PORT (RAP)

2.3.1.1 REGISTER DATA PORT (RDP)



CSR DATA
Bits 15:00
Writing data to the RDP loads data into the CSR selected by RAP. Reading the data from RDP reads the data from the CSR selected by RAP. CSR1, CSR2 and CSR3 are accessible only when the STOP bit of CSR0 is set. If an attempt to access CSR1, CSR2, or CSR3 is made without the STOP bit being set, LANCE does not respond to the bus transfer. LANCE will assert $\overline{\text{READY}}$, but no data will be transferred either into or out of these registers.

2.3.1.2 REGISTER ADDRESS PORT (RAP)



RES
Bits 15:02
Reserved and read as zeros.

CSR
Bits 01:00
CSR address select bits. READ/WRITE. Selects the CSR to be accessed through the RDP. RAP is cleared by Bus RESET.

CSR<1:0>	CSR
0	CSR0
1	CSR1
2	CSR2
3	CSR3

2.3.2 CONTROL AND STATUS REGISTER DEFINITION

2.3.2.1 CONTROL AND STATUS REGISTER 0 (CSR0)

RAP = 0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ERR	BABL	CERR	MISS	MERR	RINT	TINT	IDON	INTR	INEA	RXON	TXON	TDMD	STOP	STRT	INIT

ERR
Bit 15
(Error Summary) Error Summary is set by the 'OR' of BABL, CERR, MISS and MERR. ERR remains set as long as any of the error flags are true. ERR is read only, writing it has no effect. It is cleared by $\overline{\text{RESET}}$ or by setting the stop bit.

BABL
Bit 14
(Babble) BABL is a transmitter timeout error. It indicates that the transmitter has been on longer than the time required to send the maximum length packet. BABL will be set if the number of bytes transmitted exceeds 1518. When BABL is set, an interrupt will be generated if INEA = 1. BABL is READ/CLEAR ONLY and is set by LANCE and cleared by writing a "1" into the bit. Writing a "0" has no effect. $\overline{\text{RESET}}$ or setting the STOP bit clears it.

CERR
Bit 13
(Collision Error)
Collision Error indicates that the collision input to the chip failed to activate within 2 usec after a chip-initiated transmission was completed. Collision after transmission is a transceiver test feature. CERR is READ/CLEAR ONLY. The chip sets it and clears it by writing a "1" into the bit. Writing a "0" has no effect. $\overline{\text{RESET}}$ or setting the STOP bit clears it.

MISS
Bit 12
(Missed Packet) Missed Packet is set whenever a packet arrives and passes address recognition, but is lost because the receiver does not own a receive buffer. When MISS is set, an interrupt will be generated if INEA = 1. MISS is READ/CLEAR ONLY and is set by LANCE and cleared by writing a "1" into the bit. Writing a "0" has no effect. $\overline{\text{RESET}}$ or setting the STOP bit clears it.

MERR
Bit 11
(Memory Error) Memory Error sets when LANCE is the Bus Master and has not received READY within 25.6 μsec after asserting the address on the DAL lines. When a Memory Error is detected, the receiver and transmitter are turned off and an interrupt is generated if INEA = 1. MERR is READ/CLEAR ONLY and is set by the chip and cleared by writing a "1" into the bit. Writing a "0" has no effect. $\overline{\text{RESET}}$ or setting the STOP bit clears it.

RINT
Bit 10
(Receiver Interrupt) Receiver Interrupt is set after LANCE updates the last entry in the Receive Descriptor Ring for the completed packet. When RINT is set, an interrupt is generated if INEA = 1. RINT is READ/CLEAR ONLY and is set by LANCE and cleared by writing a "1" into the bit. Writing a "0" has no effect. RESET or setting the STOP bit clears it.

TINT
Bit 09
(Transmitter Interrupt) Transmitter Interrupt is set after LANCE updates the last entry in the Transmit Descriptor Ring for that completed packet. When TINT is set, an interrupt is generated if INEA = 1. TINT is READ/CLEAR ONLY and is set by LANCE and cleared by writing a "1" into the bit. Writing a "0" has no effect. $\overline{\text{RESET}}$ or setting the STOP bit clears it.

IDON
Bit 08
(Initialization Done) Initialization Done indicates that LANCE has completed the initialization procedure started by setting the INIT bit. When IDON is set, the chip has read the Initialization Block from memory and stored the new parameters. When IDON is set, an interrupt is generated if INEA = 1. IDON is READ/CLEAR ONLY and is set by LANCE and cleared by writing a "1" into the bit. Writing a "0" has no effect. $\overline{\text{RESET}}$ or setting the STOP bit clears it.

INTR
Bit 07
(Interrupt Flag) Interrupt Flag indicates that one or more of the following interrupt causing conditions has occurred: BABL, MISS, MERR, RINT, TINT, IDON. If INEA = 1 and INTR = 1 the $\overline{\text{INTR}}$ output pin will be low. INTR is READ ONLY, writing this bit has no effect. INTR is cleared by $\overline{\text{RESET}}$ or by setting the STOP bit.

INEA
Bit 06
(Interrupt Enable) Interrupt Enable allows the INTR Output pin to be driven low when the Interrupt Flag is set. If INEA = 1 and INTR = 1 the INTR pin will be low. If INEA = 1 and INTR = 1 the INTR pin will be low. If INEA = 0 the INTR pin will be high, regardless of the state of the Interrupt Flag. INEA is READ/WRITE set by writing a "1" into this bit and is cleared by writing a "0" into this bit or by $\overline{\text{RESET}}$ or by setting the STOP bit.

RXON
Bit 05
(Receiver On) Receiver On indicates that the receiver is enabled. RXON and IDON are set at the same time, if the DRX bit in the Mode Register is a "0". RXON is cleared by MERR or STOP being set or by RESET. RXON is READ ONLY, writing this bit has no effect. RXON is gated by the STRT bit; thus it will always be read as a "0" until STRT is set.

TXON
Bit 04
(Transmitter On) Transmitter On indicates that the transmitter is enabled. TXON and IDON are set at the same time, if the DTX bit in the Mode Register is "0". TXON is cleared by MERR, or STOP being set, a TRANSMIT UNDERFLOW, or by RESET. TXON is READ ONLY; writing this bit has no effect. TXON is gated by the STRT bit; thus it will always be read as a "0" until STRT is set.

TDMD
Bit 03
(Transmit Demand) When set, Transmit Demand causes LANCE to access the Transmit

Descriptor Ring without waiting for the polltime interval to elapse. (about 1.6 ms). TDMD need not be set to transmit a packet, it merely hastens LANCE's response to a Transmit Descriptor Ring entry insertion by the host. TDMD is WRITE WITH ONE ONLY and microcode clears it after it is used. It may read as a "1" for a short time after it is written because the LANCE microcode may have been busy when TDMD was set. It is also cleared by RESET or by setting the STOP bit. Writing a "0" in this bit has no effect.

STOP
Bit 02
(Stop) STOP disables LANCE from all external activity when set and clears the internal logic. Setting STOP is the equivalent of asserting Bus RESET. LANCE remains inactive and STOP remains set until the STRT or INIT bit is set. If STRT, INIT and STOP are all set together, STOP will override the other bits and only STOP will be set. STOP IS READ/WRITE WITH ONE ONLY and set by RESET. Writing a "0" to this bit has no effect.

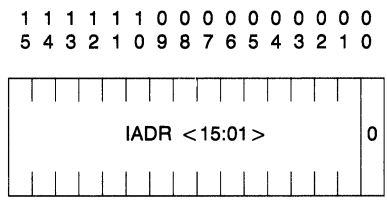
STRT
Bit 01
(Start) Start enables LANCE to send and receive packets, perform direct memory access and do buffer management. If STRT and INIT are set together, the INIT function will be executed first. STRT is READ/WRITE WITH ONE ONLY. Writing a "0" into this bit has no effect. STRT is cleared by RESET or by setting the STOP bit.

INIT
Bit 00
(Initialize) When set, Initialize causes LANCE to begin the initialization procedure and access the Initialization Block. If STRT and INIT are set together, the INIT function is executed first. INIT is READ/WRITE WITH "1" ONLY. Writing a "0" into this bit has no effect. INIT is cleared by RESET or by setting the STOP bit.

2.3.2.2 CONTROL AND STATUS REGISTER 1 (CSR1)

RAP = 1

READ/WRITE: Accessible only when the STOP bit of CSR0 is a ONE. Access at any other time will not be responded to by LANCE. READY will be asserted but no data will be transferred. CSR1 is unaffected by RESET.

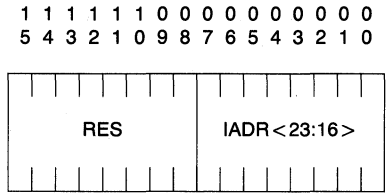


IADR
Bits 15:01
The low order 16 bits of the address of the first word (lowest address) in the Initialization Block. Bit 00 must be zero.

2.3.2.3 CONTROL AND STATUS REGISTER 2 (CSR2)

RAP = 2

READ/WRITE: Accessible only when the STOP bit of CSR0 is a ONE. Access at any other time will not be responded to by LANCE. READY will be asserted but no data will be transferred. CSR2 is unaffected by RESET.



RES
Bits 15:08
Reserved.

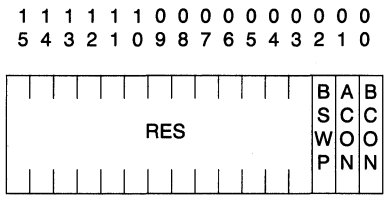
IADR
Bits 07:00
The high order 8 bits of the address of the first word (lowest address in the Initialization Block.

2.3.2.4 CONTROL AND STATUS REGISTER 3 (CSR3)

CSR3 allows redefinition of the Bus Master interface.

RAP = 3

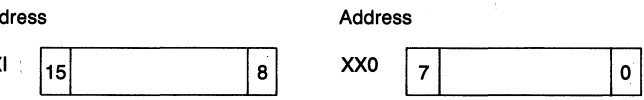
READ/WRITE: Accessible only when the STOP bit of CSR0 is a ONE. Access at any other time will not be responded to by LANCE. $\overline{\text{READY}}$ will be asserted but no data will be transferred. CSR3 is cleared by $\overline{\text{RESET}}$ or by setting the STOP bit in CSR0.



RES
Bits 15:03
Reserved/read as "0".

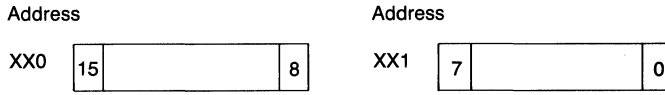
BSWP
Bit 02
(Byte Swap) Byte Swap allows LANCE to operate with memory organizations that have bits <07:00> at even addresses with bits <15:08> at odd addresses or vice versa.

With Byte Swap = 0:



This memory organization is used with the LSI 11 microprocessor and the 8086 microprocessor.

With Byte Swap = 1:



This memory organization is used with the MK68000, MK68200, and Z8000 microprocessors. Only data from SILO transfers are swapped. Initialization Block Data and Ring Descriptor entries are not swapped. BSWP is READ/WRITE and cleared by RESET or by setting the STOP bit in CSR0.

ACON
Bit 01
(ALE Control) ALE Control defines the assertive state of ALE/$\overline{AS}$ when LANCE is a Bus Master. ACON is READ/WRITE and cleared by $\overline{RESET}$ or by setting the STOP bit in CSR0.

ACON	ALE/$\overline{AS}$
0	ASSERTED HIGH (ALE)
1	ASSERTED LOW ($\overline{AS}$)

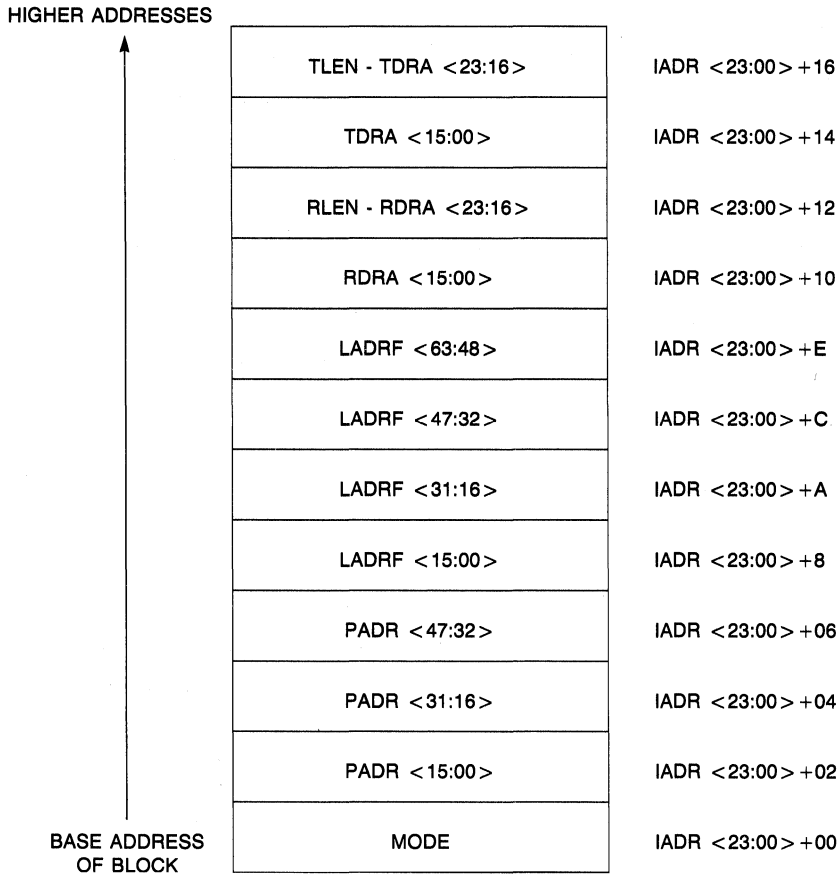
BCON
Bit 00
(Byte Control) Byte Control redefines the Byte Mask and Hold I/O Pins. BCON is READ/WRITE and cleared by $\overline{RESET}$ or by setting the STOP bit in CSR0.

BCON	I/O PIN 16	I/O PIN 15	I/O PIN 17
0	$\overline{BM1}$	$\overline{BM0}$	$\overline{HOLD}$
1	$\overline{BUSAKO}$	BYTE	$\overline{BUSRQ}$

2.4 INITIALIZATION

2.4.1 INITIALIZATION BLOCK

LANCE initialization includes the reading of the initialization block in memory to obtain the operating parameters. The following is a definition of the Initialization Block. The Initialization Block is read by LANCE when the INIT bit in CSR0 is set. The INIT bit should be set before or concurrent with the STRT bit to ensure proper parameter initialization and LANCE operation. After LANCE has read the Initialization Block, IDON is set in CSR0 and an interrupt is generated if INEA = 1.



2.4.1.1 MODE

The Mode Register allows alteration of LANCE's operating parameters. Normal operation is with the Mode Register clear.

IADR <23:00> +00

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
PROM	RES								INTL	DRTY	COLL	DTCR	LOOP	DTX	DRX

PROM
Bit 15
(Promiscuous Mode) When PROM = 1, all incoming addresses are accepted. This bit must be set in internal loopback if a physical address is not used.

RES
Bits 14:07
(Reserved)

INTL
Bit 06
(Internal Loopback) Internal Loopback is used with the LOOP bit to determine where the loopback is to be done. Internal loopback allows LANCE to receive its own transmitted packet. Since this represents full duplex operation, the packet size would be limited by the SILO size, which is 48 bytes. However, a SILO full flag is generated after 32 bytes are loaded into the SILO. This limits the transmit buffer size to 32 bytes in internal or extended loopback. With transmit CRC enabled, the LANCE generates the 4-byte CRC code and appends it to the data. Thus, the receive buffer is filled with 36 bytes and the host CPU checks the CRC result. With transmit CRC disabled, the host CPU provides 4 bytes of CRC as part of the 32 bytes in the transmit buffer. The LANCE checks the CRC on reception and transfers only 28 bytes of "data" to the receive buffer. After each Internal Loopback packet, LANCE should be reinitialized.

INTL is only valid if LOOP = 1, otherwise it is ignored.

LOOP	INTL	LOOPBACK
0	X	NO LOOPBACK, NORMAL OPERATION
1	0	EXTERNAL
1	1	INTERNAL

DRTY
Bit 05
(Disable Retry) When DRTY = 1, LANCE attempts only one packet transmission If there is a collision on the first transmission attempt, a Retry Error (RTRY) is reported in Transmit Message Descriptor 3 (TMD3).

COLL
Bit 04
(Force Collision) This bit allows the collision logic to be tested. LANCE must be in internal loopback mode for COLL to be valid. If COLL = 1, a collision will be forced during the subsequent transmission attempt. This will result in 1 or 16 total transmission attempts with a retry error reported in TMD3. The number of attempts depends upon the state of DRTY (Bit (05).

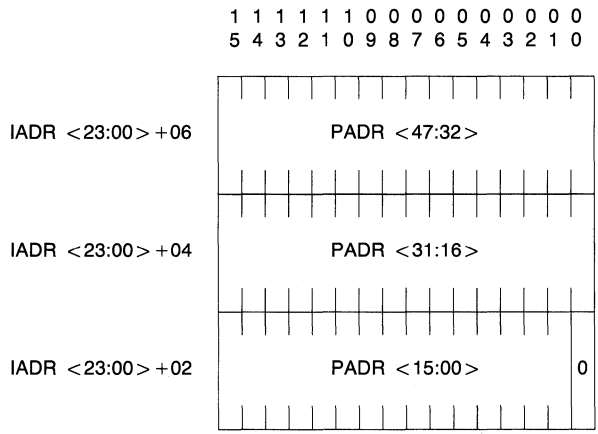
DTCR
Bit 03
(Disable Transmit CRC) When DTCR = 0, the transmitter generates and appends a CRC to the transmitted packet. When DTCR = 1, the CRC logic is allocated to the receiver and no CRC is generated and sent with the transmitted packet. During loopback, DTCR = 0 causes a CRC to be generated on the transmitted packet but the receiver will not perform a CRC check since the CRC logic is shared and cannot generate and check CRC at the same time. The generated CRC is written into memory with the data and can be checked by the host software. If DTCR = 1 during loopback the host software must append a CRC value to the transmit data. The receiver checks the CRC on the received data and reports any errors.

LOOP
Bit 02
(Loopback) Loopback allows LANCE to operate in full duplex mode for test purposes. The maximum packet size is limited to 36 bytes as described above for the INTL bit. During loopback, the runt packet filter is disabled because the maximum packet is forced to be smaller than the minimum size Ethernet packet (64 bytes). LOOP = 1 allows simultaneous transmission and reception for a message constrained to fit within the SILO. The chip waits until the entire message is in the SILO before serial transmission begins. The incoming data stream fills the SILO from behind as it is being emptied. Moving the received message out of the SILO to memory does not begin until reception has ceased. In loopback mode, transmit data chaining is not possible. Receive data chaining is allowed regardless of the receive buffer length. In normal operation, the receive buffers must be 64 bytes long, to allow time for buffer lookahead.

DTX
Bit 01
(Disable the Transmitter) Disable the Transmitter causes LANCE not to access the Transmit Descriptor Ring and therefore no transmissions are attempted. DTX disables TXON from being set when initialization is complete.

DRX
Bit 00
(Disable the Receiver) Disable the Receiver causes LANCE to reject all incoming packets and not access the Receive Descriptor Ring. DRX disables RXON from being set when initialization is complete.

2.4.1.2 PHYSICAL ADDRESS

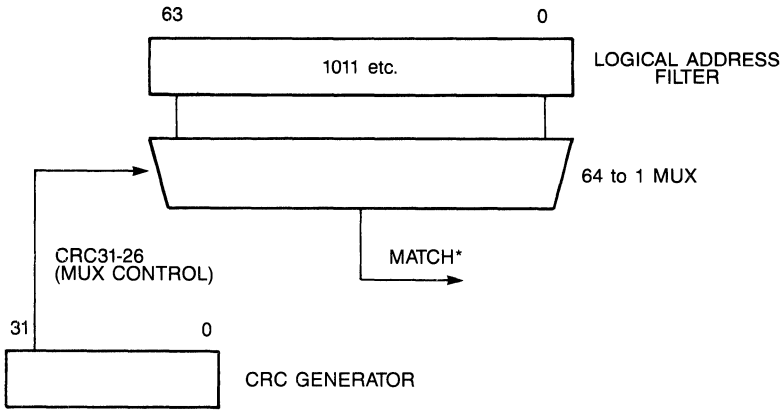


PADR
Bits 47:00
(Physical Address) Physical Address is the unique 48-bit physical address assigned to LANCE. PADR <0> must be zero.

2.4.1.3 LOGICAL ADDRESS FILTER

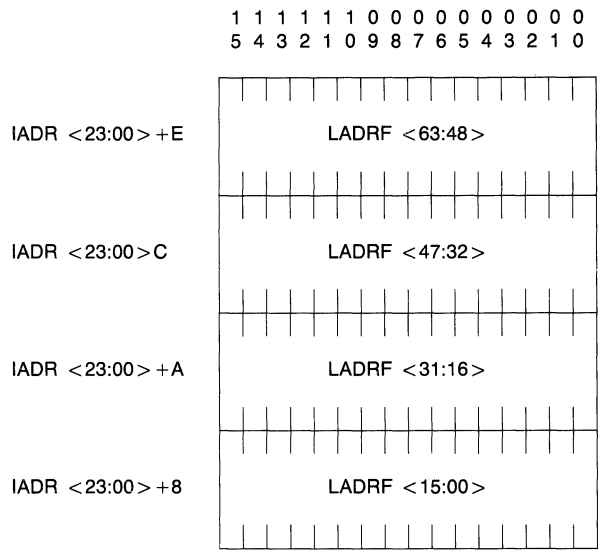
The Logical Address Filter is a 64 bit mask composed of four sixteen bit registers LADRF <63:00> in the initialization block that is used to accept incoming Logical Addresses. This is an imperfect filter that requires the host processor to do the final filtering. The first bit of the incoming address must be a "1" for either the Logical Address Filter or the Broadcast Address decode to be enabled. Otherwise the incoming address is a physical address and is compared against the contents of PADR <47:00> that was loaded through the Initialization Block.

All incoming data goes through the CRC Generator. In the case of a logical address, the six most significant bits of the CRC Generator are strobed into the Hash Register after the 48th bit of the logical address has gone through this circuitry. This 6-bit address then selects one of the 64 bits in the Logical Address Filter. If the mask bit selected is a "1", the address is accepted and the packet will be put into the current receive buffer space. The task of mapping a logical address to one of 64 bit positions is a tedious one that requires a simple computer program to generate the CRC codes for the addresses desired. The Ethernet CRC Polynomial is CRC-32, which is: $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$. Figure 13 shows one such mapping. (This is one of 2^{26} possible mappings). Hash Address 00 will select bit 0 and Hash Address 63 will select bit 63.



* If MATCH = 1, the packet is accepted.
If MATCH = 0, the packet is rejected.

The Broadcast address, which is all ones, is decoded independent of the Logical Address Filter (Broadcast Address will also map to bit 47 of the Logical Address Filter). If the Logical Address Filter is loaded with all zeroes, all incoming logical addresses except Broadcast will be rejected.

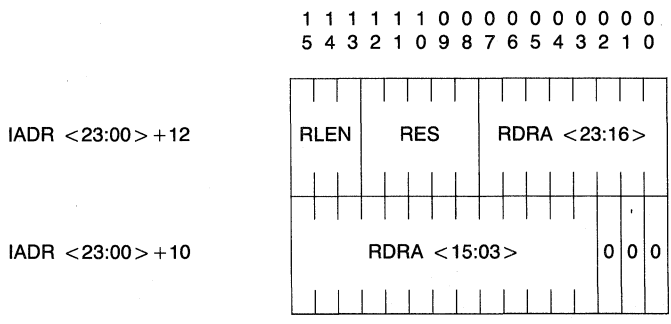


LADRF
Bits 63:00
The 64-bit mask used by LANCE to accept logical addresses.

MAPPING OF LOGICAL ADDRESS TO FILTER MASK
Figure 13

LAF REG BITS SET	LAF LOC. DEC.	DESTINATION ADDRESS ACCEPTED (HEX)	LAF REG. BITS SET	LAF LOC. DEC.	DESTINATION ADDRESS ACCEPTED (HEX)
0	0	FF FF FF FF FF 65	0	32	FF FF FF FF FF D1
	1	FF FF FF FF FF 55		33	FF FF FF FF FF F1
L	2	FF FF FF FF FF 15	L	34	FF FF FF FF FF B1
A	3	FF FF FF FF FF 35	A	35	FF FF FF FF FF 91
F	4	FF FF FF FF FF B5	F	36	FF FF FF FF FF 11
	5	FF FF FF FF FF 95		37	FF FF FF FF FF 31
0	6	FF FF FF FF FF D5	2	38	FF FF FF FF FF 71
	7	FF FF FF FF FF F5		39	FF FF FF FF FF 51
	8	FF FF FF FF FF DB		40	FF FF FF FF FF 7F
	9	FF FF FF FF FF FB		41	FF FF FF FF FF 4F
	10	FF FF FF FF FF BB		42	FF FF FF FF FF 1F
	11	FF FF FF FF FF 8B		43	FF FF FF FF FF 3F
	12	FF FF FF FF FF 0B		44	FF FF FF FF FF BF
	13	FF FF FF FF FF 3B		45	FF FF FF FF FF 9F
	14	FF FF FF FF FF 7B		46	FF FF FF FF FF DF
15	15	FF FF FF FF FF 5B	15	47	FF FF FF FF FF EF
0	16	FF FF FF FF FF 27	0	48	FF FF FF FF FF 93
	17	FF FF FF FF FF 07		49	FF FF FF FF FF B3
	18	FF FF FF FF FF 57		50	FF FF FF FF FF F3
	19	FF FF FF FF FF 77		51	FF FF FF FF FF D3
L	20	FF FF FF FF FF F7	L	52	FF FF FF FF FF 53
A	21	FF FF FF FF FF C7	A	53	FF FF FF FF FF 73
F	22	FF FF FF FF FF 97	F	54	FF FF FF FF FF 23
	23	FF FF FF FF FF A7		55	FF FF FF FF FF 13
1	24	FF FF FF FF FF 99	3	56	FF FF FF FF FF 3D
	25	FF FF FF FF FF B9		57	FF FF FF FF FF 0D
	26	FF FF FF FF FF F9		58	FF FF FF FF FF 5D
	27	FF FF FF FF FF C9		59	FF FF FF FF FF 7D
	28	FF FF FF FF FF 59		60	FF FF FF FF FF FD
	29	FF FF FF FF FF 79		61	FF FF FF FF FF DD
	30	FF FF FF FF FF 29		62	FF FF FF FF FF 9D
15	31	FF FF FF FF FF 19	15	63	FF FF FF FF FF BD

2.4.1.4 RECEIVE DESCRIPTOR RING POINTER



RLEN
Bits 15:13
(Receive Ring Length) Receive Ring Length is the number of entries in the Receive Ring expressed as a power of two.

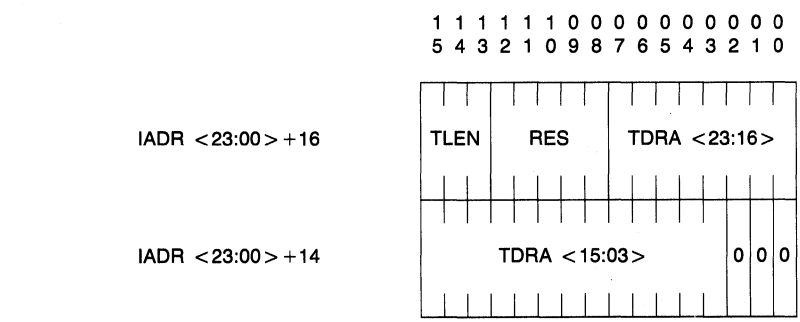
RLEN	NUMBER OF ENTRIES
0	1
1	2
2	4
3	8
4	16
5	32
6	64
7	128

RES
Bits 12:08
(Reserved)

RDRA
Bits 07:00 and 15:03
(Receive Descriptor Ring Address) Receive Descriptor Ring Address is the base address (lowest address) of the Receive Descriptor Ring.

RDRA
Bits 02:00
(Must Be Zeros) These bits are RDRA <02:00> and must be zeroes because the Receive Rings are aligned on quadword boundaries.

2.4.1.5 TRANSMIT DESCRIPTOR RING POINTER



TLEN
Bits 15:13
(Transmit Ring Length) Transmit Ring Length is the number of entries in the Transmit Ring expressed as a power of two.

TLEN	NUMBER OF ENTRIES
0	1
1	2
2	4
3	8
4	16
5	32
6	64
7	128

RES
Bits 12:08
(Reserved)

TDRA
Bits 07:00 and 15:03
(Transmit Descriptor Ring Address) This address is the base address (lowest address) of the Transmit Descriptor Ring.

Bits 02:00
(Must Be Zeros) These bits must be zeroes because the Transmit Rings are aligned on quadword boundaries.

2.5 BUFFER MANAGEMENT

Buffer Management is accomplished through message descriptors organized in ring structures in memory. Each message descriptor entry is four words long. There are two rings allocated for the LANCE:a Receive ring and a Transmit ring. The LANCE is capable of polling each ring for buffers either to empty or fill with packets to or from the channel. The LANCE is also capable of entering status information in the descriptor entry. When polling, LANCE is limited to looking one ahead of the descriptor entry with which it is currently working. The speed of the data stream restricts the receiver buffer size to a minimum of 64 bytes to avoid an overflow when chaining receive buffers. The location of the descriptor rings and their length are found in the initialization block, accessed during the initialization procedure by LANCE. Writing a "ONE" into the STRT bit of CSR0 will cause LANCE to start accessing the descriptor rings and enable it to send and receive packets. The LANCE communicates with a HOST device (probably a microprocessor) through the ring structures in memory. Each entry in the ring is either "owned" by LANCE or the HOST. There is an ownership bit (OWN) in the message descriptor entry. Mutual exclusion is accomplished by a protocol which states that each device can only relinquish ownership of the descriptor entry to the other device; it can never take ownership, and each device cannot change the state of any field in an entry after it has relinquished ownership. When chaining buffers, the minimum transmit buffer size is restricted to 100 bytes (to avoid mutual exclusion violations, which could occur following a collision). Otherwise, LANCE would access a buffer to which it had relinquished ownership (to reinitialize a transmission interrupted by a collision).

2.5.1 DESCRIPTOR RINGS

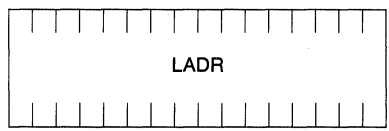
Each descriptor in a ring in memory is a 4 word entry. The following is the format of the receive and the transmit descriptors.

2.5.1.1 RECEIVE MESSAGE DESCRIPTOR ENTRY

2.5.1.1.1 RECEIVE MESSAGE DESCRIPTOR 0 (RMD0)

MEMORY ADDRESS: XXXXXXX0

1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
5	4	3	2	1	0	9	8	7	6	5	4	3	2	1	0



LADR
Bits 15:00
The Low Order 16 address bits of the buffer pointed to by this descriptor. LADR is written by the Host and unchanged by LANCE.

2.5.1.1.2 RECEIVE MESSAGE DESCRIPTOR 1 (RMD1)

MEMORY ADDRESS: XXXXXXX2

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
OWN	ERR	FRAM	OFLO	CRC	BUFF	STP	ENP	HADR							

OWN
Bit 15
This bit indicates that either the Host owns the descriptor entry (OWN = 0) or LANCE owns it (OWN = 1). The chip clears the OWN bit after filling the buffer pointed to by the descriptor entry. The Host sets the OWN bit after emptying the buffer. Once the LANCE or Host relinquishes ownership of a buffer, it may not change any field in the four words that comprise the descriptor entry.

ERR
Bit 14
(Error Summary) Error Summary is the "OR" of FRAM, OFLO, CRC or BUFF. ERR is set by LANCE when it releases the buffer and is cleared by the Host.

FRAM
Bit 13
(Framing Error) Framing Error indicates that the incoming packet contained both a non-integer multiple of eight (8) bits and a CRC error. In internal loopback, whenever a CRC error occurs, FRAM will always be set. FRAM is set by LANCE when it releases the buffer and is cleared by the Host.

OFLO
Bit 12
(Overflow) Overflow error indicates that the receiver has lost all or part of the incoming packet due to an inability to store the packet in a memory buffer before the internal SILO overflowed. OFLO is set by LANCE when it releases the buffer and is cleared by the Host.

CRC
Bit 11
CRC indicates that the receiver has detected a CRC error on the incoming packet. CRC is set by LANCE when it releases the buffer and is cleared by the Host.

BUFF
Bit 10
(Buffer Error) Buffer Error is set either when LANCE has utilized all its allocated buffers or if the next status is not acquired in time while data chaining a received packet. BUFF is set by LANCE when it releases the buffer and is cleared by the Host. If a Buffer Error occurs, an Overflow Error also occurs because LANCE tries to acquire the next buffer until the SILO overflows.

STP
Bit 09
(Start of Packet) Start of Packet indicates that this is the first buffer used by LANCE for this packet. It is used for data chaining buffers. STP is set by LANCE when it releases the buffer and is cleared by the Host.

ENP
Bit 08
(End of Packet) End of Packet indicates that this is the last buffer used by LANCE for this packet. It is used for data chaining buffers. If both STP and ENP were set, the packet would fit into one buffer and there was no data chaining. ENP is set by LANCE when it releases the buffer and is cleared by the Host.

HADR
Bits 07:00
The High Order 8 address bits of the buffer pointed to by this descriptor. This field is written by the Host and unchanged by LANCE.

2.5.1.1.3 RECEIVE MESSAGE DESCRIPTOR 2 (RMD2)

MEMORY ADDRESS: XXXXXXX4

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
1	1	1	1	BCNT											

Bits 15:12
(Must Be Ones) This field is written by the Host and unchanged by LANCE.

BCNT
Bits 11:00
(Buffer Byte Count) Buffer Byte Count is the length of the buffer pointed to by this descriptor expressed as a two's complement number. This field is written by the Host and unchanged by LANCE. The minimum buffer size is 64 bytes.

2.5.1.1.4 RECEIVE MESSAGE DESCRIPTOR 3 (RMD3)

MEMORY ADDRESS: XXXXXXX6

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RES				MCNT											

RES
Bits 15:12
(Reserved) Read as zeroes.

MCNT
Bits 11:00
(Message Byte Count) Message Byte Count is the length in bytes of the received message. MCNT is valid only when ERR is clear and ENP is set. MCNT is written by LANCE and is cleared by the Host. In data chaining, RMD3 is only written to after the last buffer status is updated. Only the status word is updated for intermediate buffers in the data chain.

2.5.1.2 TRANSMIT MESSAGE DESCRIPTOR ENTRY

2.5.1.2.1 TRANSMIT MESSAGE DESCRIPTOR 0 (TMD0)

MEMORY ADDRESS: XXXXXXX0

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
LADR															

LADR
Bits 15:00
The Low Order 16 address bits of the buffer pointed to by this descriptor. LADR is written by the Host and unchanged by LANCE.

2.5.1.2.2 TRANSMIT MESSAGE DESCRIPTOR 1 (TMD1)

MEMORY ADDRESS: XXXXXXX2

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
OWN	ERR	RES	MORE	ONE	DEF	STP	ENP	HADR							

OWN
Bit 15
This bit indicates that either the Host owns the descriptor entry (OWN = 0) or LANCE owns it (OWN = 1). The host sets the OWN bit after filling the buffer pointed to by the descriptor. LANCE clears the OWN bit after transmitting the contents of the buffer. Both the Host and LANCE must not alter a descriptor entry after it has relinquished ownership.

ERR
Bit 14
(Error Summary) Error Summary is the "OR" of LCOL, LCAR, UFLO or RTRY. ERR is set by LANCE when it releases the buffer and is cleared by the Host.

RES
Bit 13
(Reserved) LANCE will write this bit with a "0".

MORE
Bit 12
MORE indicates that more than one retry was needed to transmit a packet. MORE is set by LANCE when it releases the buffer and is cleared by the Host.

ONE
Bit 11
ONE indicates that exactly one retry was needed to transmit a packet. ONE is set by LANCE when it releases the buffer and is cleared by the Host. ONE is not valid if LCOL in TMD3 is set.

DEF
Bit 10
(Deferred) Deferred indicates that LANCE had to defer while trying to transmit a packet. This condition occurs when the channel is busy when LANCE is ready to transmit. DEFER is set by LANCE when it releases the buffer and is cleared by the Host.

STP
Bit 09
(Start of Packet) Start of Packet indicates that this is the first buffer to be used by LANCE for this packet. It is used for data chaining buffers. STP is set by the Host and is unchanged by LANCE.

ENP
Bit 08
(End of Packet) End of Packet indicates that this is the last buffer to be used by LANCE for this packet. It is used for data chaining buffers. If both STP and ENP are set, the packet fits into one buffer and there is no data chaining. ENP is set by the Host and is unchanged by LANCE.

HADR
Bits 07:00
The High Order 8 address bits of the buffer pointed to by this descriptor. This field is written by the Host and is unchanged by LANCE.

2.5.1.2.3 TRANSMIT MESSAGE DESCRIPTOR 2 (TMD2)

MEMORY ADDRESS: XXXXXXX4

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
1	1	1	1	BCNT											

ONES
Bits 15:12
(Must Be Ones) This field is set by the Host and unchanged by LANCE.

BCNT
Bits 11:00
(Buffer Byte Count) Buffer Byte Count is the usable length in bytes of the buffer pointed to by this descriptor expressed as a two's complement negative number. This is the number of bytes from this buffer that will be transmitted by LANCE. This field is written by the Host and unchanged by LANCE. The minimum buffer size is 100 bytes when chaining or 64 bytes when not chaining.

2.5.1.2.4 TRANSMIT MESSAGE DESCRIPTOR 3 (TMD3)

TMD3 is valid only if the ERR bit of TMD1 has been set by LANCE.

MEMORY ADDRESS: XXXXXXX6

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
BUFF	UFLO	RES	LCOL	LCAR	RTRY	TDR									

BUFF
Bit 15
(Buffer Error) Buffer Error is set by LANCE during transmission when LANCE does not find the ENP flag in the current buffer and does not own the next buffer. BUFF is set by LANCE and cleared by the Host. If a Buffer Error occurs, an Underflow Error will also occur because LANCE tries to read memory data until the SILO is empty. Buffer Error is valid only if UFLO is set.

UFLO
Bit 14
(Underflow Error) Underflow Error indicates that the transmitter has truncated a message due to data late from memory. UFLO indicates that owing to a lack of data from memory, the SILO has emptied before the end of the packet was reached. UFLO is set by LANCE and is cleared by the Host.

RES
Bit 13
Reserved bit. LANCE writes this bit with a "0".

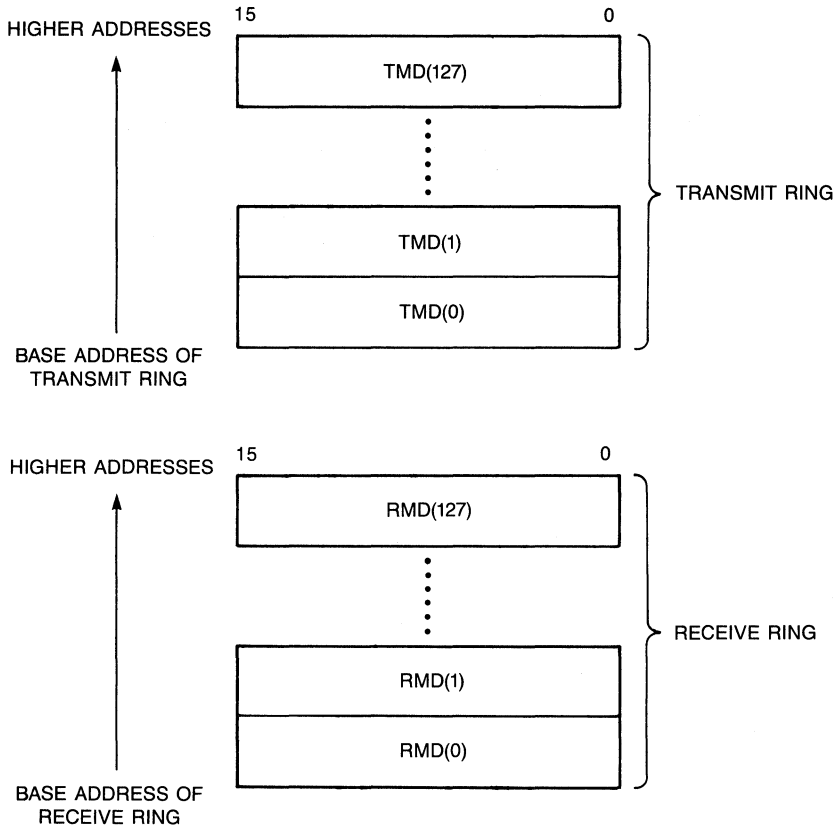
LCOL
Bit 12
(Late Collision) Late Collision indicates that a collision has occurred after the slot time of the channel has elapsed. LANCE does not retry on late collisions. LCOL is set by LANCE and is cleared by the Host.

LCAR
Bit 11
(Loss of Carrier) Loss of Carrier is set when the carrier presence (RENA) input to LANCE goes false during a LANCE-initiated transmission. LANCE does not retry upon Loss of Carrier. LCAR is set by LANCE and is cleared by the Host.

RTRY
Bit 10
(Retry Error) Retry Error indicates that the transmitter has failed in 16 attempts to successfully transmit a message due to repeated collisions on the medium. If DRTY = 1 in the MODE register, RTRY sets after 1 failed transmission attempt. RTRY is set by LANCE and is cleared by the Host.

TDR
Bits 09:00
(Time Domain Relectometry) Time Domain Reflectometry is an internal counter that counts system clocks from the start of a transmission to the occurrence of a collision. This value is useful in determining the approximate distance to a cable fault. The TDR value is written by LANCE and is valid only if RTRY is set.

DESCRIPTOR RINGS IN MEMORY



CHAPTER 3
FUNCTIONAL SPECIFICATIONS

3.0 INTRODUCTION

3.1 FUNCTIONAL DESCRIPTION

This section describes the logical elements used to implement the LANCE Ethernet Controller.

3.2 LOGIC

3.2.1 CLOCK

The LANCE has its clocks derived from a basic free running 10 MHz clock presented to the input pin TCLK. Refer to Section 4 for the clock specification. The microcycle is 200 nanoseconds long, or two basic clock ticks. The microcycle is the basic unit of time in the microsequencer and the control data path. Clock suppression is the act of selectively stretching the microcycle to allow a memory transfer to complete when the Chip is operating as a bus master. Clock suppression can only occur in those microcycles that contain an asserted USUPPRESS bit in the microword register.

3.2.2 MICROSEQUENCER

LANCE is controlled by an internal microprogram. Chained sequencing is used to advance the program address. Each microword contains the address of the next instruction plus any microbranch and trap information required in the program being executed. The microsequencer operates as a one level deep pipeline. As one micro-instruction is being executed, the next is being accessed. The basic microcycle is 200 nanoseconds long, but may be extended on 200 nanosecond boundaries to allow memory transfers to complete. During each microcycle, an address is formed to access the program store which is clocked into the microword register at the end of each cycle.

3.2.3 CONTROL DATA PATH

The Control Data Path contains the hardware necessary to build,control, and store the information required to do buffer management and to control the block transfers of data to and from the silo. The major components in this section of logic are a 24-bit adder, a data shuffler, a constant selector, and a static memory. In this memory resides twelve 24-bit Address Registers and ten 16 bit Status/ Byte Count Registers.

3.2.4 MESSAGE BYTE COUNT

The message byte count is contained in a 12-bit counter. The message byte count keeps track of the number of bytes entering or leaving the Silo under microprogram control for each transmission or reception. The value contained in the message byte count is written into memory through the MDR as part of the reception process. It is also used for the detection of runt packets on reception, and for the detection of babbling transmissions.

3.2.5 RING END FINDERS

The ring end finders, one each for the receive and transmit rings, determine whether the ring address pointers in the CDP RAM are at the end of the rings, and provide a microbranchable signal, which, when true, informs the microprogram to restore the pointers with the beginning address of the rings. The ring end finders are simply a pair of programmable modulo counters, the value of which is loaded at initialization time. The counters are independently incremented under microprogram control.

3.3 BUS CONTROL

3.3.1 BUS ADDRESS REGISTER

The Bus Address register (BA) is 27 bits wide. It is loaded directly from the Data Shuffler under control of a bit in the microword, ENA BA CLK, at the end of the microcycle. At the same time, the bus address is clocked, byte mask and read/write information, associated with the transfer is clocked into a three bit extension of the BA. Clocking of the BA initiates the bus transfer. The upper 8 bits of the BA drive A <23:16> directly. The lower sixteen bits of the BA are multiplexed onto DAL <15:00> during the address portion of the bus cycle when LANCE is the Bus Master. This is an internal register and is not directly addressable by the user.

3.3.2 MEMORY DATA REGISTER

The Memory Data register (MDR) buffers data transfers to and from the I/O bus. The MD is clocked at the end of the microcycle. It is enabled from the ENA MD CLK bit of the microword register. I/O bus data is synchronized to LANCE prior to loading the MDR.

3.3.3 BUS MASTER CONTROL

LANCE becomes a Bus Master for the purposes of acquiring data from the initialization block, buffer management, and the block move of data during the transmission or reception process. The Bus Master Control works in partnership with the microprogram. The microprogram is responsible for loading the BA and MDR for a write transaction, and loading the BA and unloading the MDR for a read transaction. Clocking the BA initiates the transfer. The microprogram also provides a clock suppress enable to stall selectively a microcycle until a memory transaction completes, thus providing synchronization between the microprogram and the Bus Master Control. During block transfer (DMA) of data, memory references overlap. LANCE performs up to 8 data transfers before relinquishing $\overline{\text{HOLD}}$. Refer to Chapter 4 for timing specifications.

3.3.4 MEMORY TIMEOUT

As a Bus Master, LANCE detects and recovers from non-existent memory errors. LANCE waits for a maximum of 25 microseconds for the assertion of $\overline{\text{READY}}$ after it asserts ALE. If LANCE does not receive $\overline{\text{READY}}$ within that time, it sets the MERR bit of CSR0, negates the RXON and TXON bits, and takes no further action unless either the $\overline{\text{RESET}}$ signal is asserted or the STOP bit of CSR0 is asserted.

3.3.5 BUS SLAVE CONTROL

The Bus Slave control is invoked when a memory transaction occurs and the $\overline{\text{CS}}$ pin is asserted. When this happens, it indicates that one of the four LANCE CSR's is being accessed. CSR0 provides visibility into LANCE and is accessed independently of the microprogram. CSR1 and CSR2 hold the address of the initialization block and are resident within the CDP RAM. Accessing CSR1 and CSR2 causes a microtrap for access. The microprogram issues the $\overline{\text{READY}}$ signal for CSR1 and CSR2. The Bus Slave Control independently returns $\overline{\text{READY}}$ for CSR0 and CSR3. CSR 3 allows the I/O pins to be programmed. CSR1, CSR2, and CSR3 are accessible only when the STOP bit of CSR0 is set. Refer to Chapter 4 for timing specifications.

3.3.6 DISCRETE USER APPARENT REGISTERS

Of the register ports and control and status registers, CSR0, CSR3, and RAP are read and written asynchronously from the parallel I/O bus. Refer to Section 2.3 for definitions of the register ports and control and status registers.

3.4 TRANSCEIVER DATA PATH

3.4.1 SERIAL DATA OUTPUT

Serial output data is presented at the TX Output pin by LANCE. The presence of the output

data stream is indicated by the assertion of the TENA level at the Output pin. TX and TENA are synchronous to the internal clock TCLK.

3.4.2 SERIAL DATA INPUT

Serial input data is presented to LANCE at the RX Input pin. The serial input data clock is presented at the RCLK Input pin. The presence of the input data stream is indicated by the assertion of the RENA at its Input pin. RX, RCLK, and RENA are asynchronous to the internal clock TCLK. RCLK is used by LANCE to clock in the input data stream. After the assertion of RENA, LANCE waits 800 nanoseconds before searching for the start bit. If LANCE detects a double ZERO prior to detecting a START bit, LANCE rejects the rest of the packet. Once the Start bit has been detected, LANCE frames the remaining bit stream into byte boundaries, synchronizes the bytes to the internal clock, and loads the Silo if not otherwise disabled.

3.4.3 SILO

The SILO provides buffer storage for the data being transferred between the parallel bus I/O pins and serial bus I/O pins. The capacity of the SILO is 48 bytes. The fall-through time of the SILO is 200 nanoseconds maximum. The SILO has the following capabilities:

1. SILO OPERATION - TRANSMISSION. Data is loaded into the SILO under microprogram control from the MDR. Data from the SILO goes to the serial output shift register.

2. SILO OPERATION - UNDERFLOW. Underflow occurs during Transmission when the output serial shift register requires data to continue an unbroken bit stream output, but data is not available at the output of the SILO, and the last data byte in the frame has been shifted out. Once the SILO has underflowed, the SILO locks out further reads and writes until cleared by the microprogram.

3. SILO OPERATION - RECEPTION. Data is loaded into the SILO from the serial input shift register during Reception. Data leaves the SILO under microprogram control. The destination is the MDR. Preamble is not loaded into the SILO.

4. SILO OPERATION - OVERFLOW. Overflow occurs during Reception when the SILO is filled and data needs to be transferred from the input serial shift register. Once the SILO has overflowed, the SILO locks out further reads and writes until cleared by the microprogram.

5. SILO OPERATION - RESTORE. During Reception, restoring the SILO refers to the action of discarding the 6 bytes of the destination address that have accumulated in the SILO after an address match has been tested and an address match has not occurred. The same action occurs if less than 6 bytes are received before the packet ends. Note that this is different from clearing the SILO since there may be residual data in the SILO from a previous reception which cannot be lost. During the Transmission process, restoring the SILO refers the action of discarding the accumulated Transmit bytes when bit stream transmission has not yet begun and the receiver becomes active.

6. SILO OPERATION - INDEXING. The SILO is capable of holding residual data from a received packet, and accepting data from a second packet. The SILO is able to mark the end of one packet and the beginning of another.

7. SILO OPERATION - CLEARING. The SILO is cleared as part of the recovery for overflow, underflow, and collision. SILO clearing is the action of flushing all data from the SILO unconditionally by clearing the address counters. The SILO is cleared by a discrete microprogram operation.

3.4.4 SILO - MEMORY BYTE ALIGNMENT

Memory buffers may begin and end on arbitrary byte boundaries. Parallel data is byte aligned between the SILO and the MDR. Byte alignment can be reversed by setting the Byte Swap (BSWP) bit in CSR3.

TRANSMISSION - WORD READ FROM EVEN MEMORY ADDRESS

BWSP = 0: SILO BYTE n gets MDR <07:00>
SILO BYTE n + 1 gets MDR <15:08>

BWSP = 1: SILO BYTE n gets MDR <15:08>
SILO BYTE n + 1 gets MDR <07:00>

TRANSMISSION - BYTE READ FROM EVEN MEMORY ADDRESS

BSWP = 0: SILO BYTE n gets MDR <07:00>

BSWP = 1: SILO BYTE n gets MDR <15:08>

TRANSMISSION - BYTE READ FROM ODD MEMORY ADDRESS

BWSP = 0: SILO BYTE n gets MDR <15:08>

BWSP = 1: SILO BYTE n gets MDR <07:00>

RECEPTION - WORD WRITE TO EVEN MEMORY ADDRESS

BSWP = 0: MDR <07:00> gets SILO BYTE n
MDR <15:08> gets SILO BYTE n + 1

BSWP = 1: MDR <15:08> gets SILO BYTE n
MDR <07:00> gets SILO BYTE n + 1

RECEPTION - BYTE WRITE TO EVEN MEMORY ADDRESS

BSWP = 0: MDR <07:00> gets SILO BYTE n
MDR <15:08> - don't care

BSWP = 1: MDR <15:08> gets SILO BYTE n
MDR <07:00> - don't care

RECEPTION - BYTE WRITE TO ODD MEMORY ADDRESS

BSWP = 0: MDR <07:00> - don't care
MDR <15:08> gets SILO BYTE n

BSWP = 1: MDR <15:08> - don't care
MDR <07:00> gets SILO BYTE n

3.4.5 CYCLIC REDUNDANCY CHECK

LANCE utilizes the 32-bit CRC function used in the Autodin-II network. Refer to the Ethernet Specification (section 6.2.4 Frame Check Sequence Field and Appendix C; CRC Implementation) for more detail. LANCE requirements for the CRC logic are the following:

1. TRANSMISSION - MODE <02> LOOP = 0, MODE <03> DTCRC = 0. LANCE calculates the CRC from the first bit following the Start bit to the last bit of the data field. The CRC value is inverted and appended onto the transmission in one unbroken bit stream.

2. RECEPTION - MODE <02> LOOP = 0. LANCE performs a check on the input bit stream from the first bit following the Start bit to the last bit in the frame. LANCE continually samples the state of the CRC check on framed byte boundaries, and, when the incoming bit stream stops, the last sample determines the state of the CRC error. Framing error (FRAM) is not reported if there is no CRC error.

3. LOOPBACK - MODE <02> LOOP = 1, MODE <03> DTRC = 0. LANCE generates and appends the CRC value to the outgoing bit stream as in Transmission but does not check the incoming bit stream.

4. LOOPBACK - MODE <02> LOOP = 1 MODE <03> DTRC = 1. LANCE performs the CRC check on the incoming bit stream as in Reception, but does not generate or append the CRC value to the outgoing bit stream.

3.5 TRANSMISSION

Serial transmission consists of sending an unbroken bit stream from the TX pin consisting of:

1. Preamble / Start bit: 64 alternating ONES and ZEROS terminating in two ONEs. The last ONE is the Start bit.

2. Data: The serialized byte stream from the Silo. Shifted out LSB first.

3. CRC: The inverted 32 bit polynomial calculated from the Data field. CRC is not transmitted if:

    1. Transmission of the Data field is truncated for any reason.

    2. CLSN becomes asserted any time during transmission.

    3. LANCE is in Loopback mode and CRC transmission is disabled (MODE <03> = 1 and MODE <02> = 1).

    4. Mode <03> DTCRC = 1 in a normal transmission mode.

Transmission is indicated at the I/O pin by the assertion of TENA with the first bit of the preamble and the negation of TENA after the last transmitted bit. LANCE starts transmitting the preamble when the following are satisfied.

1. There is at least one byte of data to be transmitted in the Silo.

2. The inter-packet delay has elapsed.

3. The backoff interval has elapsed, if a retransmission.

3.5.1 INTERPACKET DELAY

The interpacket delay is 9.6 to 10.6 microseconds including synchronization. The interpacket delay interval begins after the negation of the RENA signal, LANCE continuously monitors the RENA input pin to monitor or generate an interpacket delay. If LANCE is about to transmit (about to assert the TENA output pin) and RENA is asserted, the chip will not assert TENA until RENA has negated and the interpacket delay has elapsed. Whenever LANCE is about to transmit and is waiting for the interpacket delay to elapse, it will begin transmission immediately after the interpacket delay interval, independent of the state of RENA.

3.5.2 COLLISION DETECTION AND COLLISION JAM

Collisions are detected by monitoring the CLSN input pin. If CLSN becomes asserted during a Frame Transmission, TENA will remain asserted for at least 32 (but not more than 48) additional bit times (including CLSN synchronization). This additional transmission after collision

is referred to as COLLISION JAM. The bit pattern present at the TX output pin is unspecified during COLLISION JAM, but it may not be the 32 bit CRC value corresponding to the (partial) packet transmitted prior to the COLLISION JAM.

If CLSN becomes asserted during the reception of a packet, this reception is immediately terminated. Depending on the timing of collision detection, the following will occur. A collision that occurs within 6 byte times (4.8 microseconds) will result in the packet being rejected because of an address mismatch with the silo write pointer being reset. A collision that occurs within 64 byte times (51.2 microseconds) will result in the packet being rejected since it is a runt packet. A collision that occurs after 64 byte times will result in a truncated packet being written to the memory buffer with the CRC error bit being set in the Status Word of the Receive Ring.

3.5.3 COLLISION BACKOFF

When a transmission attempt has been terminated due to the assertion of CLSN, it is retried by LANCE up to 15 times until successful, or something else aborts the process (memory timeout). The scheduling of the retransmissions is determined by a controlled randomized process called "truncated binary exponential backoff." Upon the negation of the COLLISION JAM interval, LANCE calculates a delay before retransmitting. The delay is an integral multiple of the SLOT TIME. The SLOT TIME is 512 bit times. The number of SLOT TIMEs to delay before the nth retransmission attempt is chosen as a uniformly distributed random integer in the range:

$$0 \leq r < 2^k \qquad \text{where } k = \min(n,10)$$

If all 16 attempts fail, LANCE sets the RTRY bit in the current Transmit Message Descriptor 3 in memory, and steps over the current transmit buffer.

3.5.4 COLLISION - MICROCODE INTERACTION

The microprogram uses the time provided by COLLISION JAM, INTERPACKET DELAY, and the backoff interval to restore the address and byte counts and start loading the Silo in anticipation of retransmission. It is important that LANCE be ready to transmit when the backoff interval elapses in order to utilize the channel properly.

3.5.5 TIME DOMAIN REFLECTOMETRY

LANCE contains a time domain reflectometry counter. The TDR counter is ten bits wide. It counts at a 10 MHz rate. It is cleared by the microprogram and counts upon the assertion of RENA during transmission. Counting ceases if CLSN becomes true. The counter does not wrap around, once all ONEs are reached in the counter, that value is held until cleared. The value in the TDR is written into memory by the microprogram through the MDR. TDR is used to determine the location of suspected cable faults. Transfer from TDR counter into MDR register occurs only if RTRY is set. Normally, when RTRY is not set, the value of TDR will be all zeros.

3.5.6 HEARTBEAT

During the INTERPACKET DELAY following the negation of TENA, the CLSN input is asserted by some Version 1 and all Version 2 transceivers as a self-test. If two microseconds of the INTERPACKET DELAY elapse without CLSN having been asserted, LANCE will set the CERR bit in CSR0 (bit <13>). This function is gated off in the internal loopback mode.

3.6 RECEPTION

Serial reception consists of receiving an unbroken bit stream on the RX I/O pin consisting of:

1. Preamble / Start bit: Two ONES occurring a minimum of 8 bit times after the assertion of RENA. The last ONE is the Start bit.

2. Destination Address: The 48 bits (6 bytes) following the Start bit.

3. Data: The serialized byte stream following the Destination Address. The last four complete bytes of data are the CRC. The Destination Address and the Data are framed into bytes and enter the Silo.

Reception is indicated at the I/O pin by the assertion of RENA and the presence of clock on RCLK while TENA is deasserted.

3.6.1 STATION ADDRESS DETECTION

The station address detect logic checks the destination address of the incoming packet to determine if the packet is addressed to this node. A packet will be accepted if at least one of the following is true:

1. Physical address match: The destination address of the packet exactly matches the physical address of the node.

2. Logical address match: The destination address of the packet is hashed using the CRC. The hash function is used to determine a logical address match.

3. Promiscuous mode: The node accepts all packets regardless of the destination address.

4. Broadcast Detection: The destination address of the packet is the Broadcast Address; all ones.

3.6.1.1 PHYSICAL ADDRESS REGISTER

The physical address register is 48 bits wide and contains the physical address of LANCE. The microprogram loads the physical address from the initialization block through three sequential memory transactions. If the first bit following the Start bit is a ZERO, LANCE will perform a physical address compare. The following 47 bits are compared, bit for bit, for an exact match. If they do not match, LANCE will reject the packet. Bit <00> of the physical address register corresponds to the first bit of the destination address field, and bit <47> of the physical address register corresponds to the last bit of the destination address field.

3.6.1.2 LOGICAL ADDRESS FILTER REGISTER

The logical address filter register is 64 bits wide. The microprogram loads the logical address filter from the initialization block through four sequential memory transactions. If the first bit following the Start bit is a ONE, LANCE will perform a logical address compare. After the last bit of the destination address is clocked into the CRC check logic, the value of CRC 31:26 is used as an index into the logical address filter register. If the bit selected in the register is not a ONE, the chip will reject the packet.

3.6.1.3 PROMISCUOUS MODE

If MODE <15> PROM = 1, LANCE will accept all packets, regardless of the destination address.

3.6.1.4 BROADCAST ADDRESS DETECTION

LANCE will always accept all packets sent to the Broadcast Address of all ones.

3.6.2 RUNT PACKET FILTRATION

If, after loading a buffer, the message byte count is less than 64 bytes, LANCE does not update the ring descriptor entry that pointed to the buffer. Instead LANCE retains the buffer information for use with the next incoming packet. An incoming message must be greater than 64 bytes to be considered a valid packet.

3.7 LOOPBACK

The normal operation of LANCE is as a half duplex device. However, to provide an on-line operational test of LANCE, a pseudo-full duplex mode is provided. In this mode, simultaneous transmission and reception of a loopback packet are enabled with the following constraints:

1. The packet length must be no longer than 32 bytes, exclusive of the CRC.

2. Serial transmission does not begin until the Silo contains the entire output packet.

3. Moving the input packet from the Silo to the memory does not begin until the serial input bit stream terminates.

4. CRC may be generated and appended to the output serial bit stream or may be checked on the input serial bit stream, but not both in the same transaction.

Loopback is controlled by bits <06,03:02> INTL, DTCR, and LOOP of the MODE register. Refer to Section 2.4.1.1 for detailed operation of this register.

3.8 MICROPROGRAM OVERVIEW

3.8.1 SWITCH ROUTINE

Upon power-up, the microprogram finds itself in a routine to evaluate the INIT, STRT, and STOP bits of CSR0. INIT and STRT are cleared and STOP is set by the hardware by $\overline{\text{RESET}}$. Setting either INIT or STRT through an I/O transfer to CSR0 clears STOP. Setting STOP through an I/O transfer clears INIT and STRT. After seeing STOP cleared, the microprogram tests the state of INIT. If set, it branches to the initialization routine, returns, and tests the state of STRT. If INIT is clear and STRT is set, the microprogram goes on to the Polling routine without going to the Initialization routine. If, while the STOP bit is set, an I/O transfer to CSR1 or CSR2 occurs, the microprogram traps to the CSR service routine.

3.8.2 INITIALIZATION ROUTINE

This routine is entered only from the switch routine upon the setting of the INIT bit. Its function is to load LANCE with the data from the initialization block in memory. The routine accesses the initialization block through the address loaded into the CDP RAM by a trap to CSR1 and CSR2 that should have occurred prior to the INIT bit being set. This routine simply sequentially reads the initialization block and stores the information away in the appropriate elements of LANCE. When done, the microcode returns to the switch routine.

3.8.3 POLLING ROUTINE

This routine is entered from:

1. The switch routine upon the setting of the STRT bit.

2. The receive routine after a packet has been received.

3. The transmit routine after a packet has been transmitted.

4. The transmit routine after a Transmission Abort occurs.

5. The memory error trap routine after the trap is serviced.

The routine begins by testing to see if the receiver is disabled, and, if not, tests the current receiver buffer ownership bit to see if it owns a buffer. If LANCE had not acquired a buffer previously, the microprogram goes to the receiver polling routine to acquire one. When the microprogram returns from the receive polling routine, or if LANCE had acquired a buffer previously, it tests

to see if the transmitter is disabled, and, if not, goes to the transmit polling routine to test if there is a buffer to be transmitted. When the microprogram returns from the transmit polling routine, the microprogram enters a timing loop, and repeats the routine upon timeout (above 1.6 ms). Setting the TDMD bit in CSR0 overrides the timing loop. This forces the microprogram to fall through the wait loop. The TDMD bit is cleared immediately after leaving the wait loop. Therefore, to be effective, TDMD should be set after a buffer has been inserted on the transmit ring.

During this routine, should the receiver become active, the microprogram traps to the receive routine.

3.8.4 RECEIVE POLLING ROUTINE

This routine is entered if the receiver is enabled, and LANCE needs a free buffer. The routine begins by the microprogram performing a memory transaction to get a buffer status word from the receive descriptor ring. After acquiring the word, it tests to see if it owns the buffer. If not, the microprogram returns to the polling routine. If it does, the microprogram proceeds to acquire two additional words to obtain the rest of the buffer address and byte count. It then returns to the polling routine with the three words stored in the CDP RAM. The trap to the receive routine is enabled in this routine.

3.8.5 RECEIVE ROUTINE

The receive routine is entered when the receiver is enabled and an incoming packet address has been detected as a match. The routine is divided into three sections of code, an initialization section, a buffer lookahead section, and a descriptor update section. In the initialization section, the microprogram first tests to see if it has acquired a free buffer. If not, it makes one attempt to get the status, address, and byte count from memory. LANCE backs up the address and byte count in the CDP RAM for runt packet recovery, and proceeds to the lookahead section. In the lookahead section, the microprogram tries to acquire an additional buffer by memory transactions with the ring buffer descriptors. If it acquires one, it stores it in the CDP RAM, and waits for byte count overflow or the frame to terminate. In this section the receive DMA trap is enabled. The descriptor update section is entered when byte count overflow has occurred or the message has ended. The code section begins with a test to determine if the message has completed, if data chaining needs to be done, or if a runt packet has been encountered. If a runt packet has been encountered, the microprogram restores the address and byte count and goes to the polling routine. If the incoming message has terminated, the microprogram writes the message length into the ring descriptor entry, writes the status information into the ring descriptor entry, puts the next buffer status information it acquired in the lookahead code in the current buffer status area of the CDP RAM, advances the ring pointer, and goes to polling. If the byte count has overflowed, but the message has not ended, chaining is required. The microprogram releases the buffer by writing the status information into the ring descriptor entry, puts the next buffer status information it acquired in the lookahead code in the current buffer status area of the CDP RAM, advances the ring pointer, and returns to the lookahead code section.

3.8.6 RECEIVE DMA ROUTINE

The Receive DMA routine is entered whenever there are 16 or more bytes of data in the SILO for transfer to memory during receive. The routine is also entered when there are less than 16 bytes in the SILO and the receiver has gone inactive. This is to allow the SILO to empty at the end of reception. Once entered, the Receive DMA routine transfers 16 bytes of data to memory by doing 8 word transfers. These transfers are done on a single memory bus acquisition. This means that LANCE will arbitrate through the HOLD-HOLD ACKNOWLEDGE sequence and then keep HOLD asserted for the duration of 8 transfers. The READY signal from the bus slave device controls the individual word transfers.

If the memory buffer starts on an odd address boundary, the first transfer is 1 byte rather than 1 word (2 bytes). This routine is also used to transfer less than 16 bytes at the end of a reception depending upon the packet size, buffer addresses and data chaining.

NOTE:
DMA (direct memory access) is performed each time LANCE initiates a memory transfer. However, in this document, DMA refers only to those transfers between the SILO and Bus memory.

This routine is entered through a microtrap in the lookahead section of the receive routine. The function of the routine is to move data out of the SILO to local memory. The trap is active when there are 16 or more bytes of data in the SILO and SILO overflow has not occurred or when the incoming message has terminated with data in the SILO. The routine pipelines the data through the Memory Data register while the address and byte counts are incremented in the control data path. A memory timeout will cause a trap. The routine is exited through the URETURN register to the code section that originally trapped to this routine.

3.8.7 TRANSMIT POLLING ROUTINE

The transmit polling routine is entered from the polling routine to determine if a message has been scheduled on the transmit descriptor ring. The routine begins by testing the status word of the ring descriptor entry. The routine tests the ownership of the ring buffer by reading the status word in the ring descriptor. If LANCE does not own the buffer, the microprogram returns to the polling routine. If it does own the buffer, this indicates that a message is to be transmitted, and the microprogram performs memory transactions to acquire and store the address and byte count of the buffer in the CDP RAM. It then goes to the transmit routine to allow transmission of the buffer. The receive active trap is enabled during this routine to allow for processing of an incoming packet and termination of the transmit process.

3.8.8 TRANSMIT ROUTINE

The transmit routine is entered from the transmit polling routine when the microcode finds a buffer that it owns, indicating that a message is scheduled to be transmitted. The routine is divided into three sections of code: an initialization section, a buffer lookahead section, and a descriptor update section. Upon entering the initialization section, the first thing the microprogram does is back up the buffer address and byte count in the event of a retry. It then enables the DMA engine to start filling the SILO and send the preamble. It then enters a wait loop until the transmitter is actually sending the bit stream. It then proceeds to the lookahead section. In the lookahead section, the microprogram tests to determine if the current buffer it is transmitting has been marked with the end of packet flag. If so, data chaining is not required. The microprogram enters a wait loop for byte count overflow. If the end of packet flag is not set, the microprogram attempts to obtain the next buffer descriptor status, address, and byte count before entering the wait loop. When byte count overflow does occur, the microprogram enters the descriptor update section. In the descriptor update section, the microprogram first determines if an error has occurred or, simply, if data chaining must be performed. If an error needs to be reported, an error status word is written into the ring descriptor prior to writing the status word containing the "OWN" bit which releases the buffer. If no error is to be reported, the single word containing the "OWN" bit is written. The microprogram returns to the polling section if the "ENP" flag is found. Otherwise the microprogram returns to the lookahead section.

3.8.9 TRANSMIT DMA ROUTINE

This routine is entered through a microtrap in the lookahead section of the transmit routine. The function of the routine is to move data out of local memory into the SILO. The trap is active when there are 16 or more free locations in the SILO and SILO underflow has not occurred. The routine pipelines the data through the Memory Data register while the address and byte counts are incremented in the Control Data Path. A memory timeout will cause a trap. After a maximum of eight (8) words have been transferred into the SILO, the routine is exited through the URETURN register to the code section that originally trapped to this routine.

3.8.10 COLLISION TRAP ROUTINE

This routine is entered when a collision has been detected while the transmitter is active. The buffer address and byte counts are restored and the microprogram proceeds to the transmit routine to reschedule the transmission. This is the rule if less than 15 retransmissions have occurred. If 15 retransmissions have occurred, the microprogram goes instead to the error reporting code in the descriptor update section.

3.8.11 CSR TRAP ROUTINE

The CSR trap routine is entered only during the switch routine when the STOP bit of CSR0 is set. The function of the routine is to allow the access of CSR1 and CSR2 through an I/O transaction. The routine determines which CSR is being accessed, read or written, moves the data between the MDR and the CDP RAM, and generates a $\overline{\text{READY}}$ signal. The routine is exited through the URETURN register.

3.8.12 MEMORY TIMEOUT TRAP ROUTINE

This trap is invoked whenever a memory transfer times out. The routine sets the STOP bit of CSR0 and returns the microprogram to the start of the switch routine.

3.8.13 RETRY TRAP ROUTINE

This routine is entered when a collision has been detected. The buffer address pointer is restored and the SILO is cleared to restore the READ and WRITE pointers. If there was a TX error, it indicates that 15 retransmissions have occurred (16 total attempts) or that the Disable Retry bit (DRTY) is set in the Mode register. The microprogram then writes the status into the transmit descriptor ring.

If there was no TX error, the byte count is restored and the microprogram returns to the start of the transmit routine to attempt another transmission.

3.8.14 DATA CHAIN

If Byte Count Equal 0 becomes true, it indicates that the receive buffer is full and the packet is not yet finished, which is the data chain case. The microprogram updates the receive status in the descriptor ring. It then checks the next OWN bit. If next OWN is false, which would be the case if there was only one buffer or if there was more than one buffer but the chip did not own the next one, the microprogram waits for RX Active to go false. This indicates that no more data is arriving from the Ethernet. When RX Active goes false, the current RX OWN bit is cleared because the ring entry has just been used for the updated receive status. The SILO is then cleared to restore the READ and WRITE pointers, RX Clear is issued and the microprogram returns to the Polling routine.

If LANCE owned the next buffer, the current receive buffer parameters in the CDP Ram are updated from the next receive buffer parameters that had previously been loaded into the CDP Ram. The microprogram then checks for the end of the ring and updates the address pointers accordingly. The microprogram then goes through the receive buffer lookahead microprogram once to try to acquire another receive buffer if one is available. The microprogram finally returns to the wait loop until either RX Done, SILO overflow or receive buffer overflow becomes true. When RX Done or SILO Overflow occurs, the microcode sets the RINT bit in CSR0. The flow from this point is the same as described elsewhere.

CHAPTER 4
ELECTRICAL SPECIFICATIONS

4.0 ELECTRICAL SPECIFICATIONS

This chapter provides tabular presentations for Absolute Maximum Ratings, DC Characteristics, Capacitance, and AC Timing Specifications. In addition, illustrations are provided for an Output Load Diagram and for Serial Link, Bus Master, and LANCE Bus Slave Timing Diagrams.

ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias ..... −25°C to +100°C
Storage Temperature ..... −65°C to +150°C
Voltage on Any Pin with Respect to Ground ..... −.7 V to +7 V
Power Dissipation ..... 2.0 W

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

T_A=0°C to 70°C, V_{CC} = +5 V ± 5% unless otherwise specified.

SYMBOL	PARAMETER	MIN	MAX	UNITS
V_{IL}		−0.5	+0.8	V
V_{IH}		+2.0	V_{CC} +0.5	V
V_{OL}	@ I_{OL} = 3.2 mA		+0.5	V
V_{OH}	@ I_{OH} = −0.4 mA	+2.4		V
I_{IL}	@ V_{in} = 0.4 to V_{CC}		±10	μA

CAPACITANCE

F=1 MHz

SYMBOL	PARAMETER	MIN	MAX	UNITS
C_{IN}			10	pf
C_{OUT}			10	pf
C_{IO}			20	pf

AC TIMING SPECIFICATIONS

T_A = 0°C to 70°C, V_{CC} = +5 V± 5% unless otherwise specified.

NO.	SIGNAL	SYMBOL	PARAMETER	TEST CONDITIOS	MIN (ns)	TYP (ns)	MAX (ns)
1	TCLK	T_{TCT}	TCLK period		99		101
2	TCLK	T_{TCL}	TCLK low time		45		55
3	TCLK	T_{TCH}	TCLK high time		45		55
4	TCLK	T_{TCR}	Rise time of TCLK		0		8
5	TCLK	T_{TCF}	Fall time of TCLK		0		8
6	TENA	T_{TEP}	TENA propagation delay after the rising edge of TCLK	CL = 50 pf			75
7	TENA	T_{TEH}	TENA hold time after the rising edge of TCLK	CL = 50 pf	5		

AC TIMING SPECIFICATIONS (CONTINUED)

T_A = 0°C to 70°C, V_{CC} = +5 V± 5% unless otherwise specified.

NO.	SIGNAL	SYMBOL	PARAMETER	TEST CONDITIONS	MIN (ns)	TYP (ns)	MAX (ns)
8	TX	T_{TDP}	TX data propagation delay after the rising edge of TCLK	CL=50 pf			75
9	TX	T_{TDH}	TX data hold time after the rising edge of TCLK	CL=50 pf	5		
10	RCLK	T_{RCT}	RCLK period		85		118
11	RCLK	T_{RCH}	RCLK high time		38		
12	RCLK	T_{RCL}	RCLK low time		38		
13	RCLK	T_{RCR}	Rise time of RCLK		0		8
14	RCLK	T_{RCF}	Fall time of RCLK		0		8
15	RX	T_{RDR}	RX data rise time		0		8
16	RX	T_{RDF}	RX data fall time		0		8
17	RX	T_{RDH}	RX data hold time (RCLK to RX data change)		5		
18	RX (See note)	T_{RDS}	RX data setup time (RX data stable to the rising edge of RCLK)		See Note		
19	RENA	T_{DPL}	RENA low time		120		
20	RENA	T_{RENH}	RENA Hold time after rising edge of RCLK		40		
21	CLSN	T_{CPH}	CLSN high time		80		
22	A/DAL	T_{DOFF}	Bus master driver disable after rising edge of $\overline{HOLD}$		0		50
23	A/DAL	T_{DON}	Bus master driver enable after falling edge of $\overline{HLDA}$		0		150
24	$\overline{HLDA}$	T_{HHA}	Delay to falling edge of $\overline{HLDA}$ from falling edge of $\overline{HOLD}$ (Bus master)		0		
25	$\overline{RESET}$	T_{RW}	RESET pulse width low		200		
26	A/DAL	T_{CYCLE}	Read/write, address/data cycle time		600		
27	A	T_{XAS}	Address setup time to the falling edge of ALE		75		
28	A	T_{XAH}	Address hold time after the rising edge of $\overline{DAS}$		35		
29	DAL	T_{AS}	Address setup time to the falling edge of ALE		75		
30	DAL	T_{AH}	Address hold time after the falling edge of ALE		35		
31	DAL	T_{RDAS}	Data setup time to the rising edge of $\overline{DAS}$ (Bus master read)		50		

NOTE: T_{RDS} (min) = T_{RCT} −25ns i.e. T_{RCT} = 100ns, then T_{RDS} (min) = 75 ns.

AC TIMING SPECIFICATIONS (CONTINUED)

T_A = 0°C to 70°C, V_{CC} = +5 V± 5% unless otherwise specified.

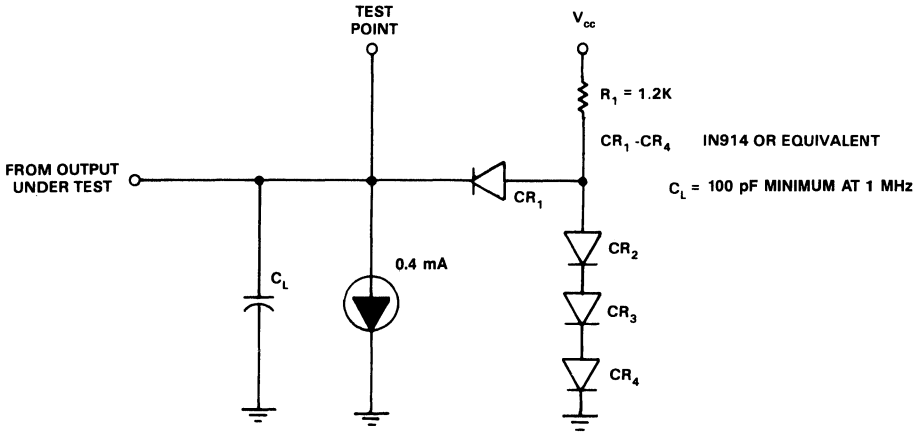
NO.	SIGNAL	SYMBOL	PARAMETER	TEST CONDITIONS	MIN (ns)	TYP (ns)	MAX (ns)
32	DAL	T_{RDAH}	Data hold time after the rising edge of $\overline{DAS}$ (Bus master read)		0		
33	DAL	T_{DDAS}	Data setup time to the falling edge of $\overline{DAS}$ (Bus master write)		0		
34	DAL	T_{WDS}	Data setup time to the rising edge of $\overline{DAS}$ (Bus master write)		200		
35	DAL	T_{WDH}	Data hold time after the rising edge of $\overline{DAS}$ (Bus slave read)		35		
36	DAL	T_{SDO1}	Data driver delay after the falling edge of $\overline{DAS}$ (Bus slave read)	(CSR 0,3, RAP)		400	
37	DAL	T_{SDO2}	Data driver delay after the falling edge of $\overline{DAS}$ (Bus slave read)	(CSR 1,2)		1200	
38	DAL	T_{SRDH}	Data hold time after the rising edge of $\overline{DAS}$ (Bus slave read)		0		35
39	DAL	T_{SWDH}	Data setup time to the falling edge of $\overline{DAS}$ (Bus slave write)		0		
40	DAL	T_{SWDS}	Data setup time to the falling edge of $\overline{DAS}$ (Bus slave write)		0		
41	ALE	T_{ALEW}	ALE width high		120		150
42	ALE	T_{DALE}	Delay from rising edge of $\overline{DAS}$ to the rising edge of ALE		70		
43	$\overline{DAS}$	T_{DSW}	$\overline{DAS}$ width low		200		
44	$\overline{DAS}$	T_{ADAS}	Delay from the falling edge of ALE to the falling edge of $\overline{DAS}$		80		130
45	$\overline{DAS}$	T_{RIDF}	Delay from the rising edge of $\overline{DALO}$ to the falling edge of $\overline{DAS}$ (BUS master read)		15		
46	$\overline{DAS}$	T_{RDYS}	Delay from the falling edge of $\overline{READY}$ to the rising edge of $\overline{DAS}$	Taryd= 300 ns	75		250
47	$\overline{DALI}$	T_{ROIF}	Delay from the rising edge of $\overline{DALO}$ to the falling edge of $\overline{DALI}$ (Bus master read)		15		
48	$\overline{DALI}$	T_{RIS}	$\overline{DALI}$ setup time to the rising edge of $\overline{DAS}$(Bus master read)		135		
49	$\overline{DALI}$	T_{RIH}	$\overline{DALI}$ hold time after the rising edge of $\overline{DAS}$ (Bus master read)		0		
50	$\overline{DALI}$	T_{RIOF}	Delay from the rising edge of $\overline{DALI}$ to the falling edge of $\overline{DALO}$ (Bus master read)		55		
51	$\overline{DALO}$	T_{OS}	$\overline{DALO}$ setup time to the falling edge of ALE (Bus master read)		110		
52	$\overline{DALO}$	T_{ROH}	$\overline{DALO}$ hold time after the falling edge of ALE (Bus master read)		35		
53	$\overline{DALO}$	T_{WDSI}	Delay from the rising edge of $\overline{DAS}$ to the rising edge of $\overline{DALO}$ (Bus master write)		35		

AC TIMING SPECIFICATIONS (CONTINUED)
T_A = 0°C to 70°C, V_{CC} = +5 V± 5% unless otherwise specified.

NO.	SIGNAL	SYMBOL	PARAMETER	TEST CONDITIONS	MIN (ns)	TYP (ns)	MAX (ns)
54	$\overline{CS}$	T_{CSH}	$\overline{CS}$ hold time after the rising edge of $\overline{DAS}$ (Bus slave)		0		
55	$\overline{CS}$	T_{CSS}	$\overline{CS}$ setup time to the falling edge of $\overline{DAS}$ (Bus slave)		0		
56	ADR	T_{SAH}	$\overline{ADR}$ hold time after the rising edge of $\overline{DAS}$ (Bus slave)		0		
57	ADR	T_{SAS}	$\overline{ADR}$ setup time to the falling edge of $\overline{DAS}$ (Bus slave)		0		
58	$\overline{READY}$	T_{ARYD}	Delay from the falling edge of ALE to the falling edge of $\overline{READY}$ to insure a minimum bus cycle time (600 ns)				80
59	$\overline{READY}$	T_{SRDS}	Data setup time to the falling edge of $\overline{READY}$ (Bus slave read)		75		
60	$\overline{READY}$	T_{RDYH}	$\overline{READY}$ hold time after the rising edge of $\overline{DAS}$ (Bus master)		0		
61	$\overline{READY}$	T_{SRO1}	$\overline{READY}$ driver turn on after the falling edge of $\overline{DAS}$ (Bus slave)	(CSR 0,3, RAP)		600	
62	$\overline{READY}$	T_{SRO2}	$\overline{READY}$ driver turn on after the falling edge of $\overline{DAS}$ (Bus slave)	(CSR 1,2)		1400	
63	$\overline{READY}$	T_{SRYH}	$\overline{READY}$ hold time after the rising edge of $\overline{DAS}$ (Bus slave)		0		35
64	READ	T_{SRH}	$\overline{READ}$ hold time after the rising edge of $\overline{DAS}$ (Bus slave)		0		
65	READ	T_{SRS}	$\overline{READ}$ setup time to the falling edge of $\overline{DAS}$ (Bus slave)		0		

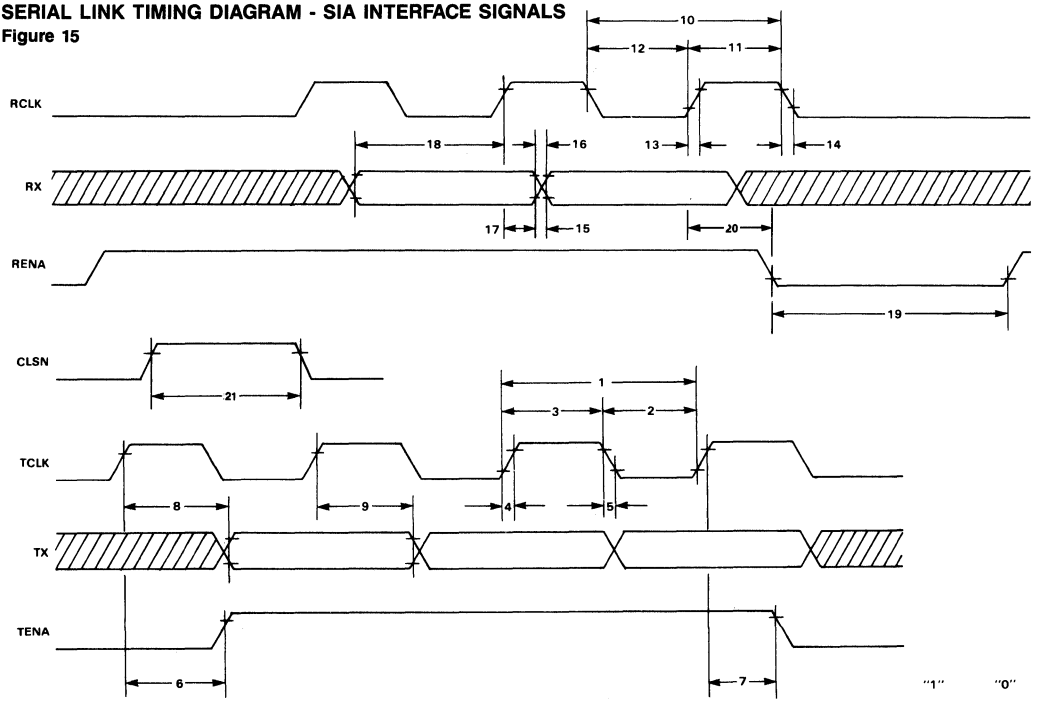
OUTPUT LOAD DIAGRAM

Figure 14



SERIAL LINK TIMING DIAGRAM - SIA INTERFACE SIGNALS

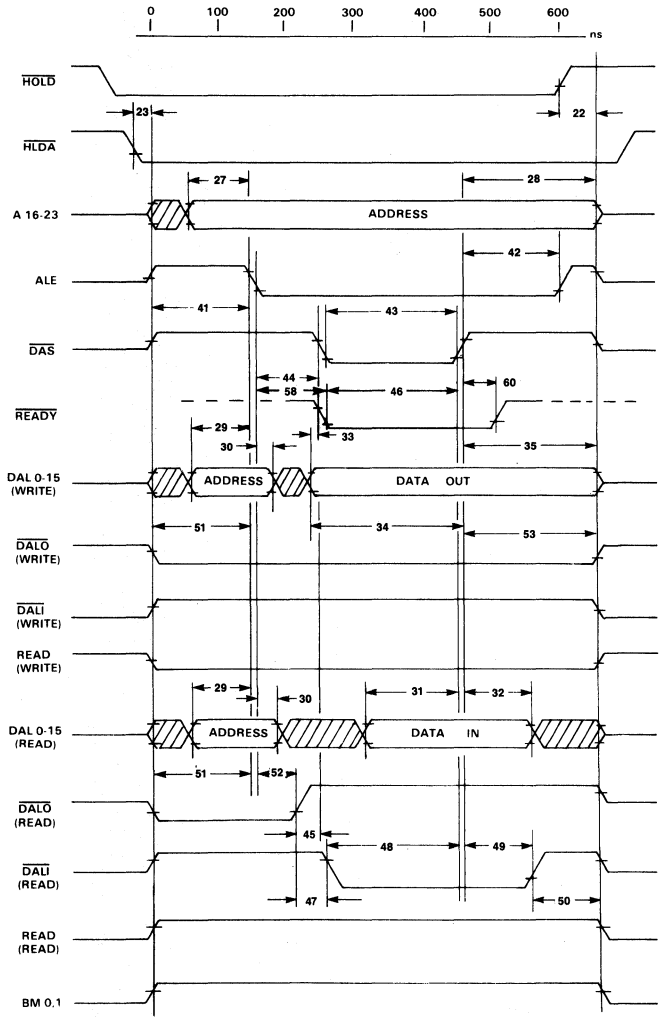
Figure 15



Timing measurements are made at the following voltages, unless otherwise specified:

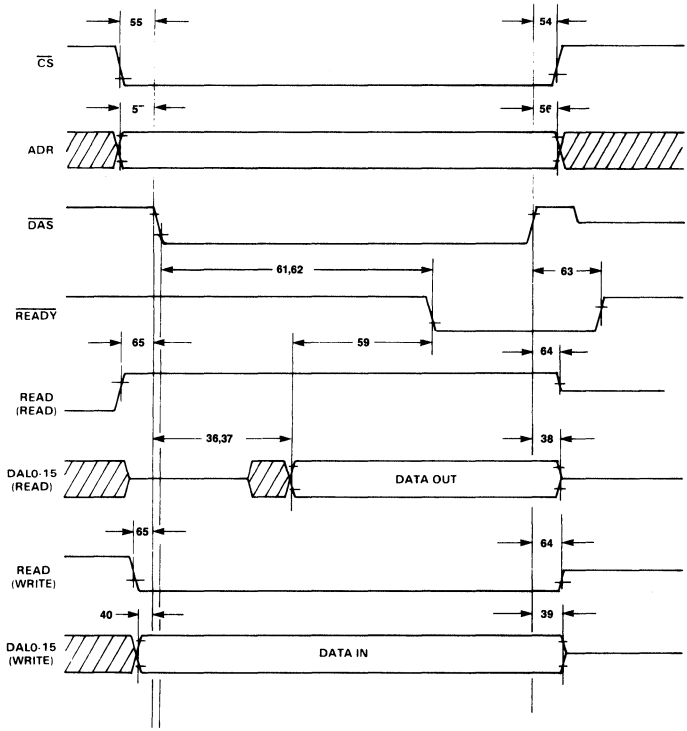
	"1"	"0"
OUTPUT	2.0 V	0.8 V
INPUT	2.0 V	0.8V
FLOAT	V	0.5 V

BUS MASTER TIMING DIAGRAM
Figure 16



NOTE:
The Bus Master cycle time will increase from a minimum of 600 ns in 100 ns steps until the slave device returns $\overline{\text{READY}}$.

LANCE BUS SLAVE TIMING DIAGRAM
Figure 17



APPLICATION
NOTE

MK68590 (LANCE™) INTERFACE TO MK68000

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

1.0 INTRODUCTION

The LANCE™ Application Note describes the basic hardware and software needed to interface the MK68590, Local Area Network Controller for Ethernet (LANCE), to the MK68000, Mostek's 16/32 microprocessor. It can be used as a "cookbook" for designing the basic hardware and software needed for a LANCE-68000 interface, but is actually more useful as a design guide.

This publication contains seven sections in addition to this introduction. Section two is the Ethernet Primer, which contains background material and basic concepts involved in Ethernet communication. Section three defines terms used throughout the Application Note. Section four is an overview of the Local Area Network Controller for Ethernet (LANCE) chip. Section five is the Ethernet Node overview, listing design requirements for an intelligent Ethernet node. It deals with the block level concepts of both hardware and software. Section six is the Hardware Description. It deals with the basic hardware requirements and includes both block diagrams and schematics. Section seven describes the software used in the LANCE-MK68000 interface. This section includes flowcharts, assembly code, and a step-by-step explanation of the software. The eighth and final section is a Assembly Code listing of the software needed for an intelligent Ethernet node.

The LANCE-MK68000 hardware and software were designed as simply as possible. The design incorporates a minimum number of interface logic gates and no time multiplexing of devices. Structured assembly code with few subroutines and loops is used, making it easy to change and understand. The schematics and assembly code are presented in a format that easily lends itself to a self-tutorial on an existing Ethernet interface design for users. The design is intended to give users ideas on how to design or how to improve present designs. But, if so desired, users can apply the information directly to quickly generate a basic working interface.

This Application Note refers to many technical aspects of the LANCE but they are not fully explained. For this reason, users should also study the MK68590 LANCE Technical Manual, published by United Technologies Mostek.

2.0 ETHERNET PRIMER

Much debate and questioning as to the nature of celestial bodies existed in the early days of science. These questions included: What type of material exists between the heavenly bodies? If it is not a vacuum, how does light move across it? The conclusion agreed upon was that an Ether existed between the planets and it was the medium light used to travel from the sun to the Earth.

Xerox borrowed this terminology in their early stages of defining a local area network. Ether was the medium information would use to travel from one station to the next throughout the network specification. They called this network "Ethernet."

Ethernet was designed as a system for local communication between computing stations. A series of tapped coaxial cables between computing stations comprise a network that connects up to 1024 different stations per network. In addition, a gateway interface may be used to connect each network to other networks. The computing stations may consist of personal computers, CAD workstations, file storage devices, magnetic tape backup stations, large central computers, printers, plotters or any device that conforms to the Ethernet standard.

The objective of Ethernet was to provide a communication system that can grow with users' needs and accommodate several buildings in a local area. One of its purposes is to eliminate bottlenecks and reliability problems associated with a central controller.

Ethernet provides for one, and only one, connection between any two points on the network. Since the Ether, or the common broadcast communication channel, is passive when an active node fails, only its operation is affected - not the entire system.

Ethernet employs Carrier Sense Multiple Access with Collision Detect (CSMA/CD). The principle behind this operation is similar to human conversation. If several people are conversing while standing in a circle (assuming it is a non-controversial discussion between polite adults), only one person speaks at a time. When the first person finishes, someone else begins to speak and continues until he or she is also finished. If no one has anything else to say, silence falls over the group.

The same is true for Ethernet. Each node listens until the network becomes silent. Then, if a message needs to be transmitted the node broadcasts onto the Ether and the remaining nodes listen.

The more people in the circle, and the more they have to say, the greater the chance that two or more people will begin speaking simultaneously. If this happens in normal conversation, all the participants who have started speaking will stop and whoever begins to speak first will be able to say what he has to say. Two or more people may occasionally begin speaking again at the same time, in which case, they will again stop talking and, hopefully, the more gracious member of the group will wait. When a person starts talking, no one else begins until that person finishes. Delays and collisions occur in Ethernet just as they do in normal conversation. Due to the propagation delays encountered in the medium, a station may not sense network activity and begin transmitting. Once it begins, it keeps listening to the network; if it detects a collision, it aborts the transmission and waits a certain amount of time determined by a random number generator.

In any given group of people, some are naturally talkers while others are listeners. If the conversation does not concern them, the listeners are less likely to pay attention. The same is true with Ethernet stations. Some stations, such as personal computers, transmit much information and others, such as printers, do much of the receiving.

A particular station's Ethernet interface connects bit-serially through an interface to a transceiver that taps into the passive Ether. The Ethernet station, or node, broadcasts its message into the passive Ether, enabling all nodes on the network to hear it. All stations receive the message and determine if they are the desired destination. If the transmitting node's destination address matches that of the receiving node, the packet is accepted and the station digests the data. If the address does not match, the receiving node rejects the packet.

A station may use two addressing schemes when broadcasting. The first is the physical addressing scheme, whereby the transmitting station addresses one, and only one unique destination station. As long as all stations on the network are not in the promiscuous mode, only one station accepts the message.

The second adddressing scheme uses a logical address. In this operation, stations receiving the message must

determine if they are one, of possibly many, intended recipients. An example of logical addressing is one in which all printers have the same logical address. If people want to send memos via the printers, they simply set the destination as the logical address — "printers." All printers on the network then see themselves as the destination and all accept the message. In addition, a station may set itself up in a promiscuous mode. In this mode, the station accepts all incoming messages, no matter what destination address the message has.

When Xerox defined Ethernet, their intent was to define a standard that all manufacturers who wanted access to the Ether, could use. They wanted to define a rigorous standard from the onset to avoid incompatability. Universal acceptance of a standard is the very key to practical applications of local area networking. The International Standards Organization (ISO) has approved a layered protocol standard that specifies functions, as well as minimal rules for accessing these functions and for information exchange between devices on the network. This seven-layer architecture logically groups functions and provides conventions for connecting functions between layers. The model, shown in Figure 1, is called the Open Systems Interconnection (OSI) network model.

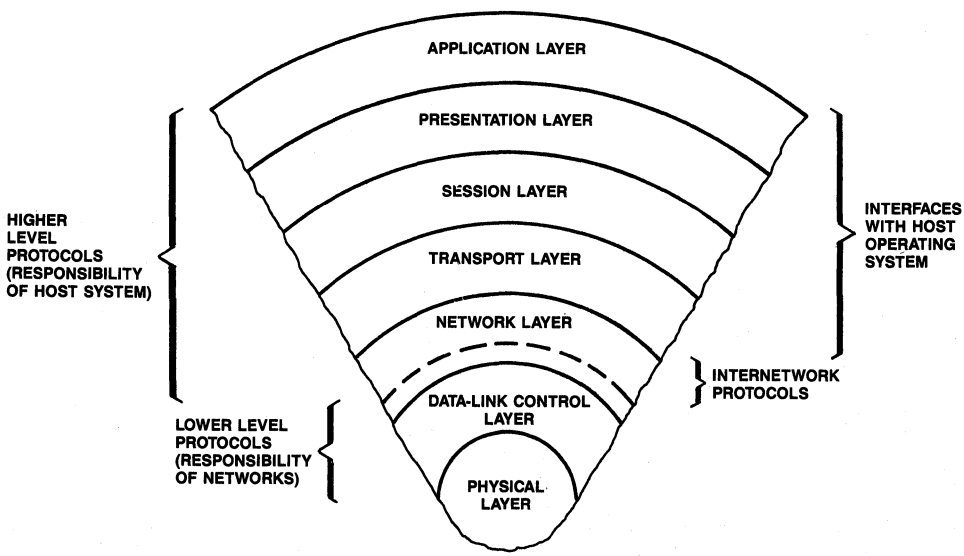


Figure 1. OSI Network Model

The bottom three layers of the OSI model include the physical, data-link control, and network layers. Hardware is based on the actual definition of the two lower layers. Specifications in these layers include the transmission medium (Ether) and how the node must interface to the Ether. The physical and data-link control layers also specify how information should be formatted for error-free transmission and reception. Each layer supports another in hierarchial fashion. In other words, layer 1 serves layer 2, layer 2 serves layer 3 and so forth. The three bottom layers differ according to network architecture. The top three layers — session, presentation, and application — are the same for all networks. The transport layer is the interfacing layer between the top three and bottom three layers.

The functions of each layer of the OSI model follow.

Physical Layer:
- Handle cables, connectors, and components
- Handle collision detection for CSMA/CD
- Handle voltages and electrical pulses

Data Link Control Layer:
- Make sure data is not mistaken for flags
- Add error checking algorithms
- Insert flags to indicate beginning and end of messages
- Provide access methods for local area networks

Network Layer:
- Internetworking
- Send control messages to peer layers about own status
- Set up routes for packets to travel (virtual circuit)
- May disassemble transport messages into packets and reassemble them at their destination
- Flow control
- Recognize message priorities and send messages in proper priority order
- Address network machines on the route through which the packets travel

Transport Layer:
- Multiplex end-user addresses onto network
- Monitor quality of service
- End-to-end error detection and recovery
- Address end user machines without concern for route of message or address machines in route between end user machines
- Possible disassemble and reassemble session messages
- Map address to names

Session Layer:
- Send information from one task to another
- Coordination and cooperation between end users tasks
- Start and stop tasks
- Dialog control
- Recovery from communication problems during a session without losing data

Presentation Layer:
- Encoding and decoding
- Data compaction
- Syntax transformation for character sets, text string, data display formats, graphics, file organization, data types

Application Layer:
- Log in
- Password checks
- Color control
- Graphics procedures
- Downline loading
- Creation of charts and displays
- File requests and file transfers

- Remote job entry
- Computer based message systems
- Job minipulation
- Virtual terminal service
- Data-based queries, insertions, and deletions
- User specific applications (e.g. editing, word processing, electronic funds transfer, airline reservation, and transaction processing)

The LANCE, together with the SIA, Transceiver, and Coaxial cable satisfy the specifications in the bottom two layers of the ISO model. By adding the software shown in this Application Note, layers 1, 2, and 3a can be satisfied.

3.0 DEFINITION OF TERMS

DMA Capability: The ability to directly access memory or memory-mapped I/O. This includes reading, writing, and control signal generation.

Peripheral: A processing unit attached to the system bus which handles part of the processing load.

Bus Master: A CPU or DMA device that has gained control of the system bus. It can initiate data transfers on the bus by issuing an address and by driving the read/write, address strobe, and data strobe control signals.

Bus Slave: A device that decodes the address, read/write, address strobe, and data strobe control signals and responds accordingly for a read or write operation.

Bus Arbitration: In a system with more than one device capable of being the Bus Master, a bus arbitration convention must be employed to determine which device may take control of the system bus at any one time. Normally one of the Bus Master type devices is responsible for receiving and granting requests for access to the system bus.

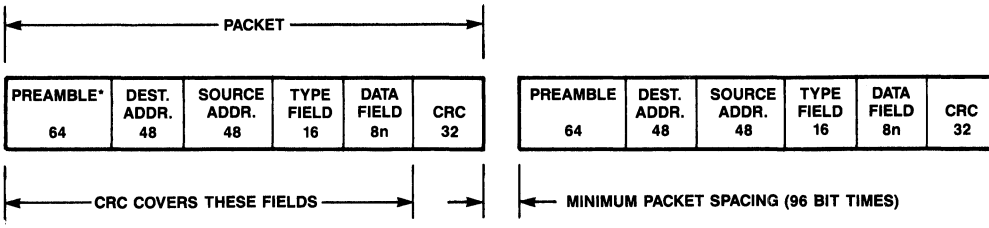
Front End Processor: A processor microsystem, usually consisting of a microprocessor, or single-chip microcomputer, along with memory and control logic. This microsystem alleviates some of the burden placed on the main host processor. The front end processor acts as an intermediate stage of processing between the host processor and an I/O device.

Intelligent Ethernet Node: An Ethernet node that acts as a front end processor to the host processor. An intelligent Ethernet node would basically consist of microprocessor or microcomputer, memory, an Ethernet protocol device (LANCE), transceiver interface device (SIA), and the associated firmware required to implement the lower layers of the Ethernet protocol.

4.0 LANCE CHIP DESCRIPTION

The MK68590 LANCE (Local Area Network Controller for Ethernet) is a 48-pin VLSI device that simplifies interfacing a microcomputer or minicomputer to an Ethernet Local Area Network (LAN). This chip operates in a local environment that includes a closely coupled memory and microprocessor. The LANCE uses scaled N-channel MOS technology and is compatible with several popular microprocessors. It interfaces to a microprocessor bus characterized by time-multiplexed address and data lines. Typically, data transfers are 16 bits wide, but byte transfers occur if the buffer memory address boundaries are odd. The address bus is 24 bits wide.

The Ethernet packet format consists of a 64-bit preamble, a 48-bit destination address, a 48-bit source address, a 16-bit type field, and a 46- to 1500-byte data field terminated with a 32-bit CRC (cyclic redundancy check) as shown in Figures 2 and 3. The packet's variable widths accommodate both short status, command and terminal traffic packets, and long data packets to printers and disks (1024 byte disk sectors, for example). Packets are spaced a minimum of 9.6 usec apart to allow one node time enough to receive back-to-back packets.



*LAST BYTE IS START OF FRAME SYNCHRONIZATION BYTE--10101011

Figure 2. Ethernet and LANCE Packet Format

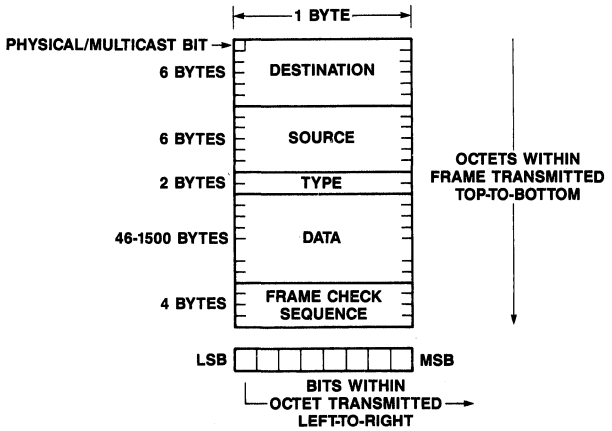


Figure 3. Ethernet and Packet Bit Transmission Sequence

The LANCE operates in a minimal configuration that requires close coupling between local memory and a processor. The local memory provides packet buffering and is a communication link between the chip and processor. During initialization, the control processor loads the starting address of the initialization block plus the operation mode into the LANCE via two control registers. The host processor talks directly to the LANCE only during this initialization as a Bus Slave peripheral. The LANCE's DMA machine, under microword control, handles all further communications.

The LANCE on-chip DMA channel provides flexibility and speed by communicating with the host, or dedicated microprocessor, through common memory locations. Buffer management is organized by a circular queue of tasks in memory called "descriptor rings" (see Figure 4). Separate descriptor rings describe transmit and receive operations. Up to 128 tasks may be queued on a descriptor ring for future execution. Each entry in a descriptor ring holds a pointer to a data memory buffer and an entry for the data buffer length. Data buffers can be chained or cascaded to handle a long packet in multiple data buffer areas. The LANCE searches the descriptor rings in a "look-ahead manner" to determine the next empty buffer for chaining buffers together or handling back-to-back packets. As each buffer is filled, an "own" bit is reset, signaling the host processor to empty this buffer.

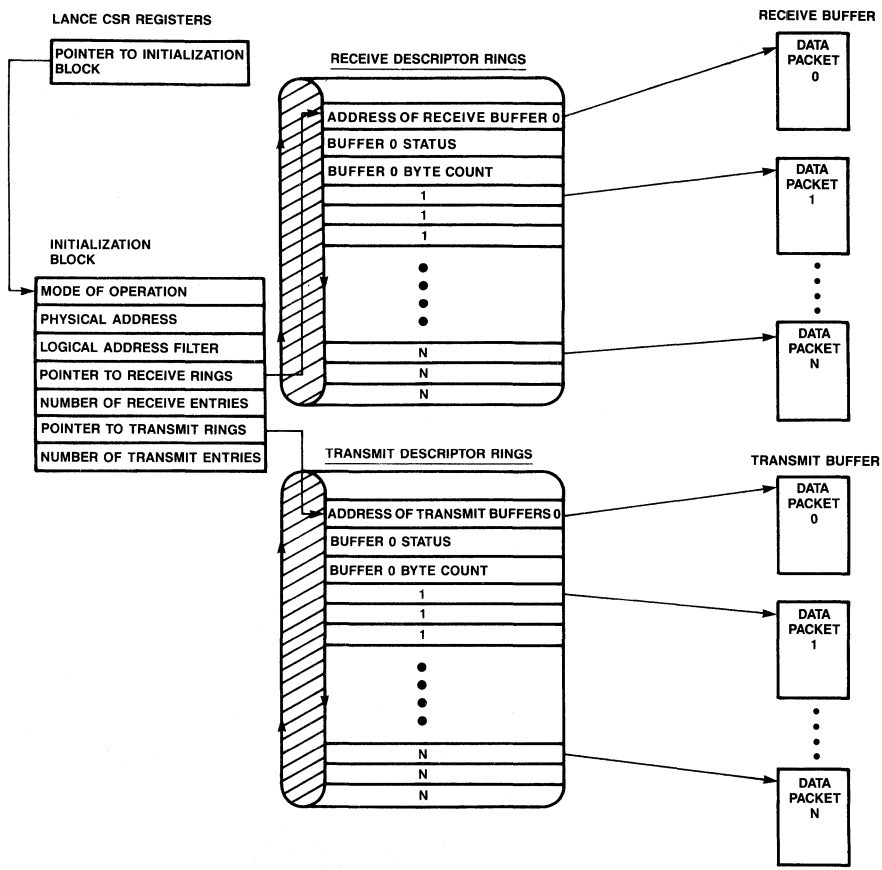


Figure 4. LANCE Memory Management

5.0 ETHERNET NODE OVERVIEW

5.1 INTRODUCTION

The LANCE has two basic types of micro-interfaces. The first is when the LANCE acts as a peripheral to a host processor and the second is when the LANCE and a dedicated microprocessor or microcontroller work together to form an intelligent node. In the second type, all processing between the processor and the LANCE occurs on a local bus, while the entire node interfaces to the main system bus as an intelligent subsystem.

The LANCE parallel interface is designed to be an easy or "friendly" interface to several popular 16-bit microprocessors. This Application Note addresses MK68000 interface requirements, but the concepts can be applied to other microprocessors.

5.2 OPERATIONAL DESCRIPTION

The following two sections are operational descriptions of a typical intelligent Ethernet node controller design, and the Ethernet node controller design used to generate this Application Note.

5.2.1 TYPICAL ETHERNET NODE

An intelligent Ethernet node's primary function is to unburden the host processor from many networking tasks and, at the same time, reduce system bus congestion by eliminating the need for the LANCE to ever access the system bus.

A typical intelligent node performs node initialization and self tests, as well as transmitting and receiving messages. It also retains statistical records of error-causing conditions and generates time-out interrupts. These timeout interrupts are used for both memory refresh and upper-level protocol requirements.

The software of the intelligent node isolates the higher level user software from node details, such as memory refresh and the LANCE interface.

In a typical system, an intelligent Ethernet controller may be designed and placed on a separate system board. The LANCE chip permits placement of the entire Ethernet controller on a single system board because it reduces the chip count. This board would interface to a particular bus structure, i.e., the VME, Versabus™, Multibus™, etc.

The system host procesor may interface to the node processor via a dual-ported memory with the use of semiphores.

5.2.2 APPLICATION-NOTE ETHERNET NODE

The Ethernet node controller design discussed in this Application Note does not have the characteristics of a typical intelligent Ethernet controller. It was designed more as a demonstration and teaching tool. The only software written for the node is the lower level software included in the Appendix.

This design uses a total of 8K bytes of memory. A greater quantity of memory would be present in a typical intelligent Ethernet node design. This design has no memory refresh requirements since static RAMs are used instead of dynamic RAMs.

This design includes a "message send request" button that users depress to send data messages to any desired node. The push button simulates a message request that the system host processor would normally generate. The button idea is only used on the breadboard for controlled message transfer for debug and demonstration purposes.

Depressing the button interrupts the local processor and calls a message routine. This message routine generates a pseudo message and updates the transmit descriptor so proper transmission can occur. Immediately after pushing the button, users can examine the memory to verify message transmission and proper hardware and software operation. The pushbutton was felt to be the best way to demonstrate message generation.

Aside from these few differences, the Ethernet node design used in this publication is functionally the same as a typical design used in industry.

Versabus is a trademark of Motorola, Inc.
Multibus is a trademark of INTEL Corp.

5.3 HARDWARE REQUIREMENTS

As the Bus Master, the LANCE has a wide 24-bit linear address space it can access directly via DMA. This 24-bit address bus interfaces directly to the MK68000's 24-bit bus. The only provision is that latches must be placed on the multiplexed address/data bus to latch up the address at the start of a read or write cycle when the LANCE is the Bus Master. Only the lower 15 bits must be latched up; the upper eight bits can be interfaced directly. When interfacing to the MK68000, BM1 and BM0 correspond to upper data strobe (UDS) and lower data strobe (LDS). Address bit A0 is not used in the basic MK68000 interface.

The basic blocks of this design include the LANCE, MK68000, memory, bus arbitration circuitry, chip select circuitry, and DTACK circuitry. Figure 5 is a block diagram of this interface.

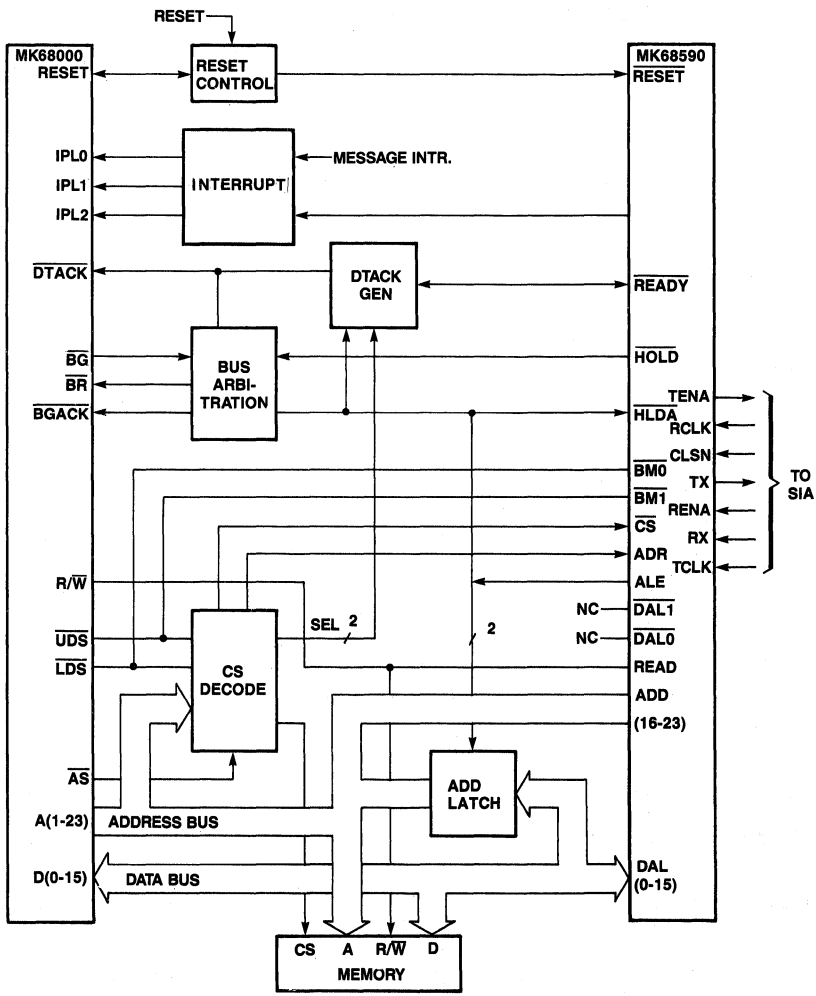


Figure 5. 68000/68590 Block Diagram

The memory includes 8K bytes of random access memory (RAM) and 4K bytes of erasable programmable read only memory (EPROM). The EPROM contains the Ethernet node program, while the RAM is used for receive and transmit rings as well as stack area.

Section 6 — Hardware Description gives a detailed hardware description.

5.4 SOFTWARE REQUIREMENTS

The software program has three functions:

1. Initialize the LANCE
2. Perform message ring management
3. Keep track of the error- and flag-causing conditions.

The software acts as an intermediate stage between the higher-level software protocol of the system host processor and the lower-level protocol implemented by the LANCE. Figure 6 shows the main flow of the software.

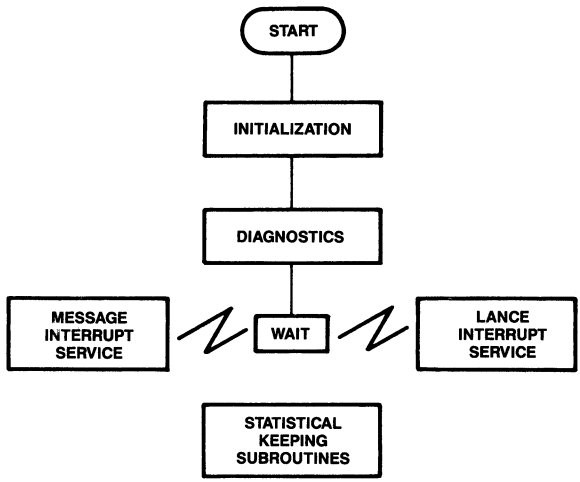


Figure 6. Program Software Overview Flowgraph

The initialization and diagnostics are implemented upon powerup. Users may set up the diagnostics submodule to be implemented any time they desire an operational check. The two service modules — LANCE Interrupt and Message Interrupt — are both interrupt-driven.

The LANCE Interrupt service routine is called when the LANCE interrupts the local processor. The LANCE interrupts the processor when a message is received or transmitted, initialization is complete, or an error has occurred. The error- or flag-causing condition is determined by reading the Control and Status Registers zero (CSR0). The processor then either services the flag-raising condition or calls one of the statistical-keeping subroutines. It then simply reports the condition to the system processor.

It is not necessary for the LANCE to operate on an interrupt-driven basis. The processor may be programmed to periodically poll the Control and Status Registers zero (CSR0) for flag-causing conditions. This Application Note performs the function on an interrupt basis to eliminate the need for a timer.

The message interrupt service routine is called when users depress the "message request" button. The routine generates a pseudo message depending on what parameters users give it. It then writes the message into a transmit message buffer and updates the transmit message descriptor.

As stated before, the "Push-button" operation is not included in a typical Ethernet node processor, but appears here to give the reader possible suggestions on how to write required software for servicing an actual system-generated message.

5.5 SYSTEM MEMORY MAP

All software activities take place in the low end of memory. The entire program uses less than 2K bytes of memory. Figure 7 is a memory map of the space this program uses.

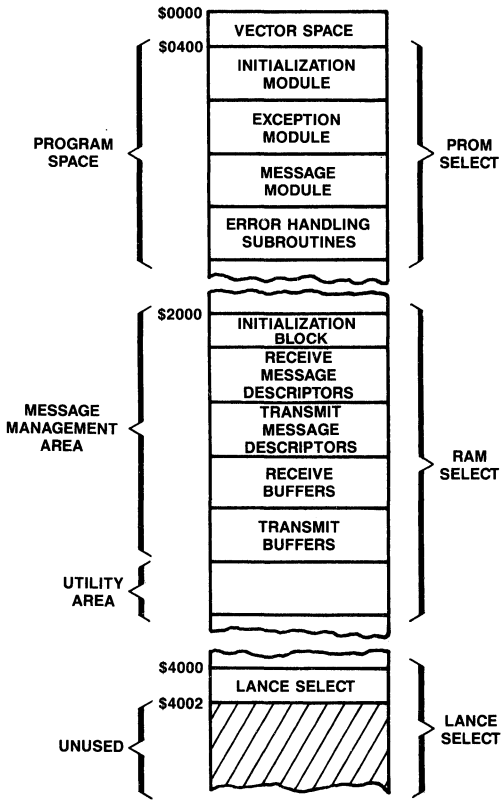


Figure 7. System Memory Map

Memory area from hex address $0000 to $03FF is reserved for vectors. The program resides in the memory space bounded by addresses $0400 and $1FFF. Message management memory space is between $2000 and $387B. This area contains the initialization block and the receive and transmit message descriptors, along with the receive and transmit buffers. The memory space between addresses $387C and $3FFF is the utility area. The program stack, ring management, and error flags reside here. Figure 8 gives a detailed map of the utility area.

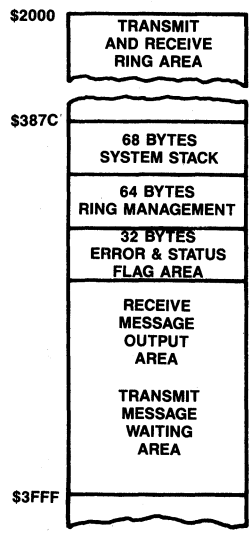


Figure 8. Utility Area Memory Map

Memory location $4000 is the address of the LANCE's register data port (RDP). Memory location $4002 is the address of the LANCE's register address port (RAP).

The receive and transmit ring length, as well as their buffer sizes, are all variable. These variables may be altered by changing an equate statement at the beginning of the program. This Application Note uses eight receive descriptors and four transmit buffers. The size for both transmit and receive buffers is 256 bytes. There are twice as many receive buffers as transmit buffers because it is undesirable for the node to miss an incoming packet due to a lack of receive buffers.

5.6 UTILITY AREA DEFINITION

The utility area is composed of the following:

1. 68 bytes of system stack
2. 64 bytes of ring management variables
3. 32 bytes of error and status flag area
4. 620 bytes for message area.

The message storage area is to be used for receive message output and transmit message waiting area. A ring management stack or status area is set aside in memory to record all transmit and receive descriptor ring activity. Figure 9 gives the address location and describes the information in that memory location.

The addressing mode to access all ring management locations is "Address Register Indirect with Displacement". Base address $38C0 is placed in register A4 upon initialization. The displacements are all defined in the equate statements at the beginning of module number one (see Software listing in the Appendix).

The ring management area has several pointers. Some point to the top and bottom of the descriptor rings. Others point to the next-descriptor to be used and the last-descriptor used. The complicated task of message management is controlled by using these pointers and other status information in the ring management area.

ADDRESS	DESCRIPTION OF CONTENTS
38C0	RECEIVE RING LENGTH Number of entries in the receive ring
38C2	TRANSMIT RING LENGTH Number of entries in the transmit ring
38C4	RECEIVE RING BASE ADDRESS POINTER This points to the first receive message descriptor
38C8	TRANSMIT RING BASE ADDRESS POINTER This points to the first transmit message descriptor
38CC	RECEIVE RING BOTTOM ADDRESS POINTER This points to the last receive message descriptor
38D0	TRANSMIT RING BOTTOM ADDRESS POINTER This points to the last transmit message descriptor
38D4	LAST RECEIVE DESCRIPTOR USED POINTER This points to the last receive descriptor to be used. When the LANCE interrupts the host because of a received message, this pointer will indicate which ring corresponds to the message. If more than one buffer was required for the incoming message, than one buffer was required for the incoming message, this pointer will point to the first descriptor used.
38D8	LAST TRANSMIT DESCRIPTOR USED POINTER This points to the last transmit descriptor turned over to the host by LANCE. When LANCE interrupts the host because it has just transmitted a message, this pointer will indicate the descriptor just used.
38DC	NEXT TRANSMIT DESCRIPTOR TO BE USED POINTER This points to the next transmit message descriptor available for use. The "number of rings available" must be checked before the next ring is accessed. If there are "0" rings available the Next Transmit Pointer will be pointing to a ring which has not been serviced by LANCE.
38E0	LOOPBACK MESSAGE COUNT This contains the number of bytes contained in the loopback message. This is not used in diagnostics
38E2	TRANSMIT DESCRIPTOR COUNT number of descriptors that are available
38E4	RING MANAGEMENT STATUS BIT #1 "1" indicates that LANCE is in LOOPBACK Mode BIT #2 "1" indicates that the START OF PACKET bit was set before BIT #3 "1" indicates that the END OF PACKET bit was set before BIT #4 "1" indicates that the program is in DIAGNOSTIC Mode BIT #5 "1" indicates that this portion of the TEST IS COMPLETE BIT #6 NOT USED BIT #7 NOT USED
38E8	LOOPBACK TRANSMIT BUFFER ADDRESS POINTER
38EC	MORE COUNTER keeps count of the number of times more than one retry was needed to transmit a packet
38EE	ONE COUNTER keeps count of the number of times exactly one retry was needed to transmit a packet
38F0	MESSAGE WORD used for testing and debugging

Figure 9. Ring Management Area Description

6.0 HARDWARE DESCRIPTION

6.1 INTRODUCTION

The circuit described in this Application Note has a minimal amount of logic for interfacing the MK68000 to the LANCE. Figure 5 is a block diagram of the circuit.

The basic interface blocks consist of the following:

1. Chip select decode and DTACK (Data Transfer Acknowledge) generation
2. Address/Data bus interface
3. Interrupt - autovector
4. Bus arbitration blocks.

Detailed schematics of these blocks are given in Figures 10 through 16.

6.2 CHIP SELECT DECODE CIRCUITRY

The Chip Select Decode circuit consists of five logic gates and a Bipolar Programmable Read Only Memory (PROM) as shown in Figure 10. The circuit output enables both the RAM and EPROM, as well as enabling the LANCE. When the LANCE is the Bus Slave and the MK68000 needs to access one of its control-status registers, the LANCE is enabled. As Bus Masters, either the MK68000 or the LANCE can access memory. The DTACK circuitry uses the output signals, RAM SELECT and ROM SELECT. They generate the needed $\overline{DTACK}$ and $\overline{READY}$ signals for the MK68000 and the LANCE, respectively.

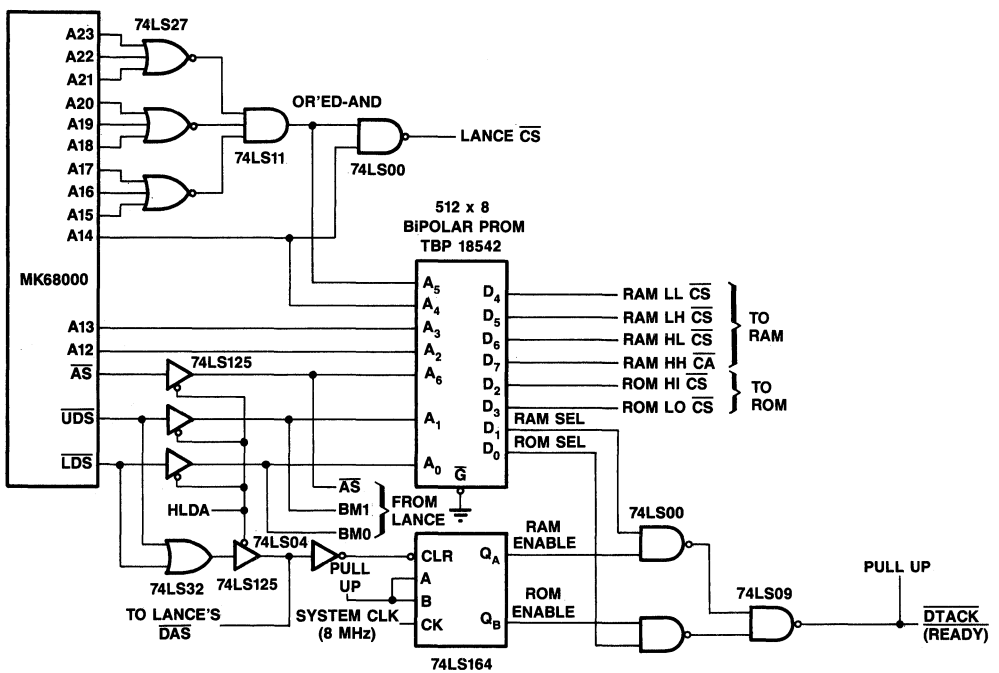


Figure 10. Chip Select Decode and DTACK Circuit

Figure 11 describes chip select decoding. Since the entire addressable memory used in this circuit resides below hex address $7FFF, address bits A15 thru A23 are not used. These address bits are all inputs to the OR-AND gate array. This array's output is active if address bits A15 through A23 are all at logic "0". The decode circuit's output enables different segments of memory. $\overline{\text{RAM HH}}$ enables high-address, high-word of RAM, while $\overline{\text{RAM HL}}$ will enable the high-address, low-word of RAM. $\overline{\text{RAM LH}}$ enables the low-address, high-word of RAM, and so forth. Figure 12 is a chip select decode PROM firmware map.

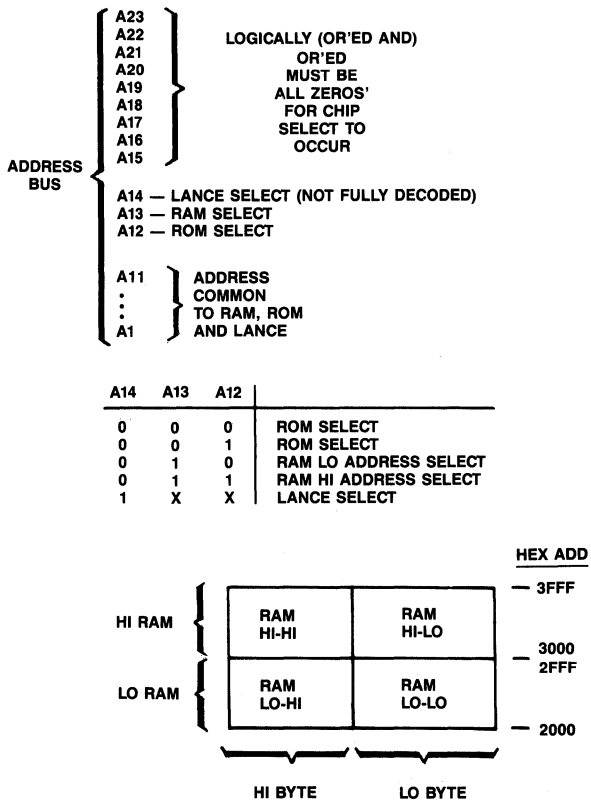


Figure 11. Chip Select Decode Description

AS/	ORED AND A14	A13	A12	UDS/	LDS/		RAM HH CS/	RAM HL CS/	RAM LH CS/	RAM LL CS/	ROM LO CS/	ROM HI CS/	ROM SELECT	RAM SELECT		
A_6	A_5 A_4	A_3	A_2	A_1	A_0	HEX ADD	D_2	D_6	D_5	D_4	D_3	D_2	D_1	D_0	HEX DATA	
0	1 0	0	0	0	0	20	1	1	1	1	0	0	1	0	F2	ROM WORD SELECT
0	1 0	0	0	0	1	21	1	1	1	1	1	0	1	0	F2	ROM HI BYTE SELECT
0	1 0	0	0	1	0	22	1	1	1	1	0	1	1	0	F6	ROM LO BYTE SELECT
0	1 0	0	0	1	1	23	1	1	1	1	1	1	0	0	FC	INVALID (NO SELECT)
0	1 0	0	1	0	0	24	1	1	1	1	0	0	1	0	F2	ROM WORD SELECT
0	1 0	0	1	0	1	25	1	1	1	1	1	0	1	0	FA	ROM HI BYTE SELECT
0	1 0	0	1	1	0	26	1	1	1	1	0	1	1	0	F6	ROM LO BYTE SELECT
0	1 0	0	1	1	1	27	1	1	1	1	1	1	0	0	FC	INVALID (NO SELECT)
0	1 0	1	0	0	0	28	1	1	0	0	1	1	0	1	CD	LOW ADDRESS/WORD SELECT
0	1 0	1	0	0	1	29	1	1	0	1	1	1	0	1	DD	LOW ADDRESS/HI BYTE SELECT
0	1 0	1	0	1	0	2A	1	1	1	0	1	1	0	1	ED	LOW ADDRESS/LO BYTE SELECT
0	1 0	1	0	1	1	2B	1	1	1	1	1	1	0	0	FC	INVALID (NO SELECT)
0	1 0	1	1	0	0	2C	0	0	1	1	1	1	0	1	3D	HI ADDRESS/WORD SELECT
0	1 0	1	1	0	1	2D	0	1	1	1	1	1	0	1	FD	HI ADDRESS/HI BYTE SELECT
0	1 0	1	1	1	0	2E	1	0	1	1	1	1	0	1	BD	HI ADDRESS LO BYTE SELECT
0	1 0	1	1	1	1	2F	1	1	1	1	1	1	0	0	FC	INVALID (NO SELECT)
1	X X	X	X	X	X		1	1	1	1	1	1	0	1	FC	INVALID (NO SELECT)
X	X X	X	X	X	X		1	1	1	1	1	1	0	0	FC	INVALID (NO SELECT)

Figure 12. Chip Select Decode PROM Firmware

6.3 DTACK CIRCUITRY

A few logic gates and and a shift register make up the $\overline{\text{DTACK}}$ circuitry (see Figure 10). The shift register allows selectable delay time outputs to compensate for varying memory access speeds.

When the LANCE is a Bus Master, $\overline{\text{READY}}$ is an asynchronous acknowledgement from the $\overline{\text{DTACK}}$ circuit that memory will accept data in a WRITE cycle, or that memory has put data on the Data/Address lines in a read cycle.

As a Bus Slave, the LANCE asserts $\overline{\text{READY}}$ when it has put data on the Data/Address lines during a READ cycle or, is about to take data off the Data/Address lines during a WRITE cycle. Ready is a response to Data Address Strobe ($\overline{\text{DAS}}$) and is negated after $\overline{\text{DAS}}$ is negated. The separate $\overline{\text{DTACK}}$ signals are wire ORed with the $\overline{\text{READY}}$ signal from the LANCE. In this manner, the $\overline{\text{READY}}$ signal can be either an input or output. When the LANCE is the Bus Master, the $\overline{\text{DTACK}}$ input on the MK68000 is in the high impedance state.

6.4 ADDRESS/DATA BUS INTERFACE

Figures 13 and 14 are schematics of address and data bus interfacing. The interfacing is very straightforward. The data bus is connected directly between the MK68000, the LANCE, and memory. Address bits A16 through A23 are connected up directly between the LANCE and the MK68000. Since the LANCE has a multiplexed Address/Data bus, tri-state latches must be placed on the DAL lines. These latches store the address during the beginning of a read or write cycle when the LANCE is a Bus Master. $\overline{HLDA}$ enables the output of the latches, this occurs only when the LANCE is a Bus Master.

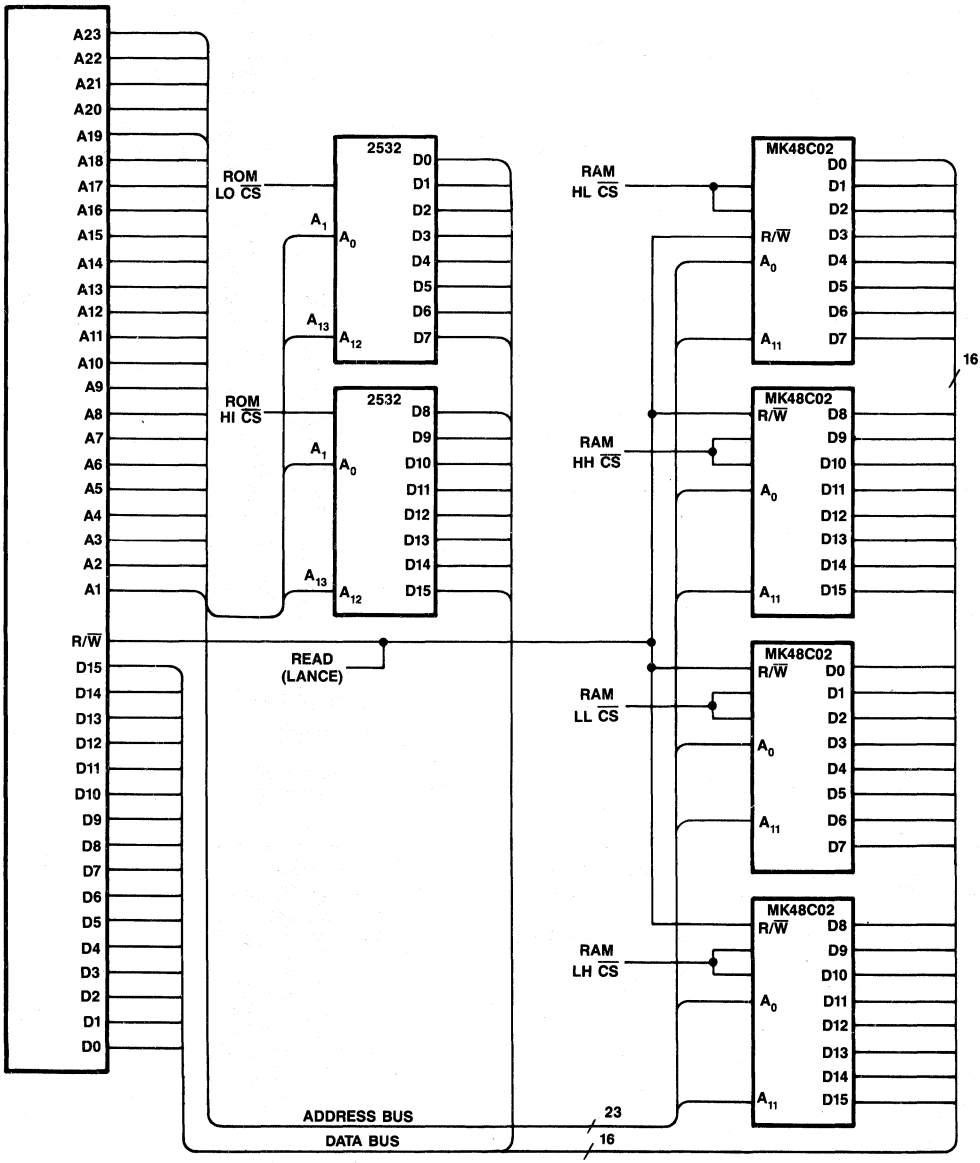


Figure 13. MK68000-Memory Interface Circuit

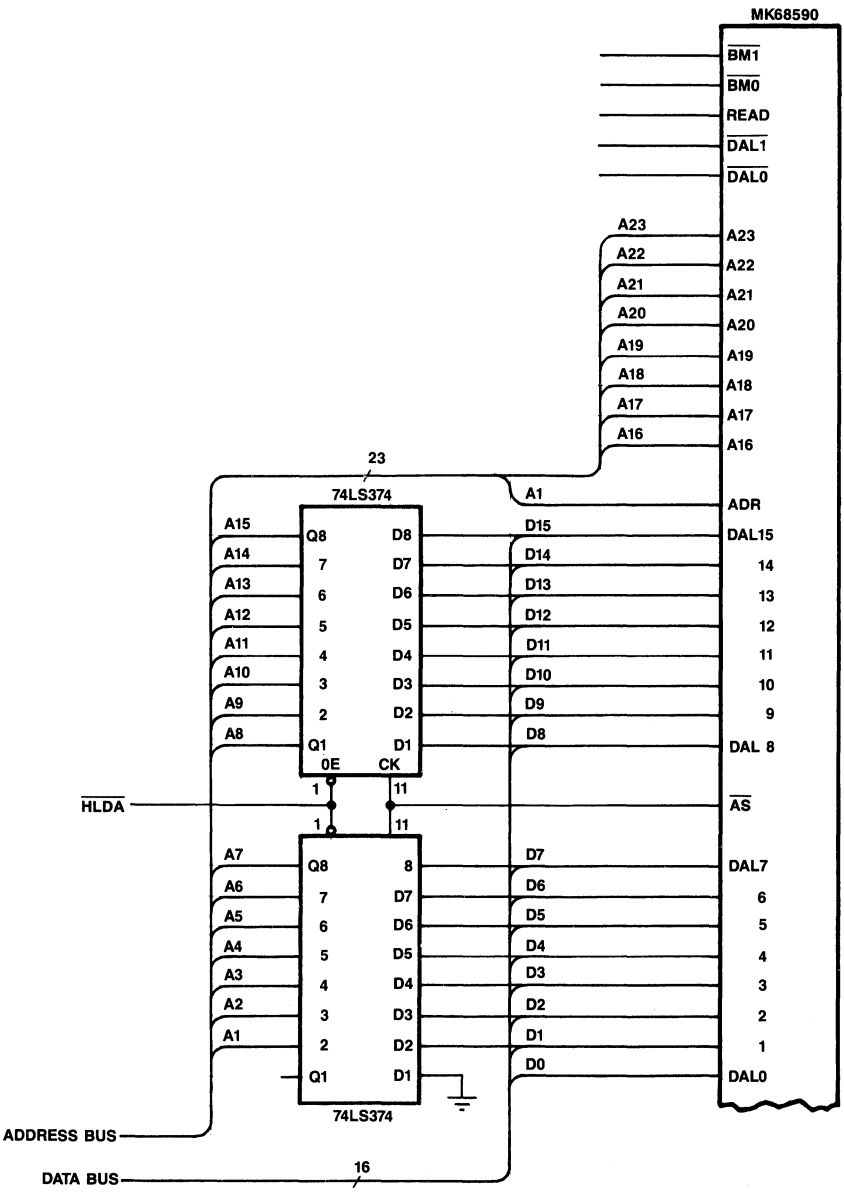


Figure 14. Address/Data Bus Interface Circuit

6.5 INTERRUPT CIRCUITRY

The interrupt circuitry, as shown in Figure 15, handles incoming interrupts to the MK68000, and also handles the interrupt acknowledgement scheme. This circuit has two interrupt sources. One can come from the LANCE, the other can come from a push button on the breadboard. The push button informs the MK68000 that a message is ready to be transmitted.

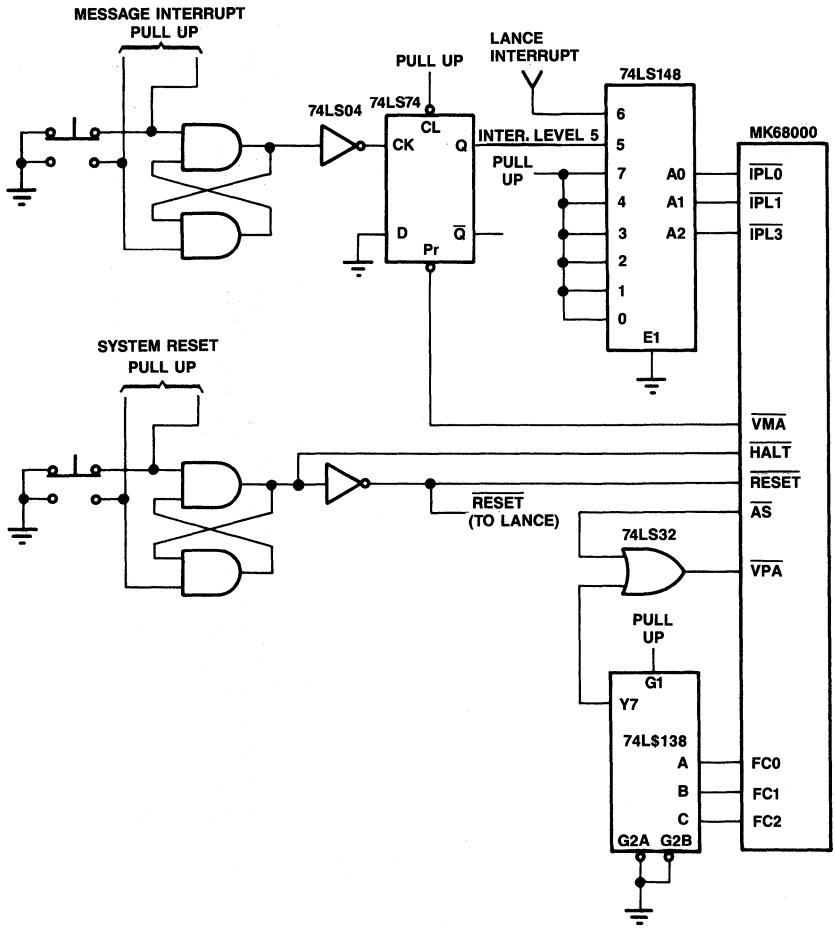


Figure 15. Interrupt and Auto Vector Circuit

6.6 AUTOVECTORING CIRCUIT

Interrupts in this program are handled with autovectoring. The interrupt from the LANCE is set to interrupt level six, and the interrupt that represents a "message ready to be transferred" from the system host is set at interrupt level five. Level seven interrupt is the nonmaskable interrupt, and is not used in this circuit.

Upon an interrupt, the MK68000 responds with binary "111"' at the Function Code Output (FC0-2). This is decoded and Valid Peripheral Acknowledge (VPA) is generated from it, which tells the MK68000 to autovector (see the MK68000 Users Manual for more details on autovectoring).

6.7 BUS ARBITRATION CIRCUIT

The Bus Arbitration circuit, as shown in Figure 16, generates the necessary control and handshake signals needed for the LANCE to take control of the bus. The MK68000 has three handshake signals for bus arbitration, while the LANCE has only two. When the LANCE requires control of the bus, it asserts $\overline{HOLD}$. The MK68000 returns a Bus Grant ($\overline{BG}$) signal. $\overline{BG}$ along with $\overline{DTACK}$ and $\overline{AS}$ generate hold acknowledge HLDA and Bus grant acknowledge ($\overline{BGACK}$). $\overline{DTACK}$ and $\overline{AS}$ are needed to verify that the previous cycle is over before the LANCE takes control of the bus. A timing diagram of the bus arbitration process is shown in Figure 17.

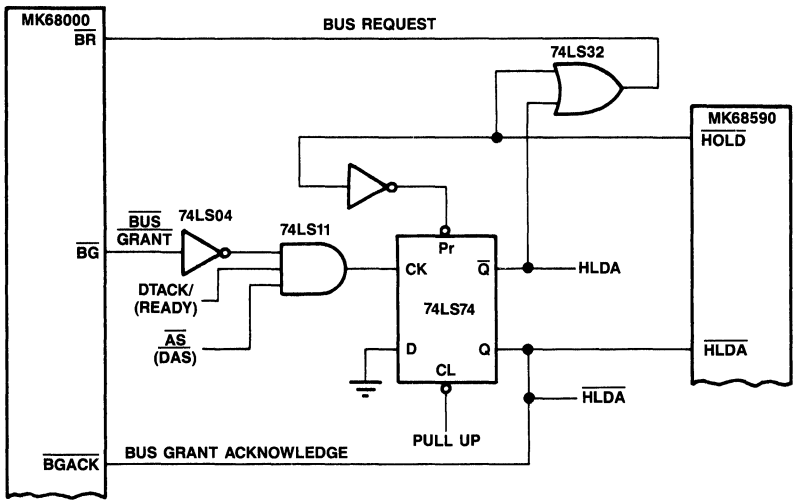


Figure 16. Bus Arbitration Circuit

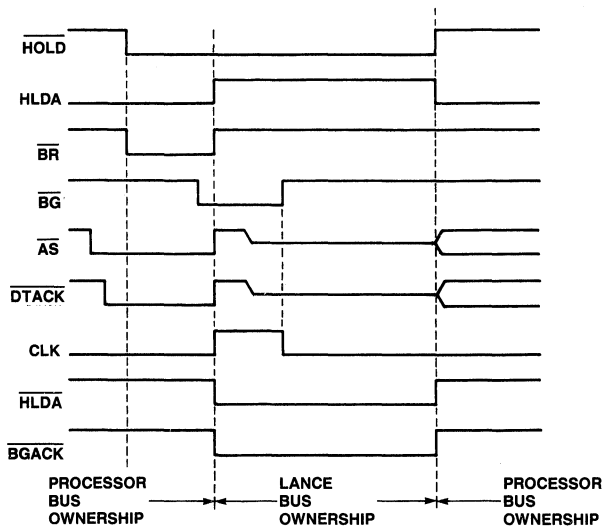


Figure 17. Bus Arbitration Timing

6.8 SIA-LANCE INTERCONNECT

Users must carefully plan the interconnect layout between SIA, the LANCE, and the output connector to the transceiver. The SIA is a very fast ECL interface device. It has an internal voltage controlled oscillator (VCO) that generates a 40 MHz clock from which internal timing is derived. This device is very susceptible to noise. For this reason, the proximity of the SIA to the LANCE and output connector is important. Very close coupling between all filter and terminating devices is required. They must be mounted directly adjacent to the SIA pins in printed circuit boards and must be attached directly to the socket pin in a breadboard situation.

Only low-profile sockets should be used for the SIA in a breadboard situation. ZIP-DIPs, or high-profile sockets result in an environment too noisy for the fast communication rates these devices generate.

Decoupling is also very important when building a breadboard or laying out a PC board. The Ground and V_{CC} pins (Pins 1 and 48) of the LANCE should be decoupled to reduce noise possibilities. These capacitors should be attached directly to the socket pins in a breadboard situation. Figure 18 gives suggested filter values to be used on the SIA.

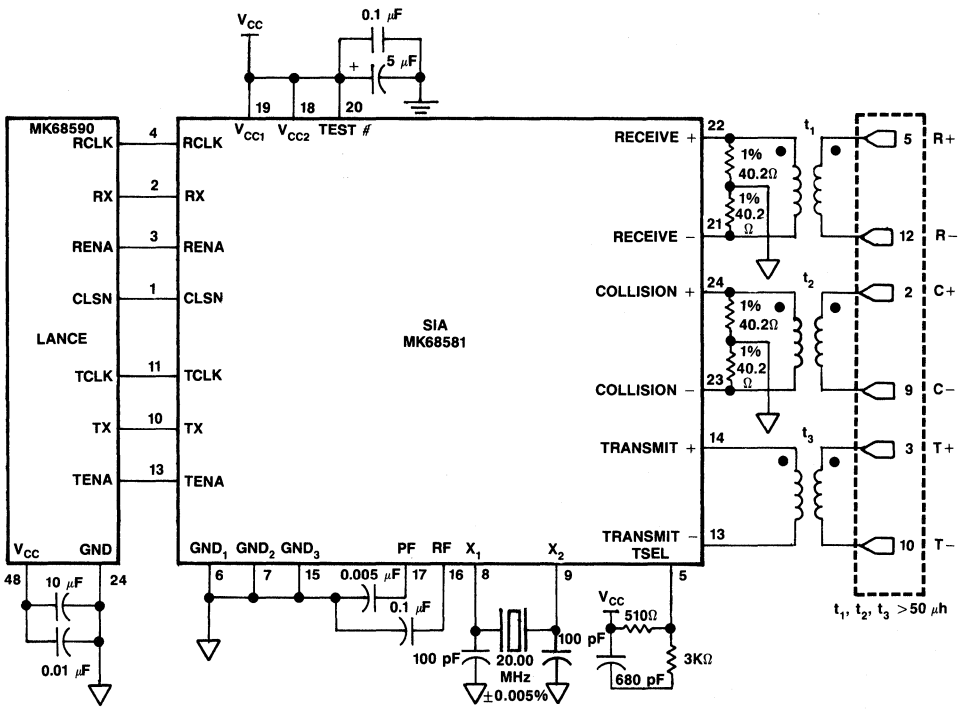


Figure 18. SIA Filter Values

7.0. SOFTWARE DESCRIPTION

7.1 INTRODUCTION

The software needed to generate a basic interface between the LANCE and the MK68000 is described in three different formats: a written description of the step-by-step process, flow charts of the individual submodules, and a printout of the actual assembly code. The assembly code appears in Appendices A, B, and C.

Users should read the software description along with studying the flow charts and assembly code. This triple reinforcement should make it easier to comprehend software requirements.

The software has four basic modules, as shown in the memory map of Figure 19. They include: Initialization & Diagnostics, LANCE Interrupt, Message Interrupt, and Status Module.

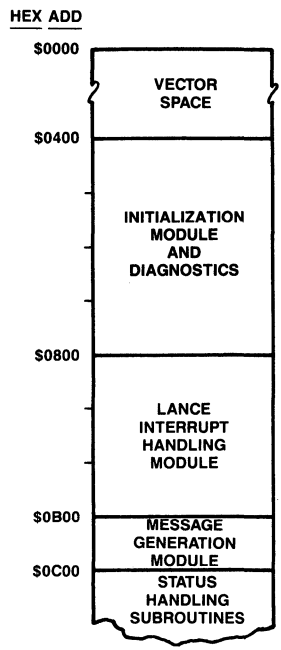


Figure 19. Software Memory Map

7.2 INITIALIZATION & DIAGNOSTICS SOFTWARE MODULE

7.2.1 INTRODUCTION

The Initialization & Diagnostics Module, as shown in Figure 20, contains six submodules:

1. Clear
2. Block-Move
3. Receive Ring Initialization
4. Transmit Ring Initialize
5. Diagnostics
6. Normal Initialize.

The diagnostics portion is actually a subroutine. Diagnostics may be performed at any time by simpling calling this subroutine.

In addition to these six submodules are two subroutines: Control and status Register Initialization Subroutine, and the Cyclic Redundancy Check Subroutine.

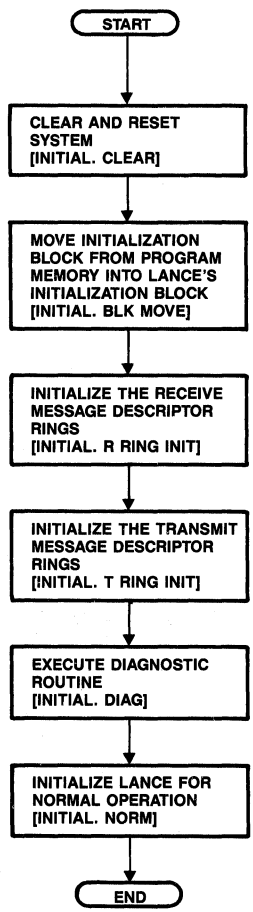


Figure 20. Initialization Software Module [LANCE. INITIAL]

7.2.2 CLEAR SUBMODULE

Upon powerup, the MK68000 (also referred to as the local host, or host) addresses the reset vector location $0000 that holds the address of the start of the program. The starting address of the Clear Submodule, shown in Figure 21, is at location $400.

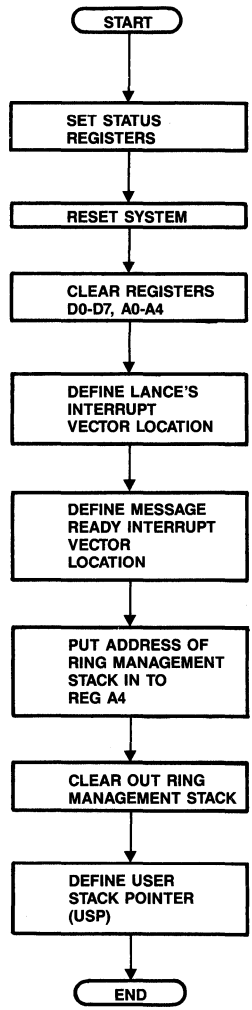


Figure 21. Clear Submodule [LANCE. INITIAL. CLEAR]

The program's first action is to reset the LANCE and other peripherals on the local system bus. Next, it clears out the address and data registers, sets the interrupt mask, loads the interrupt autovectors and both system and ring-management stack locations. The ring management area starting address is stored in Address Register A4. Following this action, the host clears all data held in the ring status register.

7.2.3 BLOCK-MOVE SUBMODULE

Once the registers have all been cleared, the processor's next task is to move the LANCE's initialization block into memory where the LANCE can access it. Information also must be extracted from the initialization block which allows the software to determine the base addresses of the transmit and receive descriptor rings and their respective lengths. These operations take place in the "Block-Move" submodule described by the flowchart in Figure 22.

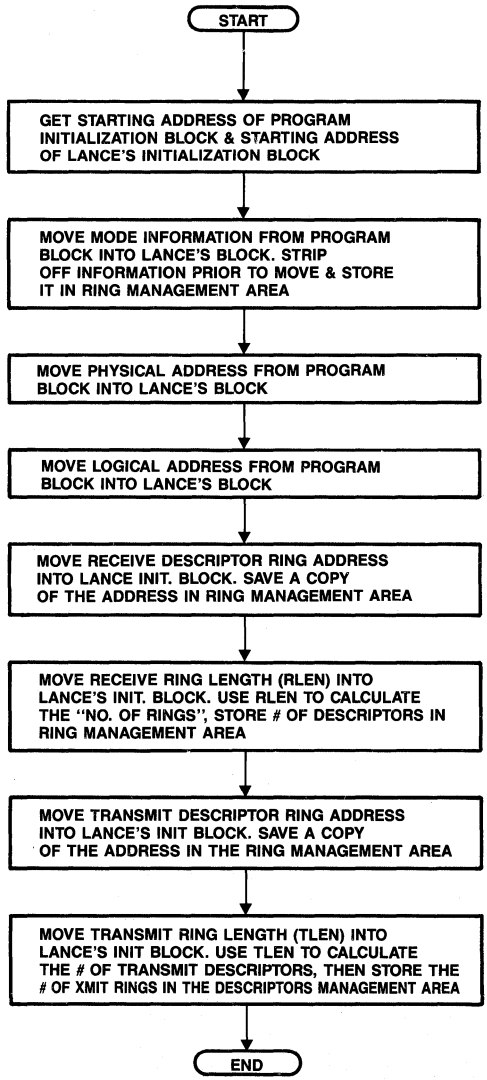


Figure 22. Block-Move Submodule [LANCE, INITIAL. BLKMOVE]

The LANCE buffer management information is set up as equates. Equates define the following information:

1. Starting address of the initialization block
2. Displacement needed between the initialization block's starting address to the receiver and transmit descriptors' starting address
3. Number of transmit and receive buffers desired
4. Desired buffer size.

By altering one or more equate statements, any of these buffer management areas may be relocated in memory.

This software routine makes all calculations needed to initialize the receive and transmit descriptors. The only limitation is that all receive descriptors must be in a contiguous block of memory. The same holds true for transmit descriptors. The buffers for the receive and transmit operation may be placed anywhere throughout the memory by specifying a buffer displacement from the descriptor's starting address (see Figure 23).

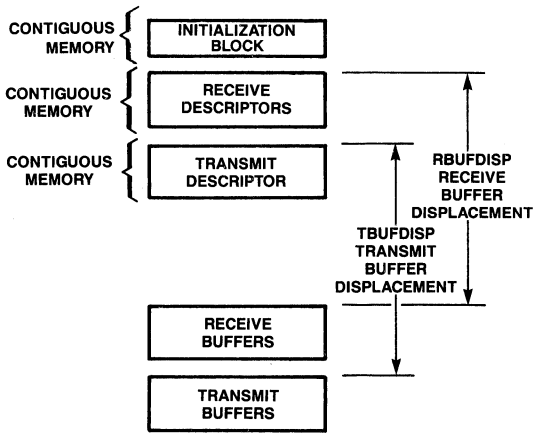


Figure 23. Buffer Displacement Diagram

This design was chosen to give the program more flexibility. The same piece of software can be used, independent of buffer number, size, and location.

Information is stripped by the block-move submodule from the initialization block source and transferred to the LANCE shared memory. If the source is EPROM, the initialization block is identical upon each powerup. If the source is downloaded from the main host, the initialization block may vary from one powerup sequence to the next. The software in this Application Note was written so the initialization block, receive and transmit descriptors, and the receive and transmit buffers are all in contiguous memory.

The "Block-Move" submodule also strips the receive and transmit ring lengths as it moves the initialization block into memory. It stores the values to be used in memory allocation calculations in the receive and transmit ring initialization routines. It also extracts mode information and sets the corresponding bits in the ring management status register. In addition, it also copies, reformats for MK68000 compatability, and stores the receive and transmit ring base address for later use.

In this software design, the receive and transmit descriptor base addresses are predetermined and the program generates the buffer addresses from ring length information. The software also could have been structured to give only ring length information. The program would then determine ring and buffer locations. Another structure may have all address information pre-calculated without any calculations necessary upon initialization, although this structure would not allow flexible ring management. The structure depends on the application desired.

7.2.4 RECEIVE RING INITIALIZATION SUBMODULE

Once the entire initialization block is moved into the share memory, the "Block-Move" submodule is complete and the "Receive Ring Initialization" submodule begins. This submodule initializes all receive ring descriptors by generating Receive Descriptors 0 through 3 (RMD0, RMD1, RMD2, & RMD3), as shown in Figure 24. It generates each descriptor's respective buffer address by displacing it with the buffer length and displacement.

For example, if 256-byte buffers are required and the receive descriptor has a starting address of hex $5000 and a buffer displacement of hex $1000, users would first add the buffer displacement to the starting address of the descriptors. This would give a receive buffer starting address of hex $6000. Therefore, the buffer address of receive buffer number 1 would be $6000. Receive buffer number 2 would have a starting address of $6100, Receive number 3 would have a starting address of $6200 and so on, each displaced 256 bytes, or one buffer length from the previous buffer. Once the descriptor is initialized, ownership of it is given to the LANCE to be used when an incoming message is received.

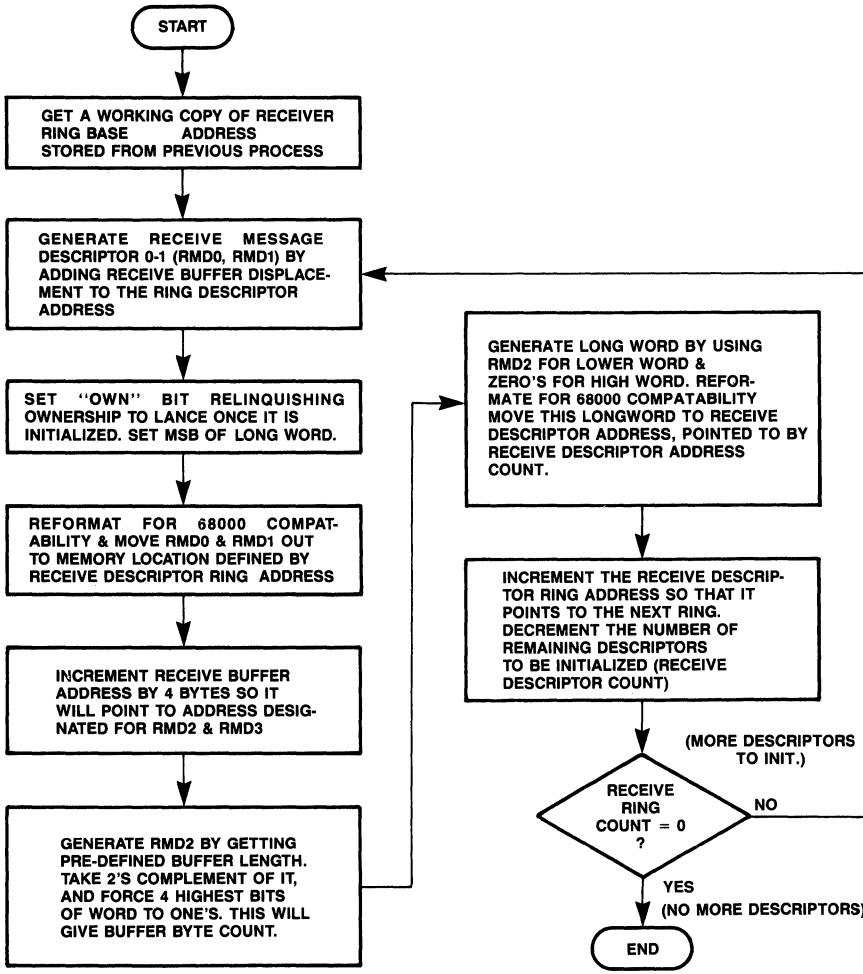


Figure 24. Receive Ring Initialization Submodule [LANCE. INITIAL. RRINGINIT]

7.2.5 TRANSMIT RING INITIALIZATION SUBMODULE

When all receive ring descriptors are initialized, the program proceeds into the "Transmit Ring Initialization" submodule shown in Figure 25. This submodule initializes the transmit descriptors in much the same way it initializes the receive descriptors, with the exception that the host retains ownership of the transmit descriptors. They are used during message transmission. This submodule also generates the 2's complement of the byte count (BCNT) and places it in the address specified for TMD2.

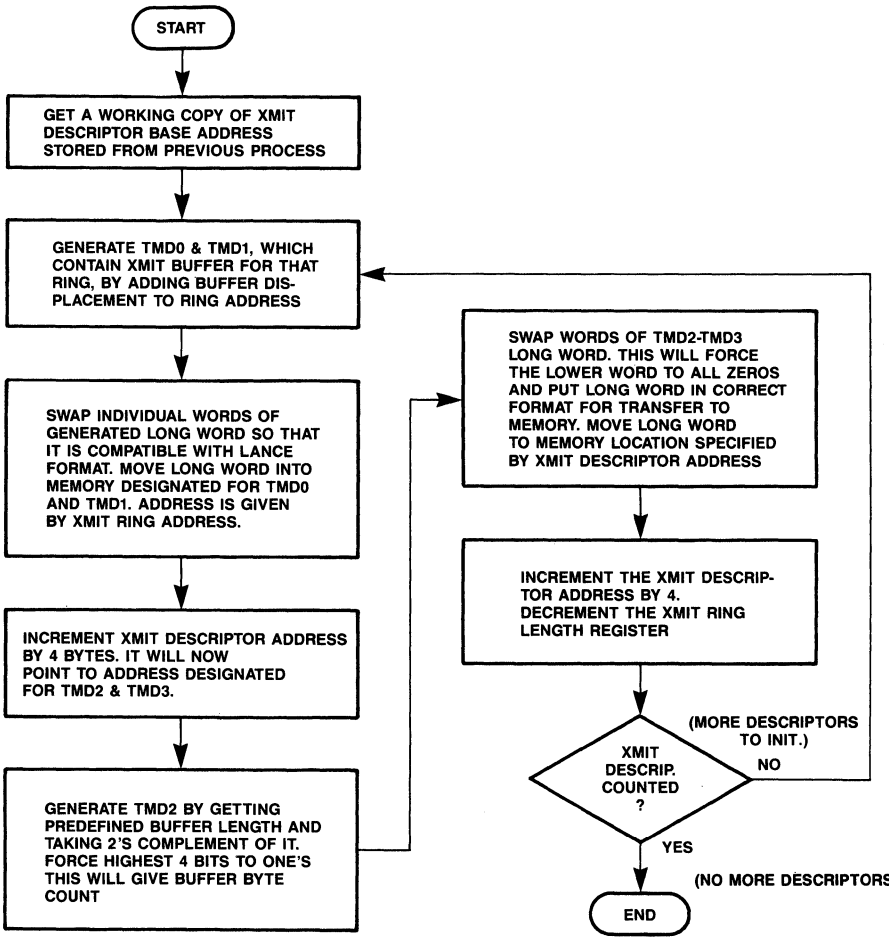


Figure 25. Transmit Ring Initialization Submodule [LANCE. INITIAL. TRINGINIT]

7.2.6 DIAGNOSTIC SUBROUTINE

At this point in the program, the initialization block is in memory, which the LANCE can access. The receive and transmit rings are initialized. A diagnostic routine now needs to be run to determine if the LANCE and associated hardware are operating properly. (See Figures 26 and 27.) This is done by placing the LANCE in four different loopback modes:

1. Internal loopback with transmit CRC enabled
2. Internal loopback with transmit CRC disabled
3. Internal loopback with transmit CRC enabled and the collision force bit set.
4. External loopback.

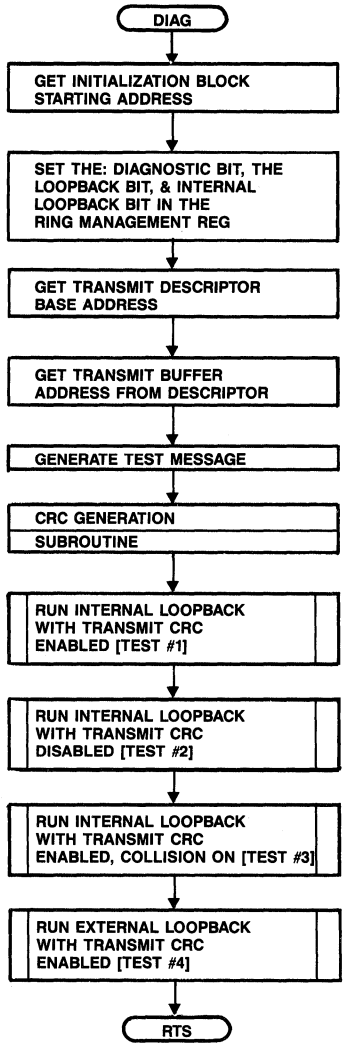


Figure 26. Diagnostics' Subroutine [LANCE. INITIAL. DIAG]

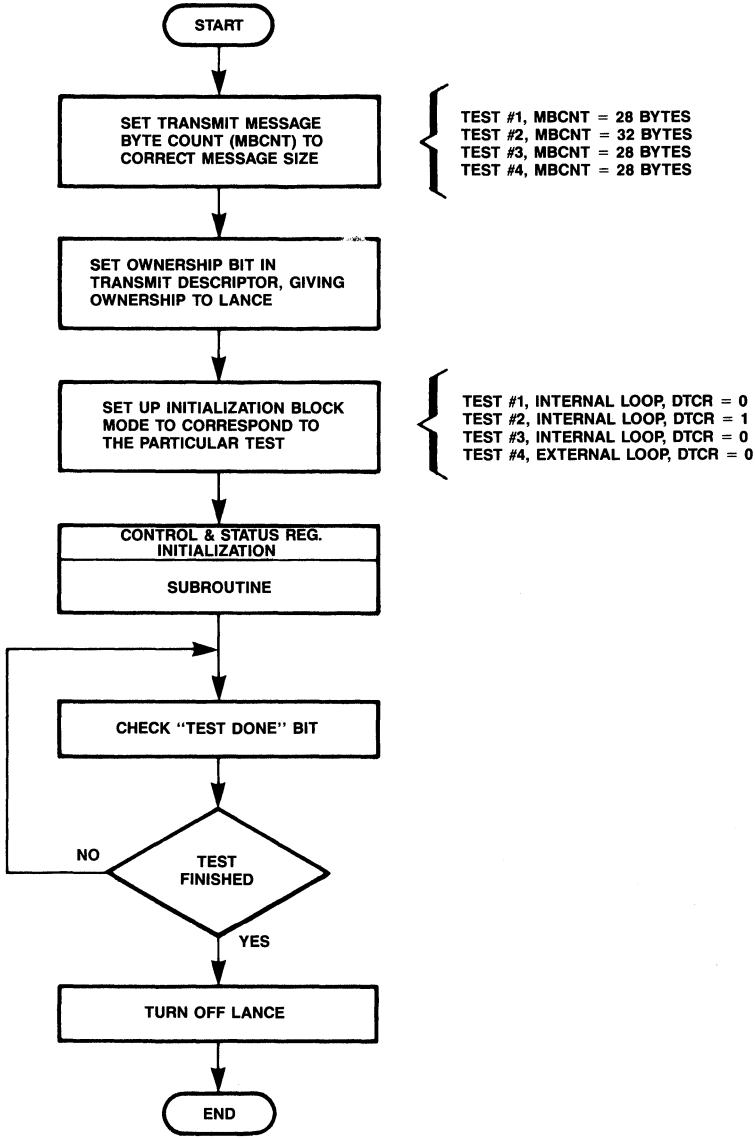


Figure 27. Loopback Diagnostic Test Routine

To test the LANCE, a test message must be generated and placed in the first transmit buffer. In addition, the first transmit descriptor must be initialized.

The test data message created in this program is 28 bytes long. The test message is all hex A's, which is alternating binary 1's and 0's. The maximum amount of data that can be transmitted in loopback mode, whether external or internal, is 32 bytes. With transmit CRC enabled, a 28-byte message is transmitted but, the actual message size is 32 bytes because the LANCE tags four bytes of hardware CRC upon transmission. The transmit length constraint is due to the size limitation of the LANCE's SILO.

In this Application Note, the loopback date size is 28 bytes for all four tests.

After the message is generated, a CRC is generated by calling the software CRC subroutine described in Section 7.2.6.1. In all but the second loopback test, the LANCE's transmit CRC is enabled (bit 3 of the mode is set for transmit CRC disable). When the transmit CRC is disabled, a software CRC is generated and transmitted with the message. For the remaining loopback tests, the LANCE generates the CRC code in hardware and tags it on the end of the transmitted message. This hardware-generated CRC is then compared to the software CRC to assure proper operation of the LANCE.

The CRC generation is followed by initialization of the transmit descriptor. The buffer byte count (BCNT) of 28 is written into transmit message descriptor 2 (TMD2). The start and end of packet bits, as well as the own bit are set in transmit message descriptor 1 (TMD1). Following this descriptor initialization, the mode is set to: promiscuous, internal loopback, with the "disable transmit CRC" bit set to "0".

As described before, with transmit CRC enabled, a CRC is generated for the outgoing message, but is not checked for the incoming message. This is because the LANCE has only one CRC device. The device can generate the CRC or check the CRC, but not concurrently. Verification of proper CRC occurs in the Receive Interrupt submodule, described later.

The final step in each loopback test is an initialization of the LANCE's control and status registers (CSRINIT subroutine call). The CSRINIT subroutine initializes the control and status registers which effectively starts the LANCE. These subroutine steps are summarized in Section 7.2.6.2.

Once the CSRINIT subroutine has executed, the LANCE initializes itself. The program stays in a loop, waiting for completion of this part of the loopback test. This is indicated when a test-complete bit is set in the ring management status register. Once one portion of the loopback test has completed, the next portion begins.

The steps taken after the CSR initialization subroutine is called include:

1. The LANCE is initialized by calling [CSRINIT].
2. The LANCE requests the bus and makes DMA cycles. It reads the entire initialization block.
3. The LANCE polls the receive and transmit rings to check for ownership (see MK68590 LANCE Technical Manual for a more detailed description of polling routines.)
4. Finding that it owns the transmit ring, it enters its transmit DMA routine.
5. Once it has completed its transmission, it immediately starts to DMA the message it concurrently received into the receive buffer.
6. The LANCE then interrupts the MK68000 to notify it that a transmission and reception has occurred.
7. The program vectors off to service the interrupt routine. During the exception processing routine, the application-dependent status subroutines are called if an error flag is found.
8. Once all exception processing is complete, the test done bit is set and a return from the exception processing occurs.
9. The "test-done" bit is constantly checked. Once set, the program continues normal execution, turning off the LANCE and proceeding to the next portion of the diagnostics.

When loopback test number one is complete, the second loopback test proceeds in a similar manner as the first. The only difference between loopback tests is the mode. For clarity, this test is repeated four times in the software rather than tightening the code by inserting four loops.

If the diagnostics detects problems with the LANCE, the status subroutines report the errors by setting a status bit in memory. This Application Note does not deal with error handling, since it is application-dependent and out

of the real of this document.

After all four loopback tests have completed, the LANCE is initialized for normal operation.

7.2.6.1 CRC CODE SOFTWARE GENERATION

Before the descriptor initialization, a CRC subroutine, is called to generate a 32-bit cycle redundancy check code (CRC) to be added at the end of the message (see Figure 28).

Since all hex A's is the predetermined data in the message, the CRC can also be predetermined. If the test message differed for each test, an actual rigorus software CRC subroutine would have to be designed. But, in this case, the CRC subroutine simply writes $B1109280 out to the message buffer. This data is the CRC code for the 28-byte test message.

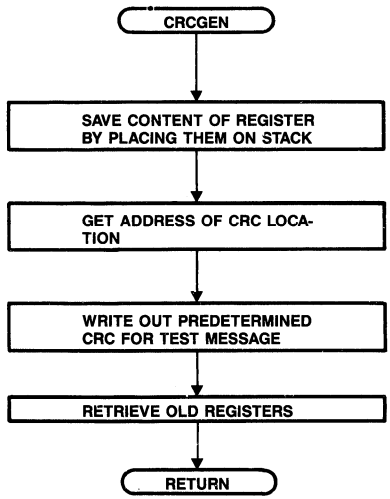


Figure 28. Cycle Redundancy Check Generation Subroutine [CRCGEN]

7.2.6.2 CONTROL AND STATUS REGISTER INITIALIZATION SUBROUTINE

The Control and Status register initialization subroutine is shown in Figure 29. The first step is to move the initialization starting address into the LANCE's Control and Status registers. The low order bits <00:15> are placed in CSR1, and the high order bits <16:23> are placed in CSR2. Next, the LANCE is made compatible to the hardware interface by setting BSWP = 1, ACON = 1, and BCON = 0 in CSR3. Finally, a $0043 is written into CSR0, which sets the Interrupt Enable, the Start and Initialize bits. Immediately following this last write, the LANCE starts its initialization procedure by requesting the bus and completing 12 DMA cycles. Each DMA cycle corresponds by moving one word of the initialization block into its internal registers.

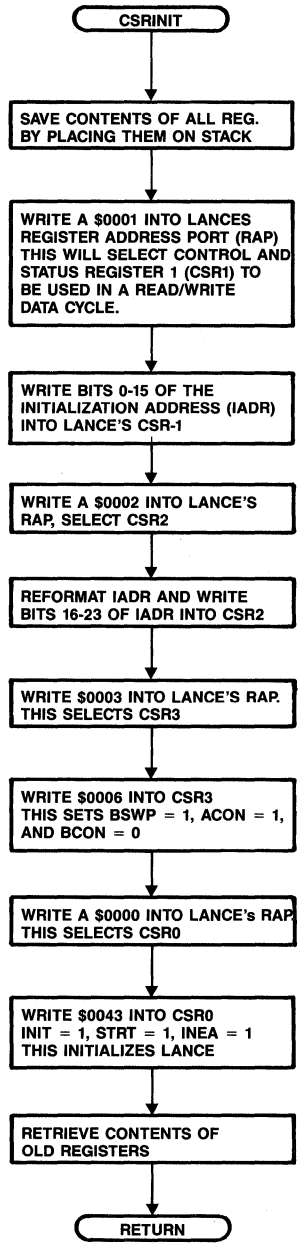


Figure 29. Control and Status Register Initialization Subroutine [CSRINIT]

Once the DMA cycles are complete, the LANCE interrupts to notify the host of completed initialization. If the Interrupt Enable bit in CSR0 is not set, the LANCE does not interrupt the host, but rather, waits for the host to poll its Control and Status register.

Next, a polling routine is begun to determine which receive and transmit descriptors are owned by LANCE. When a LANCE-owned receive ring is found, that result is stored and polling continues to locate a relinquished transmit ring. The CSR initialization submodule is complete when the final CSR0 takes place. The program then returns from this subroutine.

7.2.7 NORMAL-OPERATION INITIALIZATION

After the diagnostics are complete, the normal-operation initialization occurs. This submodule is shown in Figure 30. The predefined mode in the program initialization block is moved into the LANCE's initialization block. The mode information is checked to determine if the desired mode is a loopback mode. If it is, the ring management status register is set up accordingly. The LANCE is then restarted by calling the control and status register initialization subroutine, CSRINIT.

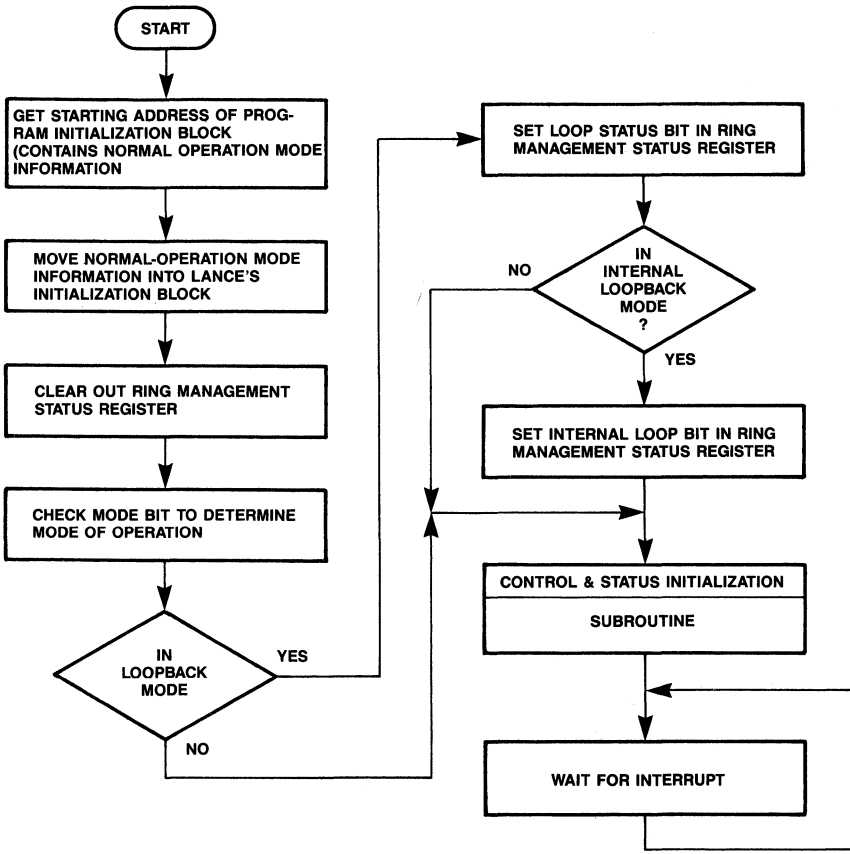


Figure 30. Normal Operation Initialization Submodule [LANCE. INITIAL. NORM]

After the Normal-Operation Initialization, the initialization software module is complete and stays in a wait loop. The program is completely interrupt-driven from this point on and only moves out of the wait loop when an interrupt occurs.

7.3 LANCE INTERRUPT EXCEPTION SOFTWARE MODULE

7.3.1 INTRODUCTION

The LANCE Interrupt Exception Module has basically four submodules. They are:

1. Interrupt Error Determination Submodule
2. Transmit Interrupt Handling Submodule
3. Receive Interrupt Handling Submodule
4. Initialization Done Interrupt Handling Submodule

Figure 31 depicts the flow of the Exception Software Module. The LANCE Interrupt Exception Software Module, also referred to as the LANCE Interrupt Routine, is called when the LANCE interrupts the host processor. The LANCE interrupts the host if a message has been transmitted or received, the LANCE has finished its initialization routine, or an error has occurred.

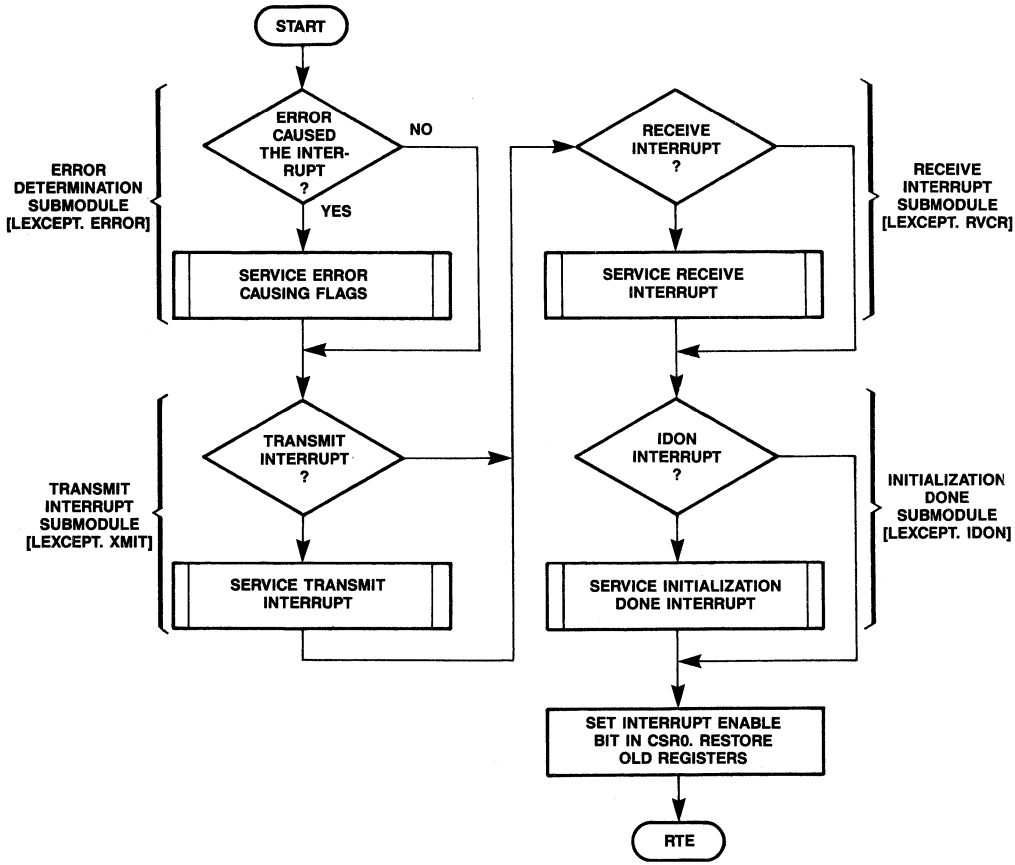


Figure 31. LANCE Exception Processing Module [LEXCEPT]

The LANCE interrupt is hardware set at level 6; the second highest priority. The only higher priority is level seven, that of the nonmaskable interrupt. When the LANCE interrupts the MK68000, it autovectors to memory location $800.

The first action the MK68000 takes is to get the LANCE's status from CSR0. This status helps determine what caused the interrupt. The error bit is the first bit checked. If this bit is not set, the Transmit Interrupt bit is checked to see if a transmitted message caused the interrupt. If an error did cause the interrupt, the software determines the type of error and the routine proceeds to the transmit interrupt check. Once the transmit bit is checked, the receive bit is checked in the same manner. Finally the Initialization Done bit is checked and the program returns to the waiting loop.

All flag-causing conditions are serviced and the error-causing conditions call application-dependent service subroutines. For the purposes of this Application Note, these error service routines simply set certain bits in memory that correspond to the error. The programmer may then examine memory for errors.

7.3.2 INTERRUPT ERROR DETERMINATION SUBMODULE

The first task in this submodule, as shown in Figure 32, is to save the registers. Information in the data and address registers is placed on the stack to be retrieved after exception processing. Next, status information in the Control and Status Register zero (CSR0) is moved into one of the MK68000's registers. Following this, all flags set in CSR0 and the Interrupt Enable bit are cleared. This occurs by clearing bit 6 (Interrupt Enable bit) in the register containing a copy of CSR0, and writing this copy back into CSR0. Since the flags are all cleared by writing a "1" in their bit location, all flags set in CSR0 are cleared. The Error bit in CSR0 clears itself after all the individual error flags are cleared. The interrupt enable bit is cleared by writing a "0" in its bit location. The LANCE's interrupt capabilities are disabled because it is not desirable to have another interrupt occur while the present interrupt from the LANCE is being serviced.

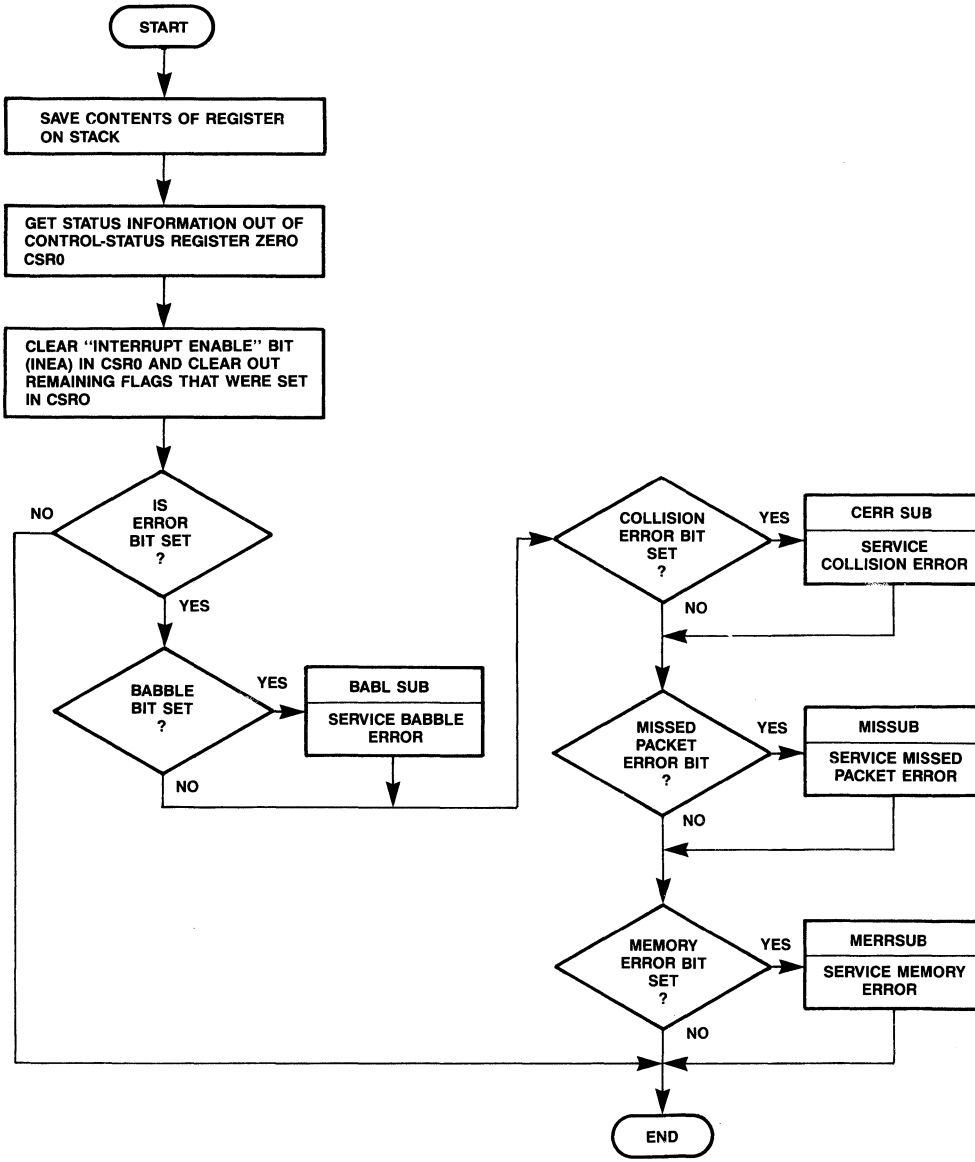


Figure 32. Interrupt Error Determination Submodule [LANCE. LEXCEPT. ERROR]

The Error Summary bit is the first status bit to be checked. If this bit is not set, no error-causing conditions are present and the individual error bits need not be checked. The Transmit Interrupt bit is checked next to see if it is set.

If the Error Summary bit is set, each individual error bit is checked. If any are set, an error-handling subroutine is called to report or service the error. Again, as stated before, these are application-dependent subroutines. The user can implement error handling routines to suit system requirements.

When it is determined whether an error caused the interrupt, the Transmit Interrupt bit is checked. Since more than one condition can cause the interrupt, all bits must be checked. The interrupt pin is simply an OR of the interrupt-causing conditions. If another interrupt occurs after the interrupt pin is asserted, another transition on the interrupt pin will not occur.

7.3.3 TRANSMIT INTERRUPT HANDLING SUBMODULE

If the Transmit Interrupt bit is set, the Transmit Interrupt Handling Submodule is executed (see Figure 33). First, the address pointer to the last transmit descriptor ring is retrieved from the ring management area. This address is incremented by two bytes so it points to the transmit status (TMD1). Next, the transmit status is moved into a MK68000 register. The "More" bit is checked to see if more than one transmission attempts were required. If so, the More counter in the ring management area is updated. The "One" bit is then checked to see if it took exactly one attempt to transmit the message. If so, the One counter is updated in a similar manner.

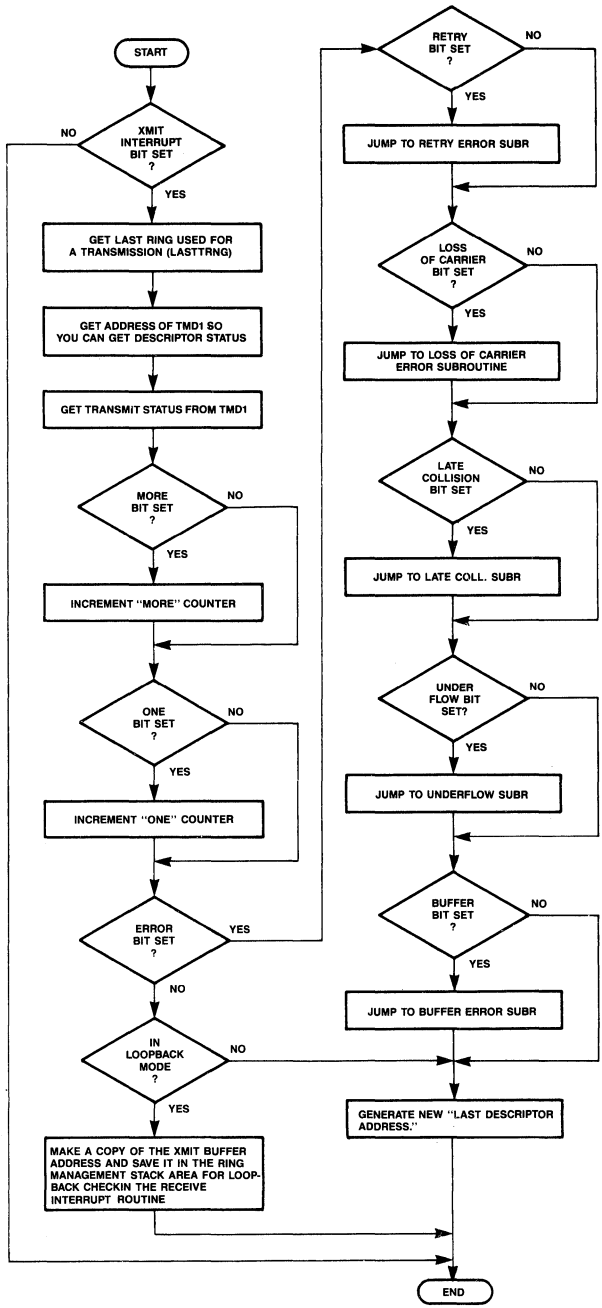


Figure 33. Transmit Interrupt Handling Submodule [LANCE. LEXCEPT. XMIT]

Next, the Transmit Error bit is tested to see if a transmission error occurred. As with the Interrupt Error bit in CSR0, if this bit is not set, it is not necessary to check each individual error bit, but if this Error Summary bit is set, the program does check each individual error bit. It checks the errors in the following order: retry error, loss of carrier error, late collision error, underflow error, and finally the buffer error. If any of these errors have occurred, the error handling subroutines are called to report and/or service the error-causing conditions.

If the transmission error summary bit is not set, the program checks to see if the LANCE is in the loopback mode. If this is true, a copy of the starting address of the transmit buffer is saved so the data in this buffer can be compared against data in the loopbacked message just received. This comparison indicates loopback mode status.

If the LANCE is in the loopback mode, the pointer to the last transmit descriptor is not incremented. This is because the descriptor buffer must not be available for additional messages until data in the transmit buffer is compared to that in the receive message buffer. This comparison occurs in the Receive Interrupt Handling Submodule of the module that is presently executing. At this time, the Last Transmit Descriptor pointer is updated.

In all other cases, before this submodule is complete, the last descriptor address pointer is updated to point to the next available descriptor. When the last descriptor address is updated, the present address pointed to must be compared with the bottom of the ring.

If the pointer is pointing to the bottom of the ring, it must not be simply incremented but, the address of the top of the ring must be placed in the pointer register. Once the Transmit Interrupt Handling Submodule is complete, the Receive Interrupt bit is checked in the CSR0 status.

7.3.4 RECEIVE INTERRUPT HANDLING SUBMODULE

The Receive Interrupt Handling Submodule, shown in Figure 34, is the most complicated piece of software in this program because it must handle loopback messages differently from a normal received message.

Two loopback situations can occur: One can occur during the diagnostic routine, and the other is the normal condition loopback. The latter loopback happens when the programmer desires to have external or internal loopback as a normal operating mode. This would most likely be the case during debut and system integration.

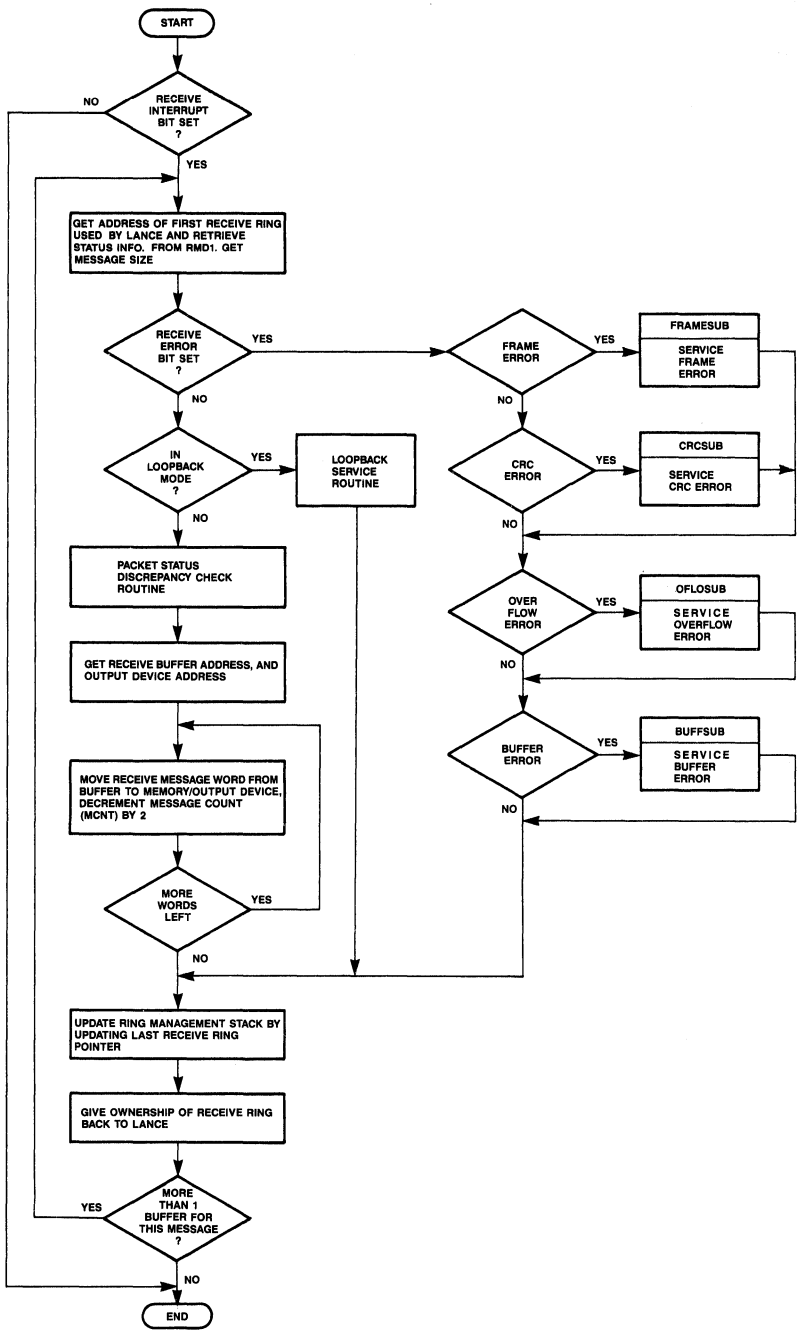


Figure 34. Receive Interrupt Handling Submodule [LANCE. LEXCEPT. RVCR]

If during CSR0 status checking the Receive Interrupt bit is set, the Receive Interrupt Handling Submodule is executed. The first step is to check the status of the receive message descriptor that the LANCE has turned over to the host by retrieving the Receive Descriptor pointer from the ring management area. Next, receive message descriptor number one (RMD1) is moved into one of the 68000's registers and the Receive Error Summary bit is checked. If this bit is set, the individual error bits are checked to see which error, or combination of errors, caused the error summary bit to be set. Error bits are checked in the following order: frame error, CRC error, overflow error, and buffer error.

If the Error Summary bit is not set, and LANCE is in the loopback mode, the loopback routine is executed (see Figure 35). The loopback routine is still part of the receive interrupt routine, but is listed separately for clarity.

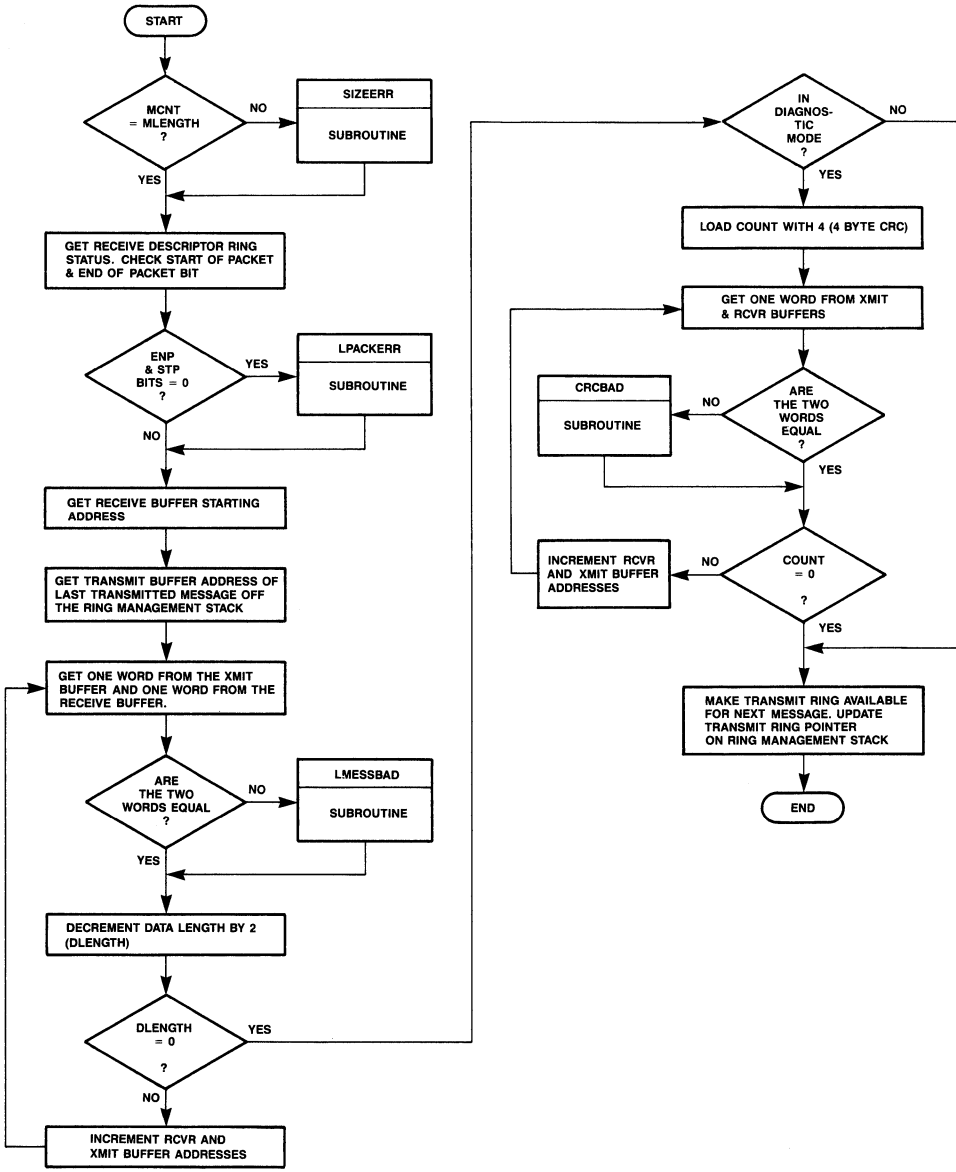


Figure 35. Loopback Service Routine [LANCE. LEXCEPT. RVCR. LOOPBACK]

7.3.4.1 LOOPBACK HANDLING ROUTINE

The first step in this routine is to check the received message length, which must be equal to the message sent, plus four bytes if transmit CRC is enabled. This is done by checking MCNT against the transmit message word (MLENGTH). The transmit message word length is in the ring management area (see Ring Management). The size of the transmit message is moved into MLENGTH when loopback occurs during the diagnostics.

In normal operation with the application breadboard, an arbitrary message size can be written into DLENGTH, followed by pushing the message interrupt button, and a message of that data size is transmitted.

If the message sizes do not match, an error subroutine is called. Next the packet check is made. In loopback mode, transmit data chaining cannot occur and the maximum received message size is 36 bytes. The receive buffers are larger than 36 bytes and since there must be only one packet per message, the start- and end-of-packet bits must be set. If both are not set, an error routine is called.

After the packet check, the receive and transmit buffer starting addresses are retrieved. The receive buffer address is taken from the receive descriptor, while the transmit buffer address is taken out of LOOPXADD from the Ring Management Area. LOOPXADD is moved into the Ring Management Area during the transmit interrupt routine. By using these addresses, the transmit and receive message data can be compared to verify proper transmission and reception. If any part of the message has been altered, an error subroutine is called.

When the entire message has been compared, the program checks if it is in the diagnostic mode. As stated previously, a software CRC is generated for the test message, and is compared to LANCE's hardware CRC. If any of the two do not match, an error subroutine is called. This comparison is only performed during diagnostics. If the program is in loopback, but not in diagnostics, this part of the routine is omitted.

After all comparisons are made, the transmit descriptor pointer is updated. The transmit descriptor pointer is not updated in the transmit interrupt routine because the descriptor points to the transmit buffer needed for the loopback data comparison. If the transmit buffer is made available before the data comparison, the buffer might be written over, thus invalidating the comparison.

7.3.4.2 RECEIVE INTERRUPT NORMAL OPERATION

If no errors are detected, and the LANCE is not in loopback, the receive interrupt routine proceeds normally. A packet check then searches for any errors with the start-of-packet and end-of-packet bits (see Figure 36). The ring management status register contains information on the status of these bits. A receive message coming in with the start-of-packet bit set and the end-of-packet bit not set indicates that more than one buffer contains the message. In this situation, the start-of-packet bit is set in the ring management status register. If the following descriptor contains another start-of-packet bit, an error flag is set since an end-of-packet has not been detected between the two start-of-packets. If the end-of-packet bit is set in the descriptor, the whole packet is received and the status register is set accordingly. The same holds true for two end-of-packets detected sequentially. If two end-of-packets are detected, without a start-of-packet in between them, an error flag is raised. These error flags call application-dependent subroutines to service the error.

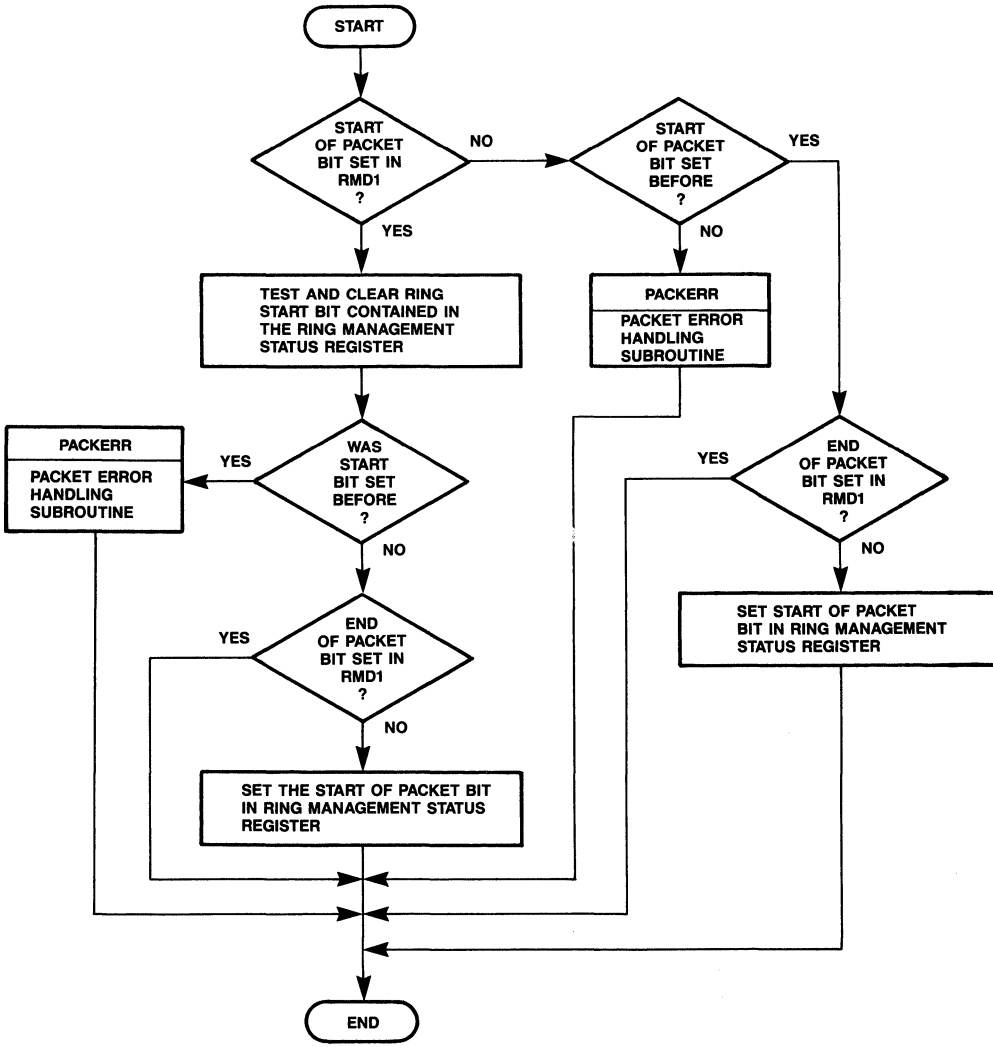


Figure 36. Packet Status Discrepancy Check Routine [LANCE. LEXCEPT. RCVR. PACKCHECK]

Once the packet check is complete, the received message is moved to an output device or to another memory location. Once moved, this layer of software no longer handles the message, instead the upper level software takes over. The upper level reformats the message and combines messages by sequence number as well as routing them to their final destination.

In this Application Note, the message is simply moved to another memory block. This can be accomplished effectively by changing the receive buffer starting address in the receive message descriptor to the address of an empty memory block. Then the used buffer address can be passed on to the next software layer. The same holds for transmitted messages. If the number of messages exceeds the number of available buffers, the host either rejects the last message and waits for a free buffer or moves the message into an empty memory block. When a descriptor is free, the host then changes the transmit buffer address in the descriptor.

The message is moved from the message buffer into the output memory a word at a time. Each time a word is moved, a count of the message length is decremented and checked to see if any messages still need to be transferred. Once the entire message is out of the buffer, the ring management area is updated by moving the last receive descriptor pointer to the next descriptor to be used by the LANCE. The LANCE again owns the buffer.

The start bit in the ring management area undergoes a final check. A set bit indicates that this receive buffer was only one of several buffers needed for the full message. If more buffers are associated with this message, a jump back to the beginning of the receive interrupt routine is made and the routine is executed again until the entire message is processed. If the start bit is not set, this was the only buffer needed for the message, thus, the routine is completed.

7.3.5 INITIALIZATION DONE INTERRUPT HANDLING SUBMODULE

The final submodule of the LANCE interrupt processing routine, shown in Figure 37, is the Initialization Done Interrupt Handling Submodule. This submodule determines if the host was interrupted because the LANCE had just completed initialization. CSR0 is checked to see if the IDON bit is set. If so, a flag-raising routine is called.

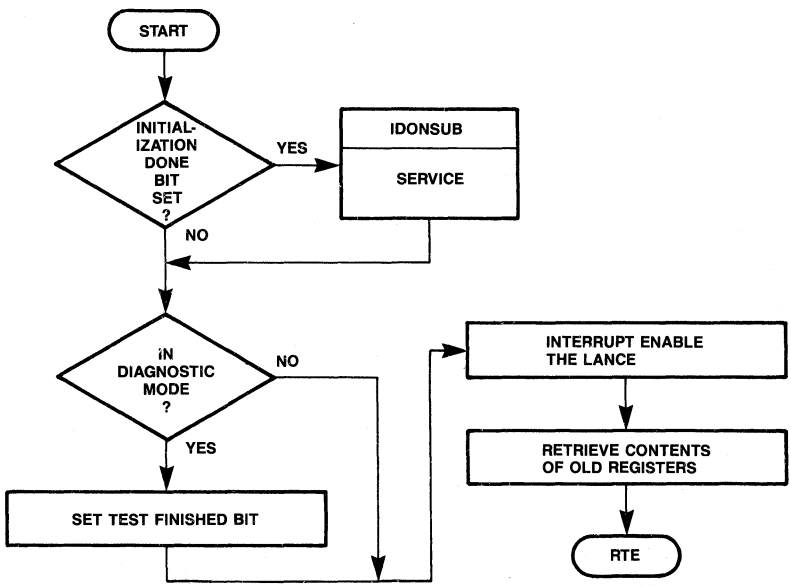


Figure 37. Initialization Done Interrupt Handling Submodule [LANCE. LEXCEPT. IDON]

The diagnostic bit in the ring management register is then checked. If the LANCE is in the diagnostic routine, the test done bit is set. The test done bit indicates a message has been loopbacked and checked and the next portion of the diagnostics may begin. This bit is checked after both a completed interrupt service routine and a Return From Exception.

At this point, all of the LANCE's interrupting conditions have been checked and serviced. During the exception processing, the LANCE's interrupting capabilities are disabled because another interrupt from the LANCE should not be performed while the first one is being serviced. Since servicing is complete the Interrupt Enable bit can again be set again in CSR0.

The module is concluded by moving the contents of the old registers off the stack and back into the register locations. A Return From Exception is then executed.

7.4 MESSAGE INTERRUPT SOFTWARE MODULE

The Message Interrupt Software Module, shown in Figure 38, is the routine that services the "push-button" message generator used in Aplication Note's hypothetical design. This push button is used for demonstration and debugging. The software description is included in this Application Note because the service routine is general enough to be adapted to any type of interrupt. The source of the interrupt may be anything, such as another processor controlling a terminal, a file server, or, as in this case, a push-button switch.

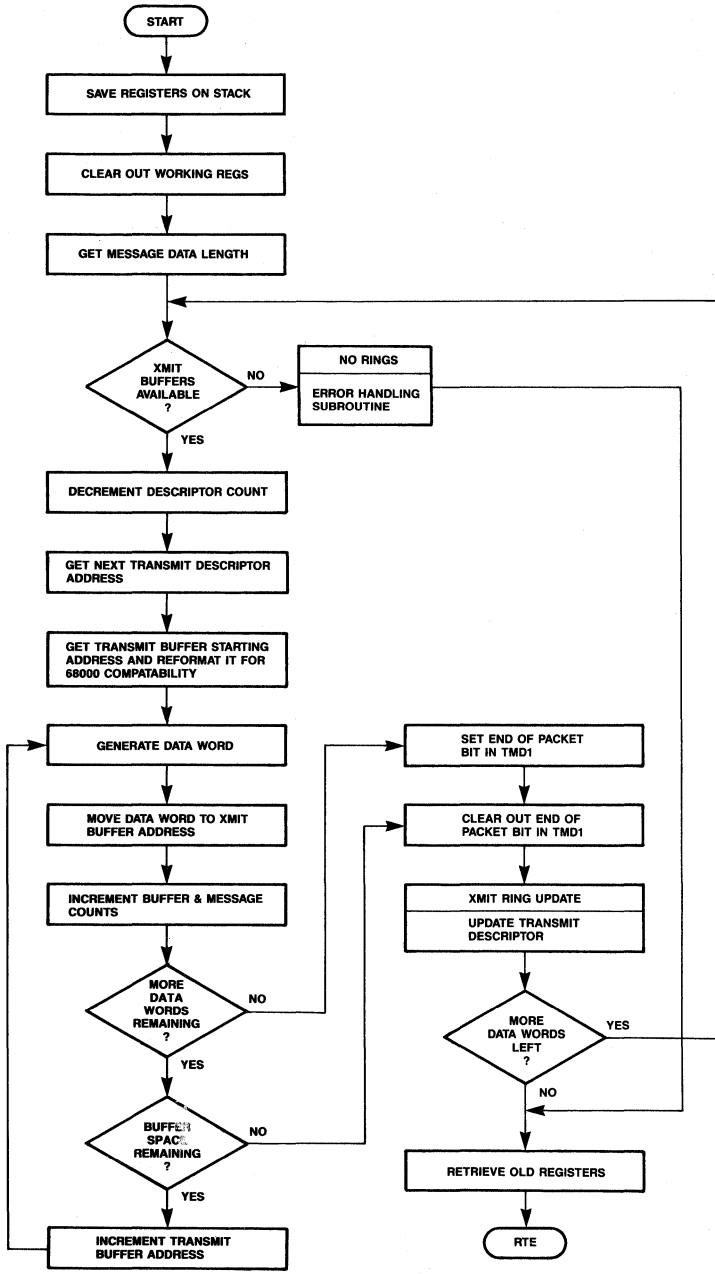


Figure 38. Message Interrupt Software Module [LANCE. MESSAGE]

There is, however, one major difference between this module and one used in real life. In addition to servicing the transmit message, this module also generates the message.

This module's basic function is to fill up as many transmit buffers as needed for the outgoing message, and to set the status information in the message descriptor accordingly.

The message interrupt is hardware set at interrupt level 5. Upon interrupt, the processor autovectors to memory location $0B00, the location of this module.

The software first saves the contents of the old registers and then clears the registers for use. Next, the message data length is retrieved from DLENGTH in the Ring Management Area. This message data length is manually written into before the message button is depressed.

Next, the Descriptor Count is checked for available transmit buffers. If none are available, an error subroutine is called, which sets an error bit in the status area, and the routine is over. If a buffer is available, the descriptor count is decremented and the Next Descriptor Ring address is moved into a register from the Ring Management Area. The Next Transmit Descriptor points to the descriptor of the next transmit buffer. The transmit buffer address is then moved in from the descriptor and reformatted for MK68000 compatability.

A message data word is then generated. The message consists of byte values ranging from zero to the hex value specified by DLENGTH. In other words, if the value $20 is written into DLENGTH and a message is generated, it consists of 32 bytes. The value of the first byte is $00, the second, $01, the third, $03, the 32nd, $1F, and so forth.

Each time a data word is generated, the transmit buffer address is incremented along with the buffer and message counts. The buffer count records how many bytes have been moved into the present transmit buffer. If the transmit message length exceeds the buffer size, more then one transmit buffer is used. The message count keeps track of the number of generated message words. If this amount equals DLENGTH, the message generation part of this module is complete.

If the transmit buffer is full, and more data words need to be generated, the transmit descriptor for that buffer is updated, and the rest of the message is placed in the next available transmit message buffer. In this case, the first transmit descriptor has the start-of-packet bit set, but the end-of-packet bit is not set. Figure 39 shows a flow chart of the transmit descriptor update submodule.

Once the entire message has been moved into the message buffer, or buffers, the last transmit descriptor is updated with the status information, along with a 2's complement of the number of bytes placed in its buffer. Finally, the old registers are retrieved, and a Return From Exception is executed.

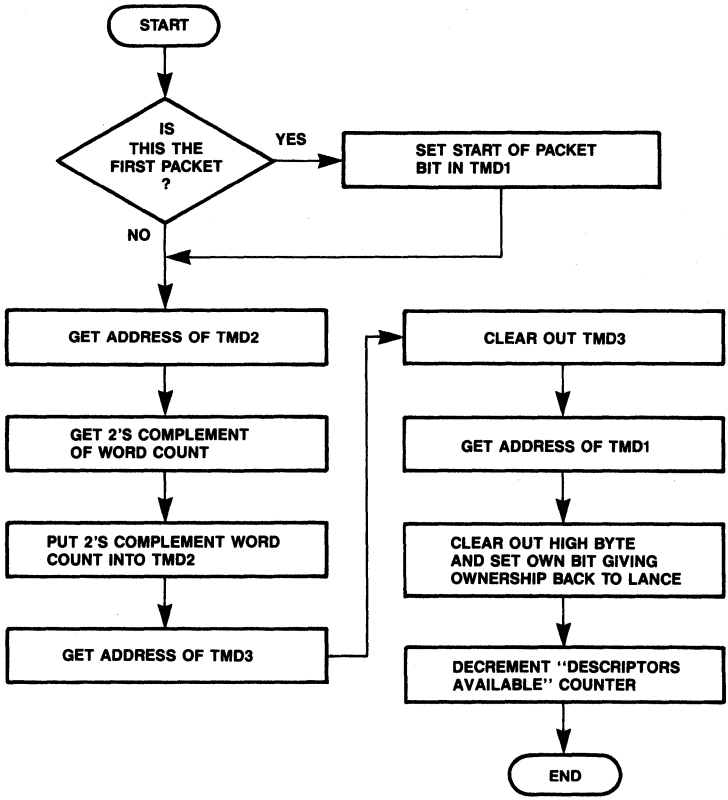


Figure 39. Transmit Ring Update Submodule [MESSAGE. XMIT RING UPDATE]

8.0 APPENDICES

Appendix A (paragraph 8.1) presents the initialization assembly code. Appendix B (paragraph 8.2) provides the LANCE interrupt assembly code. Appendix C (paragraph 8.3) addresses the message interrupt assembly code.

8.1 APPENDIX A, INITIALIZATION ASSEMBLY CODE

The following pages provide a listing of the initialization assembly code.

UNITED TECHNOLOGIES MOSTEK 68000 Assembler V1.4
Site 99994 MOSTEK
INITIAL.A68

```
Line S Location  Value          Source
   1 0
   2 0
   3 0
   4 0
   5 0                          ****************************************************************+
   6 0                          *+***************************************************************+*
   7 0                          **                                                               **
   8 0                          ** MODULE NAME:  INITIAL.                                        **
   9 0                          **                                                               **
  10 0                          ** AUTHOR:  JIM FONTAINE                                         **
  11 0                          **                                                               **
  12 0                          ** PROGRAM: LANCE                                                **
  13 0                          **                                                               **
  14 0                          ** LATEST REVISION DATE:  JANUARY 20,1984                         **
  15 0                          **                                                               **
  16 0                          ********************************************************************
  17 0                          **                                                               **
  18 0                          ** DESCRIPTION:  THIS MODULE WILL INITIALIZE THE ETHERNET NODE   **
  19 0                          ** AND MAKE IT OPERATIONAL.  THIS MODULE IS COMPOSED OF SIX      **
  20 0                          ** SUBMODULES.  THEY ARE: CLEAR, BLKMOVE, RRINGINIT, TRINGINIT,  **
  21 0                          ** DIAG, AND NORM.                                               **
  22 0                          ** THE CLEAR SUBMODULE CLEARS OUT THE WORKING REGISTERS, RESETS  **
  23 0                          ** THE SYSTEM,  DEFINES THE INTERRUPT VECTORS AND STACK          **
  24 0                          ** LOCATIONS. THE BLKMOVE SUBMODULE MOVES THE INITIALIZATION     **
  25 0                          ** BLOCK FROM PROGRAM MEMORY INTO THE MEMORY SPACE ALLOCATED FOR **
  26 0                          ** LANCE'S INITIALIZATION BLOCK. RRINGINIT SUBMODULE INITIALIZES **
  27 0                          ** THE RECEIVE MESSAGE DESCRIPTOR RINGS. THE TRINGINIT SUBMODULE **
  28 0                          ** INITIALIZES THE TRANSMIT MESSAGE DESCRIPTOR RINGS.  THE       **
  29 0                          ** DIAGNOSTIC SUBMODULE RUNS THROUGH A INTERNAL AND EXTERNAL     **
  30 0                          ** LOOPBACK ROUTINE TO TEST THE PROPER OPERATION OF THE LANCE    **
  31 0                          ** AND ADDITIONAL HARDWARE.  FINALLY, THE NORMAL SUBMODULE       **
  32 0                          ** INITIALIZES THE LANCE IN A NORMAL MODE OF OPERATION.          **
  33 0                          **                                                               **
  34 0                          ********************************************************************+
  35 0                          ****************************************************************+
  36 0
  37 0
  38 0                          ************************************************
  39 0                          *                                              *
  40 0                          *              EQUATE TABLE                    *
  41 0                          *                                              *
  42 0                          ************************************************
  43 0
  44 0                                  XREF     DATINTR
  45 0                                  XREF     LANINTR
  46 0
  47 0                          *   DESCRIPTOR RING STACK ALLOCATION   *
  48 0
  49 0
  50 0          00000000        RLEN     EQU      $00                ;38C0   RECEIVER RING LENGTH
  51 0          00000002        TLEN     EQU      $02                ;38C2   TRANSMIT RING LENGTH
```

```
Line S Location  Value         Source
  52 0           00000004      RRNGBASE EQU      $04              ;38C4   RECEIVER RING BASE ADDRESS
  53 0           00000008      TRNGBASE EQU      $08              ;38C8   TRANSMIT RING BASE ADDRESS
  54 0           0000000C      RRNGBOT  EQU      $0C              ;38CC   RECEIVER RING BOTTOM ADDRESS
  55 0           00000010      TRNGBOT  EQU      $10              ;38D0   TRANSMIT RING BOTTOM ADDRESS
  56 0           00000014      LASTRRNG EQU      $14              ;38D4   ADDRESS OF LAST RECEIVE RING USED
  57 0           00000018      LASTTRNG EQU      $18              ;38D8   ADDRESS OF LAST TRANSMIT RING USED
  58 0           0000001C      NEXTTRNG EQU      $1C              ;38DC   ADDRESS OF NEXT AVAILABLE TRANSMIT RING
  59 0           00000020      LOOPMCNT EQU      $20              ;38E0   MESSAGE COUNT OF LOOP MESSAGE
  60 0           00000022      TRINGCNT EQU      $22              ;3EE2   NUMBER OF TRANSMIT RINGS AVAILABLE TO USE
  61 0           00000024      RINGSTAT EQU      $24              ;38E4   RING STATUS
  62 0           00000028      LOOPXADD EQU      $28              ;38E8   ADDRESS OF LOOPBACK BUFFER
  63 0           0000002C      MORE     EQU      $2C              ;38EC   RUNING COUNT OF "MORE" FLAGS
  64 0           0000002E      ONE      EQU      $2E              ;38EE   RUNNING COUNT OF "ONE" FLAGS
  65 0           00000034      DLENGTH  EQU      $34              ;38F0   DESIRED MESSAGE DATA SIZE
  66 0           00000038      MLENGTH  EQU      $38              ;38F4   TOTAL LENGTH OF TRANSMITTED MESSAGE
  67 0
  68 0           00000100      BUFLEN   EQU      $0100            ;TRANSMIT & RECEIVE BUFFER LENGTH
  69 0           00000060      RBUFDIS  EQU      $0060            ;RECEIVER BUFFER DISPLACEMENT FROM DESCRIPT. RING
  70 0           00001020      TBUFDIS  EQU      $1020            ;XMIT BUFFER DISPLACEMENT FROM THE DESCRIPT RING
  71 0
  72 0
  73 0
  74 0                         *   MEMORY MAP LOCATIONS   *
  75 0
  76 0
  77 0           00002000      IADR     EQU      $2000            ;LANCES INITIALIZATION BLOCK BASE ADDRESS
  78 0           0000387C      STACK    EQU      $387C            ;STACK BASE ADDRESS
  79 0           000038C0      RINGSTK  EQU      $38C0            ;XMIT & RVCR USERS STACK BASE ADDRESS
  80 0
  81 0           00000044      MODE     EQU      $0044            ;ETHERNET MODE
  82 0           00000004      PADR1    EQU      $0004            ;PHYSICAL ADDRESS <00:15>
  83 0           00000000      PADR2    EQU      $0000            ;PHYSICAL ADDRESS <16:31>
  84 0           00000000      PADR3    EQU      $0000            ;PHYSICAL ADDRESS <32:47>
  85 0           00000008      LADR1    EQU      $0008            ;LOGICAL ADDRESS <00:15>
  86 0           00000000      LADR2    EQU      $0000            ;LOGICAL ADDRESS <16:31>
  87 0           00000000      LADR3    EQU      $0000            ;LOGICAL ADDRESS <32:47>
  88 0           00000000      LADR4    EQU      $0000            ;LOGICAL ADDRESS <48:63>
  89 0           00002018      RDRA1    EQU      $2018            ;RECEIVE DESCRIPTOR ADDRESS <00:15>
  90 0           00006000      RDRA2    EQU      $6000            ;RECEIVE DESCRIPTOR ADDRESS <16:23>
  91 0           00002058      TDRA1    EQU      $2058            ;TRANSMIT DESCRIPTOR ADDRESS <00:15>
  92 0           00004000      TDRA2    EQU      $4000            ;TRANSMIT DESCRIPTOR ADDRESS <16:23>
  93 0
  94 0           00004002      RAP      EQU      $4002            ;LANCE'S REGISTER ADDRESS PORT ADDRESS
  95 0           00004000      RDP      EQU      $4000            ;LANCE'S REGISTER DATA PORT ADDRESS
  96 0
  97 0
  98 0                         *   KEYWORD VALUE EQUATES   *
  99 0
 100 0
 101 0           00000000      CSR0     EQU      $00              ;ADDRESS OF CONTROL-STATUS REGISTER 0
 102 0           00000001      CSR1     EQU      $01              ;ADDRESS OF CONTROL-STATUS REGISTER 1
```

```
Line S Location  Value          Source
 103 0           00000002       CSR2     EQU      $02                ;ADDRESS OF CONTROL-STATUS REGISTER 2
 104 0           00000003       CSR3     EQU      $03                ;ADDRESS OF CONTROL-STATUS REGISTER 3
 105 0
 106 0                          *   WORD VALUE DEFINITION   *
 107 0
 108 0
 109 0                                   XDEF     RAP
 110 0                                   XDEF     RDP
 111 0
 112 0                                   XDEF     CSR0
 113 0                                   XDEF     CSR1
 114 0                                   XDEF     CSR2
 115 0                                   XDEF     CSR3
 116 0
 117 0                                   XDEF     RLEN
 118 0                                   XDEF     TLEN
 119 0                                   XDEF     RRNGBASE
 120 0                                   XDEF     TRNGBASE
 121 0                                   XDEF     RRNGBOT
 122 0                                   XDEF     TRNGBOT
 123 0                                   XDEF     LASTRRNG
 124 0                                   XDEF     LASTTRNG
 125 0                                   XDEF     NEXTTRNG
 126 0                                   XDEF     LOOPMCNT
 127 0                                   XDEF     TRINGCNT
 128 0                                   XDEF     RINGSTAT
 129 0                                   XDEF     MORE
 130 0                                   XDEF     ONE
 131 0                                   XDEF     LOOPXADD
 132 0                                   XDEF     DLENGTH
 133 0                                   XDEF     TBUFLEN
 134 0                                   XDEF     MLENGTH
 135 0
 136 0                                   XDEF     DIAG
 137 0
 138             00000400                ORG      $400
 139
 140                            ********** MAIN PROGRAM **********************
 141
 142
 143                            ****************************************************
 144                            *                                                  *
 145                            *      INITIAL.CLEAR                               *
 146                            *      INITIALIZE MK68000 AND CLEAR REGISTERS      *
 147                            *                                                  *
 148                            ****************************************************
 149
 150
 151
 152   00000400 46FC2700        CLEAR    MOVE.W   #$2700,SR          SET UP STATUS REGISTER
 153   00000404 4E70                     RESET                        RESET THE 68000
```

```
Line S Location  Value          Source
 154
 155                            ***   CLEAR  ALL  DATA  REGISTERS   ***
 156
 157   00000406 4280                    CLR.L    D0                  CLEAR OUT DATA REG D0
 158   00000408 4281                    CLR.L    D1                  CLEAR OUT DATA REG D1
 159   0000040A 4282                    CLR.L    D2                  CLEAR OUT DATA REG D2
 160   0000040C 4283                    CLR.L    D3                  CLEAR OUT DATA REG D3
 161   0000040E 4284                    CLR.L    D4                  CLEAR OUT DATA REG D4
 162   00000410 4285                    CLR.L    D5                  CLEAR OUT DATA REG D5
 163   00000412 4286                    CLR.L    D6                  CLEAR OUT DATA REG D6
 164   00000414 4287                    CLR.L    D7                  CLEAR OUT DATA REG D7
 165
 166                            ***   CLEAR  ADDRESS  REGISTERS  A0 AND A4   ***
 167
 168   00000416 2040                    MOVE.L   D0,A0               CLEAR ADDRESS REG A0
 169   00000418 2240                    MOVE.L   D0,A1               CLEAR ADDRESS REG A1
 170   0000041A 2440                    MOVE.L   D0,A2               CLEAR ADDRESS REG A2
 171   0000041C 2640                    MOVE.L   D0,A3               CLEAR ADDRESS REG A3
 172   0000041E 2840                    MOVE.L   D0,A4               CLEAR ADDRESS REG A4
 173
 174                            ***   DEFINE STACK AND INTERRUPT VECTOR LOCATIONS   ***
 175
 176
 177   00000420 207C00000078            MOVE.L   #$78,A0             DEFINE VECTOR FOR "LANCE" INTERRUPT
 178   00000426 20BCFFFFFFFF            MOVE.L   #LANINTR,(A0)       MOVE VECTOR LOCATION TO LOCATION $78
 179   0000042C 207C00000074            MOVE.L   #$74,A0             DEFINE VECTOR FOR "DATA FOR XMIT" INTERRUPT
 180   00000432 20BCFFFFFFFF            MOVE.L   #DATINTR,(A0)       MOVE VECTOR LOCATION TO LOCATION $74
 181   00000438 287C0000038C0           MOVE.L   #RINGSTK,A4         MOVE RING STACK LOCATION TO REGISTER A4
 182   0000043E 207C0000387C            MOVE.L   #STACK,A0           MOVE STACK LOCATION TO A0
 183   00000444 4E60                    MOVE.L   A0,USP              MOVE STACK LOCATION TO USER STACK POINTER
 184   00000446 46FCA400                MOVE.W   #$A400,SR           SET UP MASK IN STATUS REGISTER
 185   0000044A 29400028                MOVE.L   D0,LOOPXADD(A4)     CLEAR OUT LOOP ADDRESS ON STACK
 186   0000044E 19400024                MOVE.B   D0,RINGSTAT(A4)     CLEAR OUT RING STATUS
 187   00000452 3940002E                MOVE.W   D0,ONE(A4)          CLEAR OUT THE ONE'S COUNTER
 188   00000456 3940002C                MOVE.W   D0,MORE(A4)         CLEAR OUT THE MORE'S COUNTER
 189   0000045A 39400020                MOVE.W   D0,LOOPMCNT(A4)     CLEAR OUT THE MESSAGE COUNT
 190
 191                            ********************************************************
 192                            *                                                      *
 193                            *      INITIAL.BLKMOVE                                 *
 194                            *      MOVE INITIALIZATION BLOCK                       *
 195                            *                                                      *
 196                            ********************************************************
 197
 198
 199   0000045E 207C0000071C            MOVE.L   #PROGIADR,A0        GET STARTING ADDRESS OF PROGRAM INIT. BLOCK
 200   00000464 227C00002000            MOVE.L   #IADR,A1            GET STARTING ADDRESS OF LANCE INIT. BLOCK
 201
 202   0000046A 2290            RETURN  MOVE.L   (A0),(A1)           MOVE LONG WORD OF PROG BLOCK INTO LANCE BLOCK
 203   0000046C 0C04000F                CMPI.B   #15,D4              SEE IF WE ARE UP TO ADDRESS IADR <23:00>+20 (OCT)
 204   00000470 6E00000A                BGT      COUNT16             IF SO BRANCH TO COUNT = 16
```

```
Line S Location  Value      Source
 205   00000474 5848       INCREM   ADD      #04,A0          INCREMENT THE PROGRAM INIT BLOCK ADDRESS BY 4
 206   00000476 5849                ADD      #04,A1          INCREMENT THE LANCE INIT BLOCK ADDRESS IN A1 BY 4
 207   00000478 5844                ADD      #04,D4          INCREMENT COUNTER BY 4
 208   0000047A 60EE                BRA      RETURN          GO BACK AND LOAD THE NEXT LONG WORD
 209   0000047C 0C040010  COUNT16   CMPI.B   #16,D4          SEE IF THE COUNT IS EQUAL TO 16
 210   00000480 66000030            BNE      COUNT20         IF NOT BRANCH TO COUNT = 20
 211
 212                      ***   RECEIVE RING LENGTH CALCULATION   ***
 213
 214   00000484 2010                MOVE.L   (A0),D0         MOVE RECEIVE RING ADDRESS AND LENGTH TO D0
 215   00000486 E758                ROL.W    #3,D0           MOVE RECEIVE LENGTH TO LOWER BYTE OF LONG WORD
 216   00000488 1200                MOVE.B   D0,D1           SAVE A COPY OF CODED RECEIVER RING LENGTH IN REG D1
 217   0000048A 02010007            ANDI.B   #$07,D1         CLEAR OUT EVERYTHING EXCEPT FOR THE LENGTH
 218   0000048E 7A01                MOVEQ    #01,D5          LOAD REG D1 WITH  1 FOR CALC. RING LENGTH
 219   00000490 04010001  NXTPOWER  SUBI.B   #01,D1          DECREMENT LENGTH COUNT
 220   00000494 6D06                BLT.S    CALCDONE        IF COUNTER IS LESS THAT "0" CALCULATION IS FINISHED
 221   00000496 CAFC0002            MULU     #2,D5           MULTIPLY BY 2 TO CALCULATE POWER
 222   0000049A 60F4                BRA.S    NXTPOWER        CALCULATE NEXT POWER OF 2
 223
 224   0000049C 3885       CALCDONE MOVE.W   D5,RLEN(A4)     MOVE RECEIVER LENGTH OUT ONTO THE RING STACK
 225   0000049E E658                ROR.W    #3,D0           MOVE THE WORD BACK INTO ORIGINAL POSISION
 226   000004A0 024000FF            ANDI.W   #$00FF,D0       CLEAR OUT THE STATUS FOR THE ADDRESS WORD
 227   000004A4 4840                SWAP     D0              REFORMAT THE WORDS FOR 68000 COMPATABILITY
 228   000004A6 29400004            MOVE.L   D0,RRNGBASE(A4) PUT RECEIVE DESCRIPTOR BASE ADDRESS ON RING STACK
 229   000004AA 29400014            MOVE.L   D0,LASTRRNG(A4) PUT RVCR DESCRIPTOR BASE ADDRESS IN LAST RVCR RING SPOT
 230   000004AE 2A40                MOVE.L   D0,A5           SAVE A COPY OF THE RVCR RING BASE ADD. IN REG A5
 231   000004B0 60C2                BRA      INCREM          GO INCREMENT THE REGISTERS
 232
 233                      ***   TRANSMIT RING LENGTH CALCULATION   ***
 234
 235   000004B2 2010       COUNT20  MOVE.L   (A0),D0         MOVE TRANSMIT RING ADDRESS AND LENGTH TO D0
 236   000004B4 E758                ROL.W    #3,D0           MOVE XMIT LENGTH TO LOWER BYTE OF LONG WORD
 237   000004B6 1200                MOVE.B   D0,D1           MAKE A COPY OF CODED XMIT RING LENGTH IN REG D1
 238   000004B8 02010007            ANDI.B   #$07,D1         CLEAR OUT EVERYTHING EXCEPT FOR THE LENGTH
 239
 240   000004BC 7C01                MOVEQ    #01,D6          LOAD REG D1 WITH 1 FOR CALC. RING LENGTH
 241   000004BE 04010001  NXPOWER   SUBI.B   #01,D1          DECREMENT LENGTH COUNT
 242   000004C2 6D06                BLT.S    CALCDNE         IF COUNTER IS LESS THAT "0" CALCULATION IS FINISHED
 243   000004C4 CCFC0002            MULU     #2,D6           MULTIPLY BY 2 TO CALCULATE POWER
 244   000004C8 60F4                BRA.S    NXPOWER         CALCULATE NEXT POWER OF 2
 245
 246   000004CA 39460002  CALCDNE   MOVE.W   D6,TLEN(A4)     MOVE XMIT LENGTH OUT ONTO THE RING STACK
 247   000004CE 39460022            MOVE.W   D6,TRINGCNT(A4) MOVE XMIT RING COUNT OUT TO "COUNTER STACK LOCATION
 248   000004D2 E658                ROR.W    #3,D0           MOVE THE WORD BACK INTO ORIGINAL POSITION
 249   000004D4 024000FF            ANDI.W   #$00FF,D0       CLEAR THE STATUS OUT OF THE ADDRESS WORD
 250   000004D8 4840                SWAP     D0              REFORMAT THE WORDS FOR 68000 COMPATABILITY
 251   000004DA 29400008            MOVE.L   D0,TRNGBASE(A4) PUT XMIT DESCRIPTOR BASE ADDRESS ON RING STACK
 252   000004DE 2940001C            MOVE.L   D0,NEXTTRNG(A4) PUT XMIT DESCRIPTOR BASE ADD IN NEXT RING SPOT
 253   000004E2 29400018            MOVE.L   D0,LASTTRNG(A4) PUT A COPY OF XMIT DESCR. ADD. IN LAST RING SPOT
 254   000004E6 2C40                MOVE.L   D0,A6           SAVE A COPY OF THE BASE ADDRESS IN REG A6
 255
```

```
Line S Location  Value          Source
 256
 257                            ********************************************************
 258                            *                                                      *
 259                            *    INITIAL.RRINGINIT                                 *
 260                            *    INITIALIZE THE RECEIVE MESSAGE DESCRIPTOR RINGS   *
 261                            *                                                      *
 262                            ********************************************************
 263
 264                            ***   GENERATE RMD0, AND RMD1   ***
 265
 266   000004E8 220D                    MOVE.L   A5,D1               GET COPY OF RVCR RING BASE ADD. AND PUT IT IN D1
 267   000004EA 068100000060            ADD.L    #RBUFDIS,D1         GENERATE RECEIVE BUFFER ADDRESS BY ADDING DISPLACEMENT
 268   000004F0 2401                    MOVE.L   D1,D2               COPY
 269   000004F2 600A                    BRA.S    FIRSTRCV            GO INITIALIZE FIRST RECEIVE RING
 270
 271   000004F4 588D              NEXTRRNG ADDQ.L   #$04,A5           GENERATE NEXT ADDRESS OF MESSAGE DESCRIPTOR
 272   000004F6 068200000100            ADDI.L   #BUFLEN,D2          INCREMENT THE BUFFER DISPLACEMENT WITH BUFFER LENGTH
 273   000004FC 2202                    MOVE.L   D2,D1
 274   000004FE 008180000000      FIRSTRCV ORI.L    #$80000000,D1       SET OWN BIT IN DESCRIPTOR WORD
 275   00000504 4841                    SWAP     D1                  MAKE WORDS COMPATABILITY WITH 68000 FORMAT
 276   00000506 2A81                    MOVE.L   D1,(A5)             MOVE LONG WORD INTO DESCRIPTOR RING ADDRESS
 277
 278                            ***   GENERATE RMD2, AND RMD3   ***
 279
 280   00000508 588D                    ADDQ.L   #$04,A5             GENERATE NEXT ADDRESS OF DESCRIPTOR WORD
 281   0000050A 203C00000100            MOVE.L   #BUFLEN,D0          GET RING BUFFER LENGTH
 282   00000510 0A40FFFF                EORI.W   #$FFFF,D0           GET 2'S COMPLEMENT BY EXCLUSIVE ORING AND,
 283   00000514 06400001                ADDI.W   #$01,D0             ADDING 1 TO THE RESULT. THIS GIVES BYTE COUNT
 284   00000518 4840                    SWAP     D0                  MAKE WORDS CAMPATABILITY WITH 68000 FORMAT
 285   0000051A 2A80                    MOVE.L   D0,(A5)             MOVE LONG WORD TO MESSAGE DESCRIPTOR 2 AND 3
 286
 287                            ***   GENERATE NEXT RECEIVE DESCRIPTOR RING   ***
 288
 289   0000051C 04050001                SUBI.B   #$01,D5             DECREMENT THE RECEIVER RING COUNT
 290   00000520 66D2                    BNE.S    NEXTRRNG            IF THERE IS STILL ANOTHER RING LEFT, GO INIT. IT
 291   00000522 598D                    SUBQ.L   #$04,A5             OR, POINT BACK TO THE BEGINING OF THE ADDRESS
 292   00000524 294D000C                MOVE.L   A5,RRNGBOT(A4)      MOVE IT OUT ONTO THE RING STACK
 293
 294                            ********************************************************
 295                            *                                                      *
 296                            *    INITIAL.TRINGINIT                                 *
 297                            *    INITIALIZE THE TRANSMIT MESSAGE DESCRIPTOR RINGS  *
 298                            *                                                      *
 299                            ********************************************************
 300
 301                            ***   GENERATE TMD0, AND TMD1   ***
 302
 303   00000528 220E                    MOVE.L   A6,D1               GET XMIT RING BASE ADDRESS AND PUT IT IN D1
 304   0000052A 068100001020            ADD.L    #TBUFDIS,D1         GENERATE XMIT BUFFER ADDRESS BY ADDING DISPLACEMENT
 305   00000530 2401                    MOVE.L   D1,D2               COPY IT
 306   00000532 600A                    BRA.S    FIRSTXM             GO GENERATE FIRST TRANSMIT RING
```

```
Line S Location  Value          Source
 307
 308   00000534 588E           NXTTRNG  ADDQ.L   #$04,A6              GENERATE NEXT ADDRESS OF MESSAGE DESCRIPTOR
 309   00000536 068200000100            ADDI.L   #BUFLEN,D2
 310   0000053C 2202                    MOVE.L   D2,D1
 311   0000053E 4841           FIRSTXM  SWAP     D1
 312   00000540 2C81                    MOVE.L   D1,(A6)               MOVE LONG WORD INTO DESCRIPTOR RING ADDRESS
 313
 314                           ****   GENERATE TMD2, AND TMD3   ***
 315
 316   00000542 588E                    ADDQ.L   #$04,A6               GENERATE NEXT ADDRESS OF DESCRIPTOR WORD
 317   00000544 203C00000100            MOVE.L   #BUFLEN,D0            GET RING BUFFER LENGTH
 318   0000054A 0A40FFFF                EORI.W   #$FFFF,D0             GET 2'S COMPLEMENT BY EXCLUSIVE ORING AND,
 319   0000054E 06400001                ADDI.W   #$01,D0               ADDING 1 TO THE RESULT. THIS GIVES BYTE COUNT
 320   00000552 4840                    SWAP     D0                    REFORMAT FOR 68000 COMPATABILITY
 321   00000554 2C80                    MOVE.L   D0,(A6)               MOVE LONG WORD TO MESSAGE DESCRIPTOR 2 AND 3
 322
 323                           ***   GENERATE NEXT TRANSMIT DESCRIPTOR RING   ***
 324
 325   00000556 04060001                SUBI.B   #$01,D6               DECREMENT THE MESSAGE RING COUNT
 326   0000055A 66D8                    BNE.S    NXTTRNG               IF THERE IS STILL ANOTHER RING LEFT, GO INIT. IT
 327   0000055C 598E                    SUBQ.L   #$04,A6               POINT BACK TO THE BEGINNING OF THE ADDRESS
 328   0000055E 294E0010                MOVE.L   A6,TRNGBOT(A4)        GO MOVE IT OUT ONTO THE STACK
 329
 330                           ** CALL DIAGNOSTICS ROUTINE **
 331
 332   00000562 4EB90000059A            JSR      DIAG                  CALL DIAGNOSTICS SUBROUTINE
 333
 334
 335                           ********************************************************
 336                           *                                                      *
 337                           *      INITIAL.NORM                                    *
 338                           *      INITIALIZES FOR NORMAL OPERATION                *
 339                           *                                                      *
 340                           ********************************************************
 341
 342                           ***   SET UP FOR NORMAL OPERATION   ***
 343
 344   00000568 207C0000071C            MOVE.L   #PROGIADR,A0          GET STARTING ADDRESS OF PROGRAM INIT. BLOCK
 345   0000056E 2290                    MOVE.L   (A0),(A1)             MOVE MODE INFORMATION INTO INIT BLOCK
 346
 347                           *   LOOPBACK CHECKING   *
 348   00000570 397C00000024            MOVE.W   #0,RINGSTAT(A4)       CLEAR OUTRING STATUS REGISTER
 349   00000576 3010                    MOVE.W   (A0),D0               GET MODE INFORMATION AND PUT IN REG D0
 350   00000578 08000002                BTST     #02,D0                SEE IF WE ARE IN LOOPBACK MODE
 351   0000057C 6712                    BEQ.S    GOINIT                IF NOT GO INITIALIZE THE CSR REGISTERS
 352   0000057E 08EC00010024            BSET.B   #01,RINGSTAT(A4)      IF SO, SET THE LOOP STATUS BIT
 353   00000584 08000006                BTST     #06,D0                SEE IF WE ARE IN INTERNAL LOOPBACK
 354   00000588 6706                    BEQ.S    GOINIT                IF NOT, GO INITIALIZE THE CSR REGISTERS
 355   0000058A 08EC00000024            BSET.B   #00,RINGSTAT(A4)      IF SO, SET THE INTERNAL LOOP STATUS BIT
 356   00000590 4EB9000006CC   GOINIT   JSR      CSRINIT               GO START UP THE LANCE
 357
```

```
Line S Location  Value          Source
 358   00000596 4E71           WAIT     NOP                          WAIT HERE UNTIL AN INTERRUPT OCCURS
 359   00000598 60FC                    BRA      WAIT                WAIT SOME MORE
 360
 361
 362
 363                           ********************************************************
 364                           *                                                      *
 365                           *      INITIAL.DIAG                                    *
 366                           *      LANCE DIAGNOSTIC ROUTINE                        *
 367                           *                                                      *
 368                           ********************************************************
 369
 370                           ***   DIAGNOSTIC MESSAGE GENERATION   ***
 371
 372   0000059A 4281           DIAG     CLR.L    D1                  CLEAR OUT REGISTER D1
 373   0000059C 4282                    CLR.L    D2                  CLEAR OUT REGISTER D2
 374   0000059E 227C00002000            MOVE.L   #IADR,A1            GET INITIALIZATION STARTING ADDRESS
 375   000005A4 08EC00040024            BSET.B   #04,RINGSTAT(A4)    SET DIAGNOSTIC BIT IN STATUS REG
 376
 377   000005AA 08EC00010024            BSET.B   #01,RINGSTAT(A4)    SET THE LOOP STATUS BIT
 378   000005B0 08EC00000024            BSET.B   #00,RINGSTAT(A4)    SET THE INTERNAL LOOP STATUS BIT
 379
 380   000005B6 206C001C                MOVE.L   NEXTTRNG(A4),A0     GET XMIT RING BASE ADDRESS
 381   000005BA 2610                    MOVE.L   (A0),D3             GET XMIT BUFFER BASE ADDRESS
 382   000005BC 024300FF                ANDI.W   #$00FF,D3           CLEAR STATUS OUT OF WORD
 383   000005C0 2A03                    MOVE.L   D3,D5               MAKE A COPY OF IT
 384   000005C2 4843                    SWAP     D3                  MOVE WORDS FOR 68000 COMPATABILITY
 385   000005C4 2643                    MOVE.L   D3,A3               MOVE XMIT BUFFER ADDRESS INTO ADD REG
 386   000005C6 26BCAAAAAAAA   MESS     MOVE.L   #$AAAAAAAA,(A3)     MOVE TEST MESSAGE WORD INTO BUFFER ADDRESS
 387   000005CC 5841                    ADDQ.W   #04,D1              INCREMENT MESSAGE COUNTER BY 4 (BYTES)
 388   000005CE 584B                    ADDQ.W   #04,A3              INCREMENT THE BUFFER ADDRESS
 389   000005D0 0C41001C                CMP.W    #$1C,D1             CHECK TO SEE IF THE MESSAGE IS 28 BYTES LONG
 390   000005D4 6DF0                    BLT.S    MESS                IF SO, GO ADD MORE TO THE MESSAGE
 391   000005D6 4EB900000706            JSR      CRCGEN              JUMP TO SOFTWARE CRC GENERATOR
 392   000005DC 397C00200038            MOVE.W   #$20,MLENGTH(A4)    MOVE A MESSAGE LENGTH OF 32 BYTES OUT TO
 393                           *                                     RING MANG. AREA FOR LATER COMPARISON
 394   000005E2 397C001C0034            MOVE.W   #$1C,DLENGTH(A4)    MOVE DATA SIZE OUT FOR LATER COMPARISON
 395
 396
 397                           ***  TEST INTERNAL LOOPBACK WITH TRANSMIT CRC ENABLED   ***
 398
 399   000005E8 00458300                ORI.W    #$8300,D5           SET OWNERSHIP BIT IN XMIT RING
 400   000005EC 2085                    MOVE.L   D5,(A0)             MOVE TMD1 TO RING LOCATION
 401   000005EE 5888                    ADDQ.L   #04,A0              GENERATE ADDRESS OF TMD2
 402   000005F0 20BCFFE40000            MOVE.L   #$FFE40000,(A0)     MOVE BYTE COUNT(28 BYTES) TO TMD2 ON DESCRIPTOR
 403                           *                                     RING AND CLEAR OUT TMD3
 404   000005F6 5588                    SUBQ.L   #02,A0              POINT TO TMD1
 405   000005F8 32BC8044                MOVE.W   #$8044,(A1)         SET UP INIT BLOCK TO INTERNAL LOOPBACK
 406   000005FC 4EB9000006CC            JSR      CSRINIT             GO START UP THE LANCE
 407   00000602 08AC00050024   CHECK1   BCLR.B   #05,RINGSTAT(A4)    SEE IF THIS PORTION OF THE TEST IS COMPLETE
 408   00000608 67F8                    BEQ      CHECK1              CHECK AGAIN
```

UNITED TECHNOLOGIES MOSTEK 68000 Assembler V1.4
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INITIAL.A68

```
Line S Location  Value          Source
 409
 410                            ***   TURN OFF THE LANCE   ***
 411   0000060A 247C00004002            MOVE.L   #RAP,A2              SELECT LANCE'S REGISTER ADDRESS PORT TO WRITE TO
 412   00000610 34BC0000                MOVE.W   #CSR0,(A2)           LOAD REGISTER ADDRESS PORT OF LANCE WITH CSR0
 413   00000614 267C00004000            MOVE.L   #RDP,A3              SELECT LANCE'S REGISTER DATA PORT TO WRITE TO
 414   0000061A 36BC00FF                MOVE.W   #$00FF,(A3)          TURN OFF THE LANCE
 415
 416                            ***   TEST INTERNAL LOOPBACK WITH TRANSMIT CRC DISABLED   ***
 417
 418   0000061E 00458300                ORI.W    #$8300,D5            SET OWNERSHIP BIT IN XMIT RING
 419   00000622 3085                    MOVE.W   D5,(A0)              MOVE TMD1 TO RING LOCATION
 420   00000624 5488                    ADDQ.L   #02,A0               GENERATE ADDRESS OF TMD2
 421   00000626 20BCFFE00000            MOVE.L   #$FFE00000,(A0)      MOVE BYTE COUNT(32 BYTES) TO TMD2 ON DESCRIPTOR
 422                            *                                     RING AND CLEAR OUT TMD3
 423   0000062C 5588                    SUBQ.L   #02,A0               POINT TO TMD1
 424   0000062E 32BC804C                MOVE.W   #$804C,(A1)          SET UP INIT BLOCK TO INTERNAL LOOPBACK
 425   00000632 4EB9000006CC            JSR      CSRINIT              GO START UP THE LANCE
 426   00000638 08AC00050024  CHECK2    BCLR.B   #05,RINGSTAT(A4)     SEE IF THIS PORTION OF THE TEST IS COMPLETE
 427   0000063E 67F8                    BEQ      CHECK2               CHECK AGAIN
 428
 429                            ***   TURN OFF THE LANCE   ***
 430   00000640 247C00004002            MOVE.L   #RAP,A2              SELECT LANCE'S REGISTER ADDRESS PORT TO WRITE TO
 431   00000646 34BC0000                MOVE.W   #CSR0,(A2)           LOAD REGISTER ADDRESS PORT OF LANCE WITH CSR0
 432   0000064A 267C00004000            MOVE.L   #RDP,A3              SELECT LANCE'S REGISTER DATA PORT TO WRITE TO
 433   00000650 36BC00FF                MOVE.W   #$00FF,(A3)          TURN OFF THE LANCE
 434
 435                            ***   TEST INTERNAL LOOPBACK WITH XMIT CRC ENABLED AND COLLISION FORCE ON ***
 436
 437   00000654 00458300                ORI.W    #$8300,D5            SET OWNERSHIP BIT IN XMIT RING
 438   00000658 3085                    MOVE.W   D5,(A0)              MOVE TMD1 TO RING LOCATION
 439   0000065A 5488                    ADDQ.L   #02,A0               GENERATE ADDRESS OF TMD2
 440   0000065C 20BCFFE40000            MOVE.L   #$FFE40000,(A0)      MOVE BYTE COUNT(28 BYTES) TO TMD2 ON DESCRIPTOR
 441                            *                                     RING AND CLEAR OUT TMD3
 442   00000662 5588                    SUBQ.L   #02,A0               POINT TO TMD1
 443
 444   00000664 32BC8054                MOVE.W   #$8054,(A1)          SET UP INIT BLOCK TO INTERNAL LOOPBACK
 445   00000668 4EB9000006CC            JSR      CSRINIT              GO START UP THE LANCE
 446   0000066E 08AC00050024  CHECK3    BCLR.B   #05,RINGSTAT(A4)     SEE IF THIS PORTION OF THE TEST IS COMPLETE
 447   00000674 67F8                    BEQ      CHECK3               CHECK AGAIN
 448
 449                            ***   TURN OFF THE LANCE   ***
 450   00000676 247C00004002            MOVE.L   #RAP,A2              SELECT LANCE'S REGISTER ADDRESS PORT TO WRITE TO
 451   0000067C 34BC0000                MOVE.W   #CSR0,(A2)           LOAD REGISTER ADDRESS PORT OF LANCE WITH CSR0
 452   00000680 267C00004000            MOVE.L   #RDP,A3              SELECT LANCE'S REGISTER DATA PORT TO WRITE TO
 453   00000686 36BC00FF                MOVE.W   #$00FF,(A3)          TURN OFF THE LANCE
 454
 455                            ***   TEST EXTERNAL LOOPBACK   ***
 456
 457   0000068A 08AC00000024            BCLR.B   #00,RINGSTAT(A4)     CLEAR THE INTERNAL LOOP STATUS BIT
 458   00000690 00458300                ORI.W    #$8300,D5            SET OWNERSHIP BIT IN XMIT RING
 459   00000694 3085                    MOVE.W   D5,(A0)              MOVE TMD1 TO RING LOCATION
```

```
Line S Location  Value          Source
 460   00000696 5488                   ADDQ.L   #02,A0               GENERATE ADDRESS OF TMD2
 461   00000698 20BCFFE40000           MOVE.L   #$FFE40000,(A0)      MOVE BYTE COUNT(28 BYTES) TO TMD2 ON DESCRIPTOR
 462                           *                                     RING AND CLEAR OUT TMD3
 463   0000069E 32BC8004               MOVE.W   #$8004,(A1)          SET UP INIT BLOCK TO INTERNAL LOOPBACK
 464   000006A2 4EB9000006CC           JSR      CSRINIT              GO START UP THE LANCE
 465   000006A8 08AC00050024   CHECK4  BCLR.B   #05,RINGSTAT(A4)     SEE IF THIS PORTION OF THE TEST IS COMPLETE
 466   000006AE 67F8                   BEQ      CHECK4               CHECK AGAIN
 467
 468                           ***   TURN OFF THE LANCE   ***
 469   000006B0 247C00004002           MOVE.L   #RAP,A2              SELECT LANCE'S REGISTER ADDRESS PORT TO WRITE TO
 470   000006B6 34BC0000               MOVE.W   #CSR0,(A2)           LOAD REGISTER ADDRESS PORT OF LANCE WITH CSR0
 471   000006BA 267C00004000           MOVE.L   #RDP,A3              SELECT LANCE'S REGISTER DATA PORT TO WRITE TO
 472   000006C0 36BC00FF               MOVE.W   #$00FF,(A3)          TURN OFF THE LANCE
 473
 474   000006C4 08AC00040024           BCLR.B   #04,RINGSTAT(A4)     CLEAR DIAGNOSTIC BIT
 475   000006CA 4E75                   RTS
 476
 477
 478                           *******   END OF INITIALIZATION AND DIAGNOSTIC ROUTINE   ******
 479
 480                           ********************************************************
 481                           *                                                      *
 482                           *      INITIAL.DIAG.CSRINIT                            *
 483                           *      INITIALIZES THE CONTROL AND STATUS REGISTERS    *
 484                           *                                                      *
 485                           ********************************************************
 486
 487   000006CC 48E7FFFF       CSRINIT  MOVEM.L  A0-A7/D0-D7,-(A7)    SAVE OLD REGISTERS
 488   000006D0 207C00004002            MOVE.L   #RAP,A0              SELECT LANCE'S REGISTER ADDRESS PORT TO WRITE TO
 489   000006D6 30BC0001                MOVE.W   #CSR1,(A0)           LOAD REGISTER ADDRESS PORT OF LANCE WITH CSR1 ADD.
 490   000006DA 227C00004000            MOVE.L   #RDP,A1              SELECT LANCE'S REGISTER DATA PORT TO WRITE TO
 491   000006E0 223C00002000            MOVE.L   #IADR,D1             GET INITIALIZATION BLOCK BASE ADDRESS
 492   000006E6 3281                    MOVE.W   D1,(A1)              LOAD INITIALIZATION BLOCK STARTING ADDRESS IN CSR1
 493   000006E8 30BC0002                MOVE.W   #CSR2,(A0)           SELECT LANCE REGISTER ADDRESS PORT TO WRITE TO
 494   000006EC 4841                    SWAP     D1                   GET HIGH ORDER BYTE OF INITIALIZATION ADDRESS
 495   000006EE 3281                    MOVE.W   D1,(A1)              LOAD HIGH ORDER BYTE OF INIT. BLOCK INTO CSR2
 496   000006F0 30BC0003                MOVE.W   #CSR3,(A0)           LOAD REGISTER ADDRESS PORT OF LANCE WITH CSR3
 497   000006F4 32BC0006                MOVE.W   #$0006,(A1)          INITIALIZE LANCE TO INTERFACE TO MK68000 FORMAT
 498   000006F8 30BC0000                MOVE.W   #CSR0,(A0)           LOAD REGISTER ADDRESS PORT OF LANCE WITH CSR0
 499   000006FC 32BC0043                MOVE.W   #$0043,(A1)          INITIALIZES CSR0, LANCE IS NOW READY TO RUN
 500   00000700 4CDFFFFF                MOVEM.L  (A7)+,D0-D7/A0-A7    RETRIVE OLD REGISTERS
 501   00000704 4E75                    RTS                           RETURN FROM THIS SUBROUTINE
 502
 503                           ***   END OF CSRINIT SUBROUTINE   ***
 504
 505
 506                           ********************************************************
 507                           *                                                      *
 508                           *      INITIAL.DIAG.CRC                                *
 509                           *      CYCLE REDUNDENCY CHECK SOFTWARE GENERATION      *
 510                           *                                                      *
```

```
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Line S Location  Value          Source
 511                            *                                                    *
 512                            ******************************************************
 513
 514   00000706 48E7FFFF        CRCGEN   MOVEM.L  A0-A7/D0-D7,-(A7)     SAVE OLD REGISTERS
 515   0000070A 207C00003094             MOVE.L   #$3094,A0             GET ADDRESS OF CRC LOCATION
 516   00000710 20BCB1109280             MOVE.L   #$B1109280,(A0)       MOVE CRC FOR AAA...AAA OUT TO BUFFER
 517   00000716 4CDFFFFF                 MOVEM.L  (A7)+,D0-D7/A0-A7     RETRIVE OLD REGISTERS
 518   0000071A 4E75                     RTS                            RETURN FROM THIS SUBROUTINE
 519
 520                            ***   END OF CRCGEN SUBROUTINE   ***
 521
 522
 523   0000071C 004400040000    PROGIADR DC.W     MODE,PADR1,PADR2,PADR3,LADR1,LADR2,LADR3,LADR4,RDRA1,RDRA2,TDRA1,TDRA2
 524   00000734 0100            RBUFLEN  DC.W     BUFLEN
 525   00000736 0100            TBUFLEN  DC.W     BUFLEN
 526   00000738 0060            RBUFDISP DC.W     RBUFDIS
 527   0000073A 1020            TBUFDISP DC.W     TBUFDIS
 528
 529   0000073C 00000000                 END

no errors detected.

Options in effect:

  NOA,BRL,NOCEX,CL,FRL,MC,MD,NOMEX,O,NOPCO,NOPCS,LIST,NOSTR,FORMAT,NOMOTOROLA
```

UNITED TECHNOLOGIES MOSTEK 68000 Assembler V1.4
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INITIAL.A68

SYMBOL TABLE LISTING

NAME	ATTR	SECT	VALUE
BUFLEN			00000100
CALCDNE			000004CA
CALCDONE			0000049C
CHECK1			00000602
CHECK2			00000638
CHECK3			0000066E
CHECK4			000006A8
CLEAR			00000400
COUNT16			0000047C
COUNT20			000004B2
CRCGEN			00000706
CSR0	XDEF		00000000
CSR1	XDEF		00000001
CSR2	XDEF		00000002
CSR3	XDEF		00000003
CSRINIT			000006CC
DATINTR	XREF	*	00000000
DIAG	XDEF		0000059A
DLENGTH	XDEF		00000034
FIRSTRCV			000004FE
FIRSTXM			0000053E
GOINIT			00000590
IADR			00002000
INCREM			00000474
LADR1			00000008
LADR2			00000000
LADR3			00000000
LADR4			00000000
LANINTR	XREF	*	00000000
LASTRRNG	XDEF		00000014
LASTTRNG	XDEF		00000018
LOOPMCNT	XDEF		00000020
LOOPXADD	XDEF		00000028
MESS			000005C6
MLENGTH	XDEF		00000038
MODE			00000044
MORE	XDEF		0000002C
NEXTRRNG			000004F4
NEXTTRNG	XDEF		0000001C
NXPOWER			000004BE
NXTPOWER			00000490
NXTTRNG			00000534
ONE	XDEF		0000002E
PADR1			00000004
PADR2			00000000

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INITIAL.A68

SYMBOL TABLE LISTING

NAME	ATTR	SECT	VALUE
PADR3			00000000
PROGIADR			0000071C
RAP	XDEF		00004002
RBUFDIS			00000060
RBUFDISP			00000738
RBUFLEN			00000734
RDP	XDEF		00004000
RDRA1			00002018
RDRA2			00006000
RETURN			0000046A
RINGSTAT	XDEF		00000024
RINGSTK			000038C0
RLEN	XDEF		00000000
RRNGBASE	XDEF		00000004
RRNGBOT	XDEF		0000000C
STACK			0000387C
TBUFDIS			00001020
TBUFDISP			0000073A
TBUFLEN	XDEF		00000736
TDRA1			00002058
TDRA2			00004000
TLEN	XDEF		00000002
TRINGCNT	XDEF		00000022
TRNGBASE	XDEF		00000008
TRNGBOT	XDEF		00000010
WAIT			00000596

8.2 APPENDIX B, LANCE INTERRUPT ASSEMBLY CODE

The following pages provide a listing of the LANCE interrupt assembly code.

```
UNITED TECHNOLOGIES MOSTEK 68000 Assembler V1.4
Site 99994 MOSTEK
LEXCEPT.A68

Line S Location  Value          Source
   1 0
   2 0
   3 0
   4 0
   5 0                          ********************************************************************+
   6 0                          *+*******************************************************************+*
   7 0                          **                                                                   **
   8 0                          ** MODULE NAME: LEXCEPT                                             **
   9 0                          **                                                                   **
  10 0                          ** AUTHOR:  JIM FONTAINE                                            **
  11 0                          **                                                                   **
  12 0                          ** PROGRAM: LANCE                                                   **
  13 0                          **                                                                   **
  14 0                          ** LATEST REVISION DATE: JANUARY 20, 1984                           **
  15 0                          **                                                                   **
  16 0                          ***********************************************************************
  17 0                          **                                                                   **
  18 0                          ** DESCRIPTION:  THIS MODULE IS THE LANCE INTERRUPT HANDLING        **
  19 0                          ** ROUTINE.  IT WILL EXAMINE THE CONTROL AND STATUS REGISTER        **
  20 0                          ** OF THE LANCE AND DETERMINE WHAT CAUSED LANCE TO INTERRUPT        **
  21 0                          ** THE HOST PROCESSOR.  AFTER IT DETERMINED WHAT CAUSED THE        **
  22 0                          ** THE INTERRUPT CAUSING CONDITION IT WILL SERVICE THE CON-        **
  23 0                          ** DITION OR REPORT THE ERROR.                                      **
  24 0                          **                                                                   **
  25 0                          ***********************************************************************+
  26 0                          ********************************************************************+
  27 0
  28 0                          ************************************************
  29 0                          *                                              *
  30 0                          *               EQUATE TABLE                   *
  31 0                          *                                              *
  32 0                          ************************************************
  33 0
  34 0
  35 0
  36 0
  37 0          00003A20        OUTPUT   EQU      $3A20
  38 0
  39 0          00003B20        MESSAGE  EQU      $3B20
  40 0
  41 0          0000003C        TESTTMD1 EQU      $3C
  42 0
  43 0
  44 0
  45 0                                   XDEF     OUTPUT
  46 0                                   XDEF     MESSAGE
  47 0                                   XDEF     LANINTR
  48 0                                   XDEF     CRCERR
  49 0                                   XDEF     XRINGFIX
  50 0                                   XDEF     CLEANUP
  51 0                                   XDEF     PCKDONE
```

```
Line S Location  Value          Source
  52 0
  53 0                          *   KEYWORD VALUE REFERENCE   *
  54 0
  55 0                                XREF    RAP
  56 0                                XREF    RDP
  57 0
  58 0                                XREF    CSR0
  59 0                                XREF    CSR1
  60 0                                XREF    CSR2
  61 0                                XREF    CSR3
  62 0
  63 0                                XREF    RLEN
  64 0                                XREF    TLEN
  65 0                                XREF    RRNGBASE
  66 0                                XREF    TRNGBASE
  67 0                                XREF    RRNGBOT
  68 0                                XREF    TRNGBOT
  69 0                                XREF    LASTRRNG
  70 0                                XREF    LASTTRNG
  71 0                                XREF    NEXTTRNG
  72 0                                XREF    LOOPMCNT
  73 0                                XREF    TRINGCNT
  74 0                                XREF    RINGSTAT
  75 0                                XREF    MLENGTH
  76 0                                XREF    MORE
  77 0                                XREF    ONE
  78 0                                XREF    LOOPXADD
  79 0                                XREF    DLENGTH
  80 0
  81 0                          *     SUBROUTINE CALLS REFERENCE    *
  82 0
  83 0                                XREF    BABLSUB
  84 0                                XREF    CERRSUB
  85 0                                XREF    MISSSUB
  86 0                                XREF    MERRSUB
  87 0                                XREF    FRAMSUB
  88 0                                XREF    CRCSUB
  89 0                                XREF    OFLOSUB
  90 0                                XREF    BUFFSUB
  91 0                                XREF    RTRYSUB
  92 0                                XREF    STOP
  93 0                                XREF    LCARRSUB
  94 0                                XREF    COLLSUB
  95 0                                XREF    UFLOSUB
  96 0                                XREF    BUFRSUB
  97 0                                XREF    IDONSUB
  98 0
  99 0                                XREF    SIZEERR
 100 0                                XREF    XMITSERV
 101 0                                XREF    PACKERR
 102 0                                XREF    CRCBAD
```

```
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LEXCEPT.A68

Line S Location  Value          Source
 103 0                                  XREF     LPACKERR
 104 0                                  XREF     LMESSBAD
 105 0
 106 0
 107 0
 108            00000800                ORG      $800
 109
 110                            ********************************************************
 111                            *                                                      *
 112                            *   LANCE INTERRUPT ERROR CHECKING SUBMODULE           *
 113                            *   LEXCEPT.ERROR                                      *
 114                            *                                                      *
 115                            ********************************************************
 116
 117   00000800 397CCCCCFFFF    LANINTR  MOVE.W   #$CCCC,LOOPMCNT(A4)   TEST
 118   00000806 48E7FFFE                 MOVEM.L  D0-D7/A0-A6,-(A7)     SAVE REGS ON STACK
 119   0000080A 247CFFFFFFFF             MOVEA.L  #RAP,A2               SELECT LANCE'S RAP TO WRITE INTO
 120   00000810 34BCFFFF                 MOVE.W   #CSR0,(A2)            LOAD CSR0 ADDRESS IN REG ADD PORT
 121   00000814 267CFFFFFFFF             MOVEA.L  #RDP,A3               LOAD "REG DATA PORT" ADDRESS INTO REG A3
 122   0000081A 3413                     MOVE.W   (A3),D2               MOVE CONTENTS OF CSR0 INTO REG D2
 123   0000081C 3E02                     MOVE.W   D2,D7                 GET A WORKING COPY OF CSR0
 124   0000081E 0247FFBF                 ANDI.W   #$FFBF,D7             MASK OUT INTERRUPT ENABLE BIT
 125   00000822 3687                     MOVE.W   D7,(A3)               DISABLE "INTR. ENABLE" BIT & CLEAR OUR THE REST
 126
 127                            **      DETERMINE WHAT CAUSED THE INTERRUPT   *
 128
 129   00000824 0802000F                 BTST     #$0F,D2               CHECK IF "ERROR" BIT IS SET IN CSR0
 130   00000828 672E                     BEQ.S    XMITCK                IF IT ISN'T, BRANCH TO XMIT INTR. CHECK
 131
 132   0000082A 0802000E        ERROR    BTST     #$0E,D2               CHECK IF IT IS A BABBLE ERROR
 133   0000082E 6706                     BEQ.S    CERR                  IF NOT, CHECK IF IT IS A COLLISION ERROR
 134   00000830 4EB9FFFFFFFF             JSR      BABLSUB               IF IT IS, JUMP TO BABBLE HANDLE ROUTINE
 135   00000836 0802000D        CERR     BTST     #$0D,D2               CHECK IF IT IS A COLLISION ERROR
 136   0000083A 6706                     BEQ.S    MISS                  IF NOT, CHECK IT IT IS A MISSED PACKET ERROR
 137   0000083C 4EB9FFFFFFFF             JSR      CERRSUB               IF IT IS, JUMP TO COLLISION HANDLE SUBR.
 138   00000842 0802000C        MISS     BTST     #$0C,D2               CHECK IF IT IS A MISSED PACKET ERROR
 139   00000846 4EB9FFFFFFFF             JSR      MISSSUB               IF IT IS, JUMP TO MISSED PACKET SUBR.
 140   0000084C 0802000B        MERR     BTST     #$0B,D2               CHECK IF IT IS A MEMORY ERROR
 141   00000850 6706                     BEQ.S    XMITCK                IF NOT, CHECK FOR XMIT INTR BIT SET
 142   00000852 4EB9FFFFFFFF             JSR      MERRSUB               IF IT IS, JUMP TO MEMORY ERROR SUBR.
 143
 144
 145                            ************************************************
 146                            *                                              *
 147                            *     TRANSMIT INTERRUPT HANDLING ROUTINE      *
 148                            *     LEXCEPT.XMIT                             *
 149                            *                                              *
 150                            ************************************************
 151
 152   00000858 08020009        XMITCK   BTST     #$09,D2               CHECK FOR "TRANSMIT INTR" BIT SET
 153   0000085C 670000BE                 BEQ      RVCRINT               IF IT ISN'T SEE IF RECEIVE INTERRUPT IS SET
```

```
Line S Location  Value          Source
 154
 155   00000860 206CFFFF               MOVE.L   LASTTRNG(A4),A0      LOAD UP NEXT XMIT RING ADDRESS
 156   00000864 2248                   MOVE.L   A0,A1                GET A WORKING COPY OF THE RING ADDRESS
 157   00000866 5488                   ADD.L    #$02,A0              GENERATE ADDRESS OF TMD1 (RING STATUS)
 158   00000868 3010                   MOVE.W   (A0),D0              GET STATUS (TMD1) AND PUT IT IN REG D0
 159   0000086A 0800000C               BTST     #$0C,D0              CHECK FOR "MORE" BIT SET
 160   0000086E 6704                   BEQ.S    ONETEST              IF NOT, GO CHECK "ONE" BIT
 161   00000870 526CFFFF               ADD.W    #$01,MORE(A4)        IF SO, UPDATE "MORES" COUNTER
 162   00000874 0800000B       ONETEST BTST     #$0B,D0              CHECK FOR "ONE" BIT SET
 163   00000878 6704                   BEQ.S    ERRORTST             IF NOT, GO CHECK "ERROR" BIT
 164   0000087A 526CFFFF               ADD.W    #$01,ONE(A4)         IF SO, UPDATA "ONE" COUNTER
 165
 166                           ******   TRANSMISSION ERROR DETERMINATION     *****
 167
 168   0000087E 0800000E       ERRORTST BTST    #$0E,D0              CHECK FOR "ERROR" BIT SET
 169   00000882 6764                   BEQ.S    LOOPTEST             IF NOT, CONTINUE WITH TRANSMIT ROUTINE
 170   00000884 5888                   ADD.L    #$04,A0              GENERATE ERROR STATUS ADDRESS
 171   00000886 3010                   MOVE.W   (A0),D0              GET ERROR STATUS AND PUT IT IN REG D0
 172   00000888 0800000A               BTST     #$0A,D0              CHECK FOR "RETRY" ERROR BIT SET
 173   0000088C 6712                   BEQ.S    LCARERR              IF NOT, CHECK FOR LOSS OF CARRIER
 174   0000088E 4EB9FFFFFFFF           JSR      STOP                 IF SO, STOP LANCE AND TAKE CARE OF ERROR
 175   00000894 3200                   MOVE.W   D0,D1                MOVE TIME DOMAIN REFLECTOMETRY VALUE
 176   00000896 024103FF               ANDI.W   #$03FF,D1            MASK OFF STATUS BITS
 177   0000089A 4EB9FFFFFFFF           JSR      RTRYSUB              JUMP TO RETRY ERROR SUBROUTINE
 178   000008A0 0800000B       LCARERR BTST     #$0B,D0              CHECK FOR "LOSS OF CARRIER" BIT SET
 179   000008A4 670C                   BEQ.S    LATECOLL             IF NOT, CHECK FOR LATE COLLISION
 180   000008A6 4EB9FFFFFFFF           JSR      STOP                 IF SO, STOP AND TAKE CARE OF IT
 181   000008AC 4EB9FFFFFFFF           JSR      LCARRSUB             JUMP TO "LOSS OF CARRIER" SUBROUTINE
 182   000008B2 0800000C       LATECOLL BTST    #$0C,D0              CHECK FOR "LATE COLLISION" BIT SET
 183   000008B6 670C                   BEQ.S    UFLOERR              IF NOT, CHECK FOR UNDER FLOW
 184   000008B8 4EB9FFFFFFFF           JSR      STOP                 IF SO, STOP AND TAKE CARE OF ERROR
 185   000008BE 4EB9FFFFFFFF           JSR      COLLSUB              JUMP TO "LATE COLLISION" SUBROUTINE
 186   000008C4 0800000E       UFLOERR BTST     #$0E,D0              CHECK FOR "UNDERFLOW" BIT SET
 187   000008C8 670C                   BEQ.S    NOBUFF               IF NOT, CHECK FOR BUFFER ERROR
 188   000008CA 4EB9FFFFFFFF           JSR      STOP                 IF SO, STOP AND TAKE CARE OF IT
 189   000008D0 4EB9FFFFFFFF           JSR      UFLOSUB              JUMP TO "UNDERFLOW" SUBROUTINE
 190   000008D6 0800000F       NOBUFF  BTST     #$0F,D0              CHECK FOR "BUFFER ERROR" BIT SET
 191   000008DA 670C                   BEQ.S    LOOPTEST             IF NOT, CONTINUE WITH LOOPTEST
 192   000008DC 4EB9FFFFFFFF           JSR      STOP                 IF SO, STOP AND TAKE CARE OF ERROR
 193   000008E2 4EB9FFFFFFFF           JSR      BUFRSUB              JUMP TO "BUFFER ERROR" SUBROUTINE
 194
 195                           *******   LOOPBACK TESTING   ********
 196
 197   000008E8 082C0001FFFF   LOOPTEST BTST.B   #1,RINGSTAT(A4)      SEE IF WE ARE IN THE LOOP BACK MODE
 198   000008EE 6712                   BEQ.S    FINISH               IF NOT, FINISH UP WITH THE XMIT ROUTINE
 199   000008F0 2611                   MOVE.L   (A1),D3              IF IN LOOPBACK, GET XMIT BUFFER ADDRESS
 200   000008F2 E15B                   ROL.W    #8,D3                POSITION THE UPPER BYTE OF LOWER WORD FOR CLEAR
 201   000008F4 163C0000               MOVE.B   #00,D3               CLEAR OUT STATUS PART OF RMD1
 202   000008F8 E05B                   ROR.W    #8,D3                REPOSITION BYTES
 203   000008FA 4843                   SWAP     D3                   REFORMAT THE LONG WORD ADD FOR 68000 COMPATABIOLITY
 204   000008FC 2943FFFF               MOVE.L   D3,LOOPXADD(A4)      SAVE A COPY ON THE STACK FOR LATER
```

```
Line S Location  Value          Source
 205   00000900 601A                   BRA.S    RVCRINT              GO CHECK IF RECEIVE INTER. BIT IS SET
 206
 207                            ***   TRANSMIT RING RESTORATION    ***
 208
 209   00000902 066C0001FFFF   FINISH   ADDI.W   #$01,TRINGCNT(A4)     INCREMENT THE NUMBER OF AVAILABLE XMIT RINGS
 210   00000908 B3ECFFFF               CMPA.L   TRNGBOT(A4),A1         SEE IF WE ARE ABOUT TO WRAP AROUND
 211   0000090C 660A                   BNE.S    INCRE                IF NOT, INCREMENT THE RING POINTER
 212   0000090E 296CFFFFFFFF           MOVE.L   TRNGBASE(A4),LASTTRNG(A4) MOVE THE RING BASE ADD ONTO LASTTRNG STACK SPOT
 213   00000914 60000192               BRA      IDONCHK             BRANCH TO CONT
 214   00000918 50ACFFFF       INCRE   ADD.L    #$08,LASTTRNG(A4)    UPDATE LAST RING ADDRESS
 215
 216                            **   END OF TRANSMIT INTERRUPT ROUTINE   *
 217
 218
 219                            ******************************************
 220                            *                                        *
 221                            *    RECEIVE INTERRUPT HANDLING ROUTINE  *
 222                            *    LEXCEPT.RVCR                        *
 223                            *                                        *
 224                            ******************************************
 225
 226   0000091C 0802000A       RVCRINT  BTST     #$0A,D2              CHECK FOR "RECEIVE INTR" BIT SET
 227   00000920 67000186               BEQ      IDONCHK              IF IT ISN'T, SEE IF INITIALIZATION DONE IS SET
 228
 229   00000924 206CFFFF       RVCRBUF  MOVE.L   LASTRRNG(A4),A0      GET DESCRIPTOR RING STARTING ADDR. (RMD0)
 230   00000928 2A48                    MOVE.L   A0,A5                MAKE A WORKING COPY OF IT IN REG A5
 231   0000092A 5C8D                    ADDQ.L   #$06,A5              GENERATE ADDRESS OF RDM3
 232   0000092C 3215                    MOVE.W   (A5),D1              GET MESSAGE BYTE COUNT (MCNT)
 233   0000092E 9BFC00000004            SUBA.L   #04,A5               GENERATE ADDRESS RMD1
 234
 235                            ***   ERROR CHECKING   ***
 236
 237   00000934 3015                    MOVE.W   (A5),D0              GET RECEIVED MESSAGE STATUS (RDM1)
 238   00000936 0800000E                BTST     #$0E,D0              SEE IF "ERROR" BIT IS SET
 239   0000093A 66000110                BNE      RECVERR              IF IS, FIND OUT WHAT CAUSED THE ERROR
 240
 241
 242                            ***   CHECK TO SEE IF WE ARE IN LOOPBACK MODE   ***
 243
 244   0000093E 082C0001FFFF            BTST.B   #1,RINGSTAT(A4)      CHECK TO SEE IF WE ARE IN LOOPBACK MODE
 245   00000944 670000B0                BEQ      NOLOOP               IF WE ARE NOT IN LOOPBACK MODE CONTINUE
 246
 247                            ***   LOOPBACK MESSAGE SIZE CHECK   ***
 248
 249   00000948 B26CFFFF                CMP.W    MLENGTH(A4),D1       SEE IF RVCR MESSAGE IS EQUAL TO XMIT MESSAGE
 250   0000094C 67000008                BEQ      PACKCHK              IF SO CONTINUE
 251   00000950 4EB9FFFFFFFF            JSR      SIZEERR              IF NOT, SERVICE ERROR ROUTINE
 252
 253                            ***   LOOPBACK PACKET CHECK   ***
 254
 255   00000956 08000009       PACKCHK  BTST     #09,D0               CHECK IF START OF PACKET BIT IS SET IN RMD1
```

```
Line S Location  Value          Source
 256   0000095A 6606                   BNE.S    BITTST              IF IT IS, GO CHECK THE END OF PACKET BIT
 257   0000095C 4EB9FFFFFFFF           JSR      LPACKERR            IF IT IS NOT JUMP TO PACKET ERROR SUBR.
 258   00000962 08000008       BITTST  BTST     #08,D0              CHECK IF END OF PACKET BIT IS SET
 259   00000966 6606                   BNE.S    BADDGEN             IF IT IS, GO GENERATE BUFFER ADDRESS
 260   00000968 4EB9FFFFFFFF           JSR      LPACKERR            IF IT IS NOT, JUMP TO PACKET ERROR
 261
 262                           ***   GET RVCR BUFFER STARTING ADDRESS   ***
 263
 264   0000096E 2610           BADDGEN MOVE.L   (A0),D3             MOVE RVCR BUFFER ADDRESS INTO REG D3
 265   00000970 E15B                   ROL.W    #08,D3              MOVE SECOND BYTE INTO POSITION TO BE CLEARED
 266   00000972 163C0000               MOVE.B   #$00,D3             CLEAR OUT THE STATUS
 267   00000976 E05B                   ROR.W    #$08,D3             REPOSITION BYTES
 268   00000978 4843                   SWAP     D3                  REFORMAT FOR 68000 COMPATIBILITY
 269   0000097A 3643                   MOVE     D3,A3               MOVE ADDRESS INTO AN ADDRESS REGISTER
 270
 271                           ***   LOOPBACK XMIT-RVCR WORD COMPARISON   ***
 272
 273   0000097C 322CFFFF               MOVE.W   DLENGTH(A4),D1      GET MESSAGE DATA LENGTH
 274   00000980 721C                   MOVE.L   #$01C,D1            LOAD D1 WITH 28 (28 BYTES IS THE DATA SIZE)
 275   00000982 226CFFFF               MOVE.L   LOOPXADD(A4),A1     GET LOOPBACK XMIT BUFFER STARTING ADDRESS
 276   00000986 3A13           MOREWDS MOVE.W   (A3),D5             GET ONE WORD OF RVCR BUFFER MESSAGE
 277   00000988 3C11                   MOVE.W   (A1),D6             GET ONE WORD OF XMIT BUFFER MESSAGE
 278   0000098A BC45                   CMP.W    D5,D6               SEE IF THE TWO WORDS ARE IDENTICAL
 279   0000098C 6706                   BEQ.S    INCR                IF THEY ARE EQUAL, INCREMENT THE ADDRESS
 280   0000098E 4EB9FFFFFFFF           JSR      LMESSBAD            IF THEY ARE NOT EQUAL, JUMP TO ERROR MESSAGE
 281   00000994 548B           INCR    ADDQ.L   #$2,A3              OTHERWISE, INCREMENT ADDRESS
 282   00000996 5489                   ADDQ.L   #$2,A1              INCREMENT THE ADDRESS
 283   00000998 04410002               SUBI.W   #$02,D1             DECREMENT MESSAGE COUNT
 284   0000099C 6F02                   BLE.S    CRCCK               IF NO MORE WORDS, CHECK THE CRC
 285   0000099E 60E6                   BRA.S    MOREWDS             GO GET SOME MORE WORDS TO COMPARE
 286
 287                           ***   SOFTWARE CRC TEST   ***
 288
 289   000009A0 082C0004FFFF   CRCCK   BTST.B   #04,RINGSTAT(A4)     SEE IF WE ARE IN LANCE DIAGONOSTICS
 290   000009A6 6700001E               BEQ      XRINGFIX            IF NOT, GO FIX UP RINGS
 291
 292   000009AA 7204                   MOVE.L   #$004,D1            LOAD D1 WITH 4 (4 BYTES IS THE CRC SIZE)
 293   000009AC 3A13           MORECRC MOVE.W   (A3),D5             GET ONE WORD OF RVCR BUFFER MESSAGE
 294   000009AE 3C11                   MOVE.W   (A1),D6             GET ONE WORD OF XMIT BUFFER MESSAGE
 295   000009B0 BC45                   CMP.W    D5,D6               SEE IF THE TWO WORDS ARE IDENTICAL
 296   000009B2 6706                   BEQ.S    DECR                IF THEY ARE EQUAL, GO DECREMENT THE COUNT
 297   000009B4 4EB9FFFFFFFF           JSR      CRCBAD              IF THEY ARE NOT EQUAL, JUMP TO ERROR MESSAGE
 298   000009BA 04410002       DECR    SUBI.W   #02,D1              DECREMENT MESSAGE COUNT
 299   000009BE 6F06                   BLE.S    XRINGFIX            IF NO MORE WORDS, FIX UP THE XMIT RING
 300   000009C0 548B                   ADDQ.L   #2,A3               OTHERWISE, INCREMENT ADDRESS
 301   000009C2 5489                   ADDQ.L   #2,A1               INCREMENT THE ADDRESS
 302   000009C4 60E6                   BRA.S    MORECRC             GO GET SOME MORE WORDS TO COMPARE
 303
 304                           ***   XMIT RING RESTORATION   ***
 305
 306   000009C6 082C0004FFFF   XRINGFIX BTST.B   #04,RINGSTAT(A4)     SEE IF WE ARE IN LANCE DIAGONOSTICS
```

```
Line S Location  Value          Source
 307   000009CC 660000CC               BNE      OWNSHIP              IF SO, LEAVE RINGS AS IS AND GIVE BACK OWNERSHIP
 308
 309   000009D0 066C0001FFFF   RINGFIX ADDI.W   #$01,TRINGCNT(A4)     INCREMENT THE NUMBER A AVAILABLE XMIT RINGS
 310   000009D6 206CFFFF               MOVE.L   LASTTRNG(A4),A0      GET LAST XMIT RING ADDRESS
 311   000009DA B1ECFFFF               CMPA.L   TRNGBOT(A4),A0       SEE IF WE ARE DOWN TO THE BOTTOM OF THE RINGS
 312   000009DE 6A0C                   BPL.S    RINGGEN              IF WE ARE, GO GENERATE NEW LAST RING
 313   000009E0 06AC00000008           ADDI.L   #$08,LASTTRNG(A4)    OTHERWISE, GENERATE NEW LAST RING VALUE, AND PUT ON STACK
               FFFF
 314   000009E8 60000096               BRA      CLEANUP              GO CLEAN UP RINGS
 315   000009EC 296CFFFFFFFF   RINGGEN MOVE.L   TRNGBASE(A4),LASTTRNG(A4) MAKE RING BASE THE NEW LAST RING ADDRESS
 316   000009F2 6000008C               BRA      CLEANUP              GO CLEAN UP RINGS
 317
 318
 319
 320                           ********  "NON LOOPBACK" OPERATION **********
 321
 322                           **      PACKET DISCREPANCY CHECK   *
 323
 324   000009F6 08000009       NOLOOP   BTST     #09,D0               IS THE START OF PACKET BIT SET IN RMD1?
 325   000009FA 6718                    BEQ.S    SETB4                IF NOT, SEE IF IT WAS SET PREVIOUSLY
 326   000009FC 08AC0002FFFF            BCLR.B   #02,RINGSTAT(A4)     IF SO, SEE IF IT WAS SET PREVIOUSLY
 327
 328   00000A02 6600FFFF                BNE      PACKERR              IF IT WAS SET BEFORE YOU HAVE AN ERROR
 329   00000A06 08000008                BTST     #08,D0               IF NOT SET, CHECK IF END OF PACKET BIT IS SET
 330   00000A0A 661E                    BNE.S    PCKDONE              IF IT IS, WE HAVE THE WHOLE MESSAGE,CHECK DONE
 331   00000A0C 002C0004FFFF            ORI.B    #$04,RINGSTAT(A4)    IF NOT, THIS IS ONLY THE START OF PACKET
 332   00000A12 6016                    BRA.S    PCKDONE              GO ON, PACKET CHECKS OUT
 333   00000A14 08AC0002FFFF   SETB4    BCLR.B   #2,RINGSTAT(A4)      SEE IF START OF PACKET WAS SET PREVIOUSLY
 334   00000A1A 6700FFFF                BEQ      PACKERR              IF IT WAS NOT SET BEFORE YOU HAVE AN ERROR
 335   00000A1E 08000008                BTST     #08,D0               IF IT WAS SET, SEE IF END OF PACKET IS SET
 336   00000A22 6706                    BEQ.S    PCKDONE              IF ENP SET, WE HAVE WHOLE MESSAGE, CHECK DONE
 337   00000A24 002C0004FFFF            ORI.B    #$04,RINGSTAT(A4)    IF NOT, THIS IS ONLY THE START OF MESSAGE
 338
 339                           **      CONTINUE WITH NORMAL PROCESS   *
 340
 341   00000A2A 2610           PCKDONE  MOVE.L   (A0),D3              MOVE RVCR BUFFER ADDRESS INTO REG D3
 342   00000A2C E15B                    ROL.W    #08,D3               MOVE SECOND BYTE INTO POSITION TO BE CLEARED
 343   00000A2E 163C0000                MOVE.B   #$00,D3              CLEAR OUT THE STATUS
 344   00000A32 E05B                    ROR.W    #$08,D3              REPOSITION BYTES
 345   00000A34 4843                    SWAP     D3                   REFORMAT FOR 68000 COMPATIBILITY
 346   00000A36 2643                    MOVE.L   D3,A3                MOVE ADDRESS INTO AN ADDRESS REGISTER
 347
 348                           **      MOVE RECEIVED MESSAGE FROM RECEIVE BUFFER INTO OUTPUT DEVICE   *
 349
 350   00000A38 227C00003A20            MOVE.L   #OUTPUT,A1           MOVE OUTPUT ADDRESS INTO REG A1
 351   00000A3E 3293           SOMEMORE MOVE.W   (A3),(A1)            MOVE MESSAGE WORD TO OUTPUT
 352   00000A40 548B                    ADD.L    #$2,A3               INCREMENT THE MESSAGE BUFFER ADDRESS
 353   00000A42 5489                    ADD.L    #$2,A1               INCREMENT THE MESSAGE OUTPUT ADDRESS
 354   00000A44 04410002                SUBI.W   #02,D1               DECREMENT THE MESSAGE LENGTH REGISTER
 355   00000A48 6EF4                    BGT.S    SOMEMORE             IF THERE ARE SOME MORE WORDS TO XFER, DO IT
 356   00000A4A 6034                    BRA.S    CLEANUP              FINISHED, GO CLEANUP RINGS
```

```
Line S Location  Value          Source
 357
 358                           ********  RECEIVE MESSAGE ERROR DETERMINATION  *******
 359
 360   00000A4C 4EB9FFFFFFFF   RECVERR   JSR      STOP                 STOP AND FIND OUT WHAT THE ERROR IS
 361   00000A52 0800000D                 BTST     #$0D,D0              CHECK IF "FRAME ERROR" BIT IS SET
 362   00000A56 6712                     BEQ.S    OFLOERR              IF NOT, CHECK IF OVER FLOW ERROR SET
 363   00000A58 4EB9FFFFFFFF             JSR      FRAMSUB              IF SO, JUMP TO FRAM ERROR SUBROUTINE
 364   00000A5E 0800000B       CRCERR    BTST     #$0B,D0              CHECK IF "CRC ERROR" BIT IS SET
 365   00000A62 6706                     BEQ.S    OFLOERR              IF NOT, CHECK OVERFLOW ERROR
 366   00000A64 4EB9FFFFFFFF             JSR      CRCSUB               IF SO JUMP TO CRC ERROR SUBROUTINE
 367   00000A6A 0800000C       OFLOERR   BTST     #$0C,D0              CHECK IF "OVER FLOW ERROR" BIT IS SET
 368   00000A6E 6706                     BEQ.S    BUFF                 IF NOT, CHECK BUFFER ERROR
 369   00000A70 4EB9FFFFFFFF             JSR      OFLOSUB              IF SO JUMP TO OVER FLOW SUBROUTINE
 370   00000A76 0800000A       BUFF      BTST     #$0A,D0              CHECK IF "BUFFER ERROR" BIT IS SET
 371   00000A7A 4EB9FFFFFFFF             JSR      BUFFSUB              IF SO, JUMP TO BUFFER ERROR SUBROUTINE
 372
 373                           ******    CLEANUP     ******
 374
 375   00000A80 226CFFFF       CLEANUP   MOVE.L   LASTRRNG(A4),A1      GO GET LAST RECEIVE RING ADDRESS
 376   00000A84 B3ECFFFF                 CMPA.L   RRNGBOT(A4),A1       SEE IF WE ARE DOWN TO THE BOTTOM OF THE RINGS
 377   00000A88 6A0A                     BPL.S    RINGLAST             IF WE ARE, GO GENERATE NEW LAST RING
 378   00000A8A 06AC00000008             ADDI.L   #$08,LASTRRNG(A4)    GENERATE NEW LAST RING VALUE & PUT ON STACK
                FFFF
 379   00000A92 6006                     BRA.S    OWNSHIP              GO GIVE OWNERSHIP BACK TO LANCE
 380   00000A94 296CFFFFFFFF   RINGLAST  MOVE.L   RRNGBASE(A4),LASTRRNG(A4) MAKE RING BASE THE NEW LAST RING ADDRESS
 381   00000A9A 1ABC0080       OWNSHIP   MOVE.B   #$80,(A5)            GIVE OWNERSHIP BACK TO LANCE
 382
 383   00000A9E 082C0002FFFF             BTST.B   #02,RINGSTAT(A4)     SEE IF START OF PACKET BIT IS SET
 384   00000AA4 6600FE7E                 BNE      RVCRBUF              IF SO, THERE IS MORE THAT ONE BUFFER
 385
 386
 387                           **      END OF RVCR INTERRUPT ROUTINE *
 388
 389                           ******************************************
 390                           *                                        *
 391                           *    LANCE INITIALIZATION DONE INTERRUPT *
 392                           *    LEXCEPT.IDON                        *
 393                           *                                        *
 394                           ******************************************
 395
 396   00000AA8 08020008       IDONCHK   BTST     #$08,D2              CHECK FOR "INITIALIZATION DONE" BIT SET
 397   00000AAC 6716                     BEQ.S    RESTORE              IF NOT SET, RESTORE AND FINISH UP
 398   00000AAE 4EB9FFFFFFFF             JSR      IDONSUB              IF IT IS, JUMP TO INITIALIZATION DONE SUBR.
 399
 400   00000AB4 082C0004FFFF             BTST.B   #04,RINGSTAT(A4)     SEE IF WE ARE IN LANCE DIAGONOSTICS
 401   00000ABA 67000008                 BEQ      RESTORE              IF NOT CONTIUNE NORMALLY
 402   00000ABE 08EC0005FFFF             BSET.B   #5,RINGSTAT(A4)      IF SO, SET "TEST FINISHED" BIT
 403                           *
 404   00000AC4 367CFFFF       RESTORE   MOVE.W   #RDP,A3              MOVE ADDRESS OF REGISTER DATA PORT TO A3
 405   00000AC8 36BC0040                 MOVE.W   #$0040,(A3)          SET THE INTERRUPT ENABLE BIT IN CSR0
 406                           *
```

```
UNITED TECHNOLOGIES MOSTEK 68000 Assembler V1.4
Site 99994 MOSTEK
LEXCEPT.A68

Line S Location  Value          Source
 407   00000ACC 4CDF7FFF               MOVEM.L  (A7)+,A0-A6/D0-D7     RETRIEVE OLD REGISTERS
 408   00000AD0 4E73                   RTE                            RETURN FROM EXCEPTION HANDLING
 409   00000AD2 00000000               END

no errors detected.


Options in effect:

  NOA,BRL,NOCEX,CL,FRL,MC,MD,NOMEX,O,NOPCO,NOPCS,LIST,NOSTR,FORMAT,NOMOTOROLA
```

SYMBOL TABLE LISTING

NAME	ATTR	SECT	VALUE
BABLSUB	XREF	*	00000000
BADDGEN			0000096E
BITTST			00000962
BUFF			00000A76
BUFFSUB	XREF	*	00000000
BUFRSUB	XREF	*	00000000
CERR			00000836
CERRSUB	XREF	*	00000000
CLEANUP	XDEF		00000A80
COLLSUB	XREF	*	00000000
CRCBAD	XREF	*	00000000
CRCCK			000009A0
CRCERR	XDEF		00000A5E
CRCSUB	XREF	*	00000000
CSR0	XREF	*	00000000
CSR1	XREF	*	00000000
CSR2	XREF	*	00000000
CSR3	XREF	*	00000000
DECR			000009BA
DLENGTH	XREF	*	00000000
ERROR			0000082A
ERRORTST			0000087E
FINISH			00000902
FRAMSUB	XREF	*	00000000
IDONCHK			00000AA8
IDONSUB	XREF	*	00000000
INCR			00000994
INCRE			00000918
LANINTR	XDEF		00000800
LASTRRNG	XREF	*	00000000
LASTTRNG	XREF	*	00000000
LATECOLL			000008B2
LCARERR			000008A0
LCARRSUB	XREF	*	00000000
LMESSBAD	XREF	*	00000000
LOOPMCNT	XREF	*	00000000
LOOPTEST			000008E8
LOOPXADD	XREF	*	00000000
LPACKERR	XREF	*	00000000
MERR			0000084C
MERRSUB	XREF	*	00000000
MESSAGE	XDEF		00003B20
MISS			00000842
MISSSUB	XREF	*	00000000
MLENGTH	XREF	*	00000000

UNITED TECHNOLOGIES MOSTEK 68000 Assembler V1.4
Site 99994 MOSTEK
LEXCEPT.A68

SYMBOL TABLE LISTING

NAME	ATTR	SECT	VALUE
MORE	XREF	*	00000000
MORECRC			000009AC
MOREWDS			00000986
NEXTTRNG	XREF	*	00000000
NOBUFF			000008D6
NOLOOP			000009F6
OFLOERR			00000A6A
OFLOSUB	XREF	*	00000000
ONE	XREF	*	00000000
ONETEST			00000874
OUTPUT	XDEF		00003A20
OWNSHIP			00000A9A
PACKCHK			00000956
PACKERR	XREF	*	00000000
PCKDONE	XDEF		00000A2A
RAP	XREF	*	00000000
RDP	XREF	*	00000000
RECVERR			00000A4C
RESTORE			00000AC4
RINGFIX			000009D0
RINGGEN			000009EC
RINGLAST			00000A94
RINGSTAT	XREF	*	00000000
RLEN	XREF	*	00000000
RRNGBASE	XREF	*	00000000
RRNGBOT	XREF	*	00000000
RTRYSUB	XREF	*	00000000
RVCRBUF			00000924
RVCRINT			0000091C
SETB4			00000A14
SIZEERR	XREF	*	00000000
SOMEMORE			00000A3E
STOP	XREF	*	00000000
TESTTMD1			0000003C
TLEN	XREF	*	00000000
TRINGCNT	XREF	*	00000000
TRNGBASE	XREF	*	00000000
TRNGBOT	XREF	*	00000000
UFLOERR			000008C4
UFLOSUB	XREF	*	00000000
XMITCK			00000858
XMITSERV	XREF	*	00000000
XRINGFIX	XDEF		000009C6

8.3 APPENDIX C, MESSAGE INTERRUPT ASSEMBLY CODE

The following pages provide a listing of the message interrupt assembly code.

UNITED TECHNOLOGIES MOSTEK 68000 Assembler V1.4
Site 99994 MOSTEK
MESSAGE.A68

```
Line S Location  Value          Source
   1 0                          ************************************************************+
   2 0                          *+***********************************************************+*
   3 0                          **                                                           **
   4 0                          ** MODULE NAME: MESSAGE                                     **
   5 0                          **                                                           **
   6 0                          ** AUTHOR:  JIM FONTAINE                                    **
   7 0                          **                                                           **
   8 0                          ** PROGRAM: LANCE                                          **
   9 0                          **                                                           **
  10 0                          ** LATEST REVISION DATE: JANUARY 20, 1958                   **
  11 0                          **                                                           **
  12 0                          ***************************************************************
  13 0                          ** DESCRIPTION:  THIS MODULE GENERATES A PSEUDO             **
  14 0                          ** MESSAGE THAT IS THEN PUT INTO THE TRANSMIT BUFFER.       **
  15 0                          ** THE MESSAGE CODE AND LENGTH IS DETERMINED BY THE         **
  16 0                          ** DLENGTH FOUND IN MEMORY LOCATION DLENGTH(A4)             **
  17 0                          ** THE BUFFER IS FILLED WITH CONSECUTIVE COUNTS,            **
  18 0                          ** NUMBERING FROM $0000 TO $(DLENGTH - 1). DLENGTH          **
  19 0                          ** MUST BE GREATER THAT 63 FOR NORNAL DATA TRANS-           **
  20 0                          ** MISSION AND LESS THAN 33 FOR LOOPBACK TRANS-             **
  21 0                          ** MISSION.                                                 **
  22 0                          ************************************************************+*
  23 0                          ************************************************************+
  24 0
  25 0
  26 0                          ************************************************
  27 0                          *                                              *
  28 0                          *              EQUATE TABLE                    *
  29 0                          *                                              *
  30 0                          ************************************************
  31 0
  32 0
  33 0
  34 0                          *   DESCRIPTOR RING STACK ALLOCATION   *
  35 0
  36 0
  37 0                          *   KEYWORD VALUE DEFINITION   *
  38 0
  39 0
  40 0                                XREF     RLEN
  41 0                                XREF     TLEN
  42 0                                XREF     TRNGBASE
  43 0                                XREF     TRNGBOT
  44 0                                XREF     LASTTRNG
  45 0                                XREF     NEXTTRNG
  46 0                                XREF     LOOPMCNT
  47 0                                XREF     TRINGCNT
  48 0                                XREF     RINGSTAT
  49 0                                XREF     LOOPXADD
  50 0                                XREF     MLENGTH
  51 0                                XREF     MESSAGE
```

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MESSAGE.A68

SYMBOL TABLE LISTING

NAME	ATTR	SECT	VALUE
BOTHBITS			00000B74
DATINTR	XDEF		00000B00
DLENGTH	XREF	*	00000000
ENDBIT			00000B6E
ENDPAC			00000B66
LASTTRNG	XREF	*	00000000
LOOPMCNT	XREF	*	00000000
LOOPXADD	XREF	*	00000000
MEMORY			00003FF0
MESSAGE	XREF	*	00000000
MLENGTH	XREF	*	00000000
MOREDATA			00000B48
NEXTRNG			00000B12
NEXTTRNG	XREF	*	00000000
NORINGS	XREF	*	00000000
NOUP			00000B3C
OUTPUT	XREF	*	00000000
RINGSTAT	XREF	*	00000000
RLEN	XREF	*	00000000
STARTPAC			00000B7A
STOP	XREF	*	00000000
TBUFLEN	XREF	*	00000000
TLEN	XREF	*	00000000
TMDFIX			00000B8C
TRINGCNT	XREF	*	00000000
TRNGBASE	XREF	*	00000000
TRNGBOT	XREF	*	00000000
UPDATE			00000B34
XMITDONE	XDEF		00000BB8

```
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Site 99994 MOSTEK
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Line S Location  Value          Source
  52 0                                XREF     OUTPUT
  53 0                                XREF     DLENGTH
  54 0                                XREF     TBUFLEN
  55 0
  56 0                          *     SUBROUTINE CALLS REFERENCE    *
  57 0
  58 0                                XREF     STOP
  59 0                                XREF     NORINGS
  60 0
  61 0                                XDEF     XMITDONE
  62 0                                XDEF     DATINTR
  63 0
  64 0          00003FF0        MEMORY   EQU      $3FF0
  65 0
  66 0
  67 0                          *** MAIN PROGRAM   ***
  68 0                          *
  69 0
  70            00000B00                ORG      $B00
  71
  72
  73   00000B00 48E7FFFF        DATINTR  MOVEM.L  A0-A7/D0-D7,-(A7)     SAVE OLD REGISTERS
  74   00000B04 4280                    CLR.L    D0
  75   00000B06 4281                    CLR.L    D1                     CLEAR OUT REG
  76   00000B08 4282                    CLR.L    D2
  77   00000B0A 4284                    CLR.L    D4
  78   00000B0C 4285                    CLR.L    D5
  79
  80   00000B0E 302CFFFF                MOVE.W   DLENGTH(A4),D0         GET MESSAGE DATA SIZE
  81   00000B12 046C0000FFFF    NEXTRNG SUBI.W   #00,TRINGCNT(A4)       SEE IF THERE ARE TRANSMIT RINGS AVAILABLE
  82   00000B18 6700FFFF                BEQ      NORINGS                IF NONE LEFT, GIVE ERROR
  83   00000B1C 046C0001FFFF            SUBI.W   #$01,TRINGCNT(A4)      IF THERE ARE SOME, DECREMENT THE COUNT
  84   00000B22 206CFFFF                MOVE.L   NEXTTRNG(A4),A0        GET XMIT RING BASE ADDRESS
  85
  86   00000B26 B1ECFFFF                CMPA.L   TRNGBOT(A4),A0         SEE IF WE ARE ABOUT TO WRAP AROUND
  87   00000B2A 6608                    BNE.S    UPDATE                 IF NOT UPDATE AS USUAL
  88   00000B2C 296CFFFFFFFF            MOVE.L   TRNGBASE(A4),NEXTTRNG(A4) IF SO, POINT TO TOP OF RING STACK
  89   00000B32 6008                    BRA.S    NOUP                   BRANCH TO NO UPDATE
  90
  91   00000B34 06AC00000008    UPDATE  ADDI.L   #$08,NEXTTRNG(A4)      UPDATE THE ADDRESS OF THE NEXT XMIT RING
                FFFF
  92   00000B3C 2610            NOUP    MOVE.L   (A0),D3                GET XMIT BUFFER BASE ADD
  93   00000B3E 024300FF                ANDI.W   #$00FF,D3              CLEAR STATUS OUT OF REGISTER
  94   00000B42 3A03                    MOVE.W   D3,D5                  STORE THE TMD1 WORD IN REG D5 FOR UPDATE
  95   00000B44 4843                    SWAP     D3                     MOVE WORDS FOR 68000 COMPATIBILITY
  96   00000B46 2643                    MOVE.L   D3,A3                  MOVE XMIT BUFFER ADD. INTO AN ADD. REG
  97   00000B48 068100000001    MOREDATA ADDI.L   #$01,D1                GENERATE NEXT MESSAGE BYTE TO OUTPUT
  98   00000B4E 1681                    MOVE.B   D1,(A3)                MOVE DATA BYTE INTO OUTPUT MEMORY LOCATION
  99   00000B50 06420001                ADDI.W   #$01,D2                INCREMENT BYTE COUNT 1 (TOTAL WORD COUNT)
 100   00000B54 06440001                ADDI.W   #$01,D4                INCREMENT BYTE COUNT 2 (BUFFER WORD COUNT)
 101   00000B58 B042                    CMP.W    D2,D0                  SEE IF THERE ARE MORE DATA WORDS TO OUTPUT
```

```
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Line S Location  Value          Source
 102   00000B5A 670A                    BEQ.S    ENDPAC              IF NOT, THIS IS THE END OF THE PACKET
 103   00000B5C 0C44FFFF                CMP.W    #TBUFLEN,D4         IF SO, SEE IF THERE IS MORE BUF SPACE LEFT
 104   00000B60 6718                    BEQ.S    STARTPAC            IF NOT, GO CHECK IF THIS IS THE START OF PAC
 105   00000B62 528B                    ADDQ.L   #$01,A3             IF SO, INCREMENT BUFFER ADD & GET NEXT WORD
 106   00000B64 60E2                    BRA.S    MOREDATA            GO GET ANOTHER WORD TO PUT INTO THE BUFFER
 107
 108                            * CHECK IF START & END BITS ARE SET  *
 109
 110   00000B66 082C0002FFFF    ENDPAC  BTST.B   #02,RINGSTAT(A4)    SEE IF START BIT HAD BEEN SET BEFORE
 111   00000B6C 6706                    BEQ.S    BOTHBITS            IF NOT, SET BOTH START & END OF PAC BITS IN TMD1
 112   00000B6E 00450100        ENDBIT  ORI.W    #$0100,D5           OTHERWISE SET ONLY THE END OF PACKET BIT
 113   00000B72 6018                    BRA.S    TMDFIX              GO FINISH UP TRANSMIT DESCRIPTOR 1
 114   00000B74 00450200        BOTHBITS ORI.W   #$0200,D5           SET END OF PACKET BIT IN TMD1
 115   00000B78 60F4                    BRA.S    ENDBIT              NOT GO SET END OF PACKET BIT
 116   00000B7A 082C0002FFFF    STARTPAC BTST.B  #02,RINGSTAT(A4)    SEE IF START BIT HAD BEEN SET BEFORE
 117   00000B80 660A                    BNE.S    TMDFIX              IF SO GO FINISH OF TMD1 STATUS
 118   00000B82 00450200                ORI.W    #$0200,D5           IF NOT SET START OF PACKET BIT IN TMD1
 119   00000B86 08EC0002FFFF            BSET.B   #02,RINGSTAT(A4)    SET THE START STATUS BIT IN THE RINGSTATUS
 120
 121                            *  FIX UP THE TRANSMIT DESCRIPTOR RINGS  *
 122
 123   00000B8C 5888            TMDFIX  ADDQ.L   #04,A0              GENERATE ADDRESS OF TMD2
 124   00000B8E 0A44FFFF                EORI.W   #$FFFF,D4           TAKE 2'S COMPLEMENT OF WORD COUNT
 125   00000B92 06440001                ADDI.W   #$01,D4
 126   00000B96 0044F000                ORI.W    #$F000,D4           FORCE FOUR MSB TO ONES
 127   00000B9A 3084                    MOVE.W   D4,(A0)             MOVE MESSAGE BYTE COUNT INTO TMD2
 128   00000B9C 4284                    CLR.L    D4                  CLEAR OUT MESSAGE COUNT FOR NEXT BUFFER
 129   00000B9E 5488                    ADDQ.L   #$02,A0             GENERATE ADDRESS OF TMD3
 130   00000BA0 30BC0000                MOVE.W   #$0000,(A0)         CLEAR OUT TMD3
 131   00000BA4 5988                    SUBQ.L   #04,A0              GENERATE ADDRESS OF TMD1
 132   00000BA6 00458000                ORI.W    #$8000,D5           SET OWN BIT, GIVING OWNERSHIP TO LANCE
 133   00000BAA 3085                    MOVE.W   D5,(A0)             PUT TMD1 BACK INTO XMIT RING
 134
 135                            *   CHECK TO SEE IF WE NEED TO GENERATE ANOTHER MESSAGE BUFFER   *
 136
 137   00000BAC B042                    CMP.W    D2,D0               SEE IF THERE ARE MORE DATA WORDS TO OUTPUT
 138   00000BAE 6600FF62                BNE      NEXTRNG             IF THERE ARE, SEE IF ANY BUFFER RINGS LEFT
 139   00000BB2 08AC0002FFFF            BCLR.B   #02,RINGSTAT(A4)    CLEAR OUT THE START OF PACKET BIT ON RINGSTAT
 140
 141   00000BB8 4CDFFFFF        XMITDONE MOVEM.L  (A7)+,D0-D7/A0-A7   RETRIVE OLD REGISTERS
 142
 143   00000BBC 4E73                    RTE                          RETURN FROM EXCEPTION PROCESSION
 144   00000BBE 00000000                END

no errors detected.


Options in effect:

  NOA,BRL,NOCEX,CL,FRL,MC,MD,NOMEX,O,NOPCO,NOPCS,LIST,NOSTR,FORMAT,NOMOTOROLA
```

FEATURES

- ☐ Compatible with Ethernet and IEEE-802.3 Specifications
- ☐ Crystal-controlled Manchester Encoder/Decoder
- ☐ Manchester Decoder acquires clock and data within six-bit times with an accuracy of ±3 ns.
- ☐ Guaranteed carrier and collision detection squelch threshold limits
  - — Carrier/collision detected for inputs more negative than −275 mV
  - — No carrier/collision for inputs more positive than −175 mV
- ☐ Input signal conditioning rejects transient noise
  - — Transients <10 ns for collision detector inputs
  - — Transients <20 ns for carrier detector inputs
- ☐ Receiver decodes Manchester data with up to ±20 ns clock jitter (at 10 MHz)
- ☐ TTL-compatible host interface
- ☐ Transmit oscillator accuracy ±0.01% (without adjustments)

GENERAL DESCRIPTION

The MK68591/2 Serial Interface Adapter (SIA) is a Manchester Encoder/Decoder compatible with Ethernet and IEEE-802.3 specifications. In an Ethernet/IEEE-802.3 application, the MK68591/2 interfaces the MK68590 Local Area Network Controller for Ethernet (LANCE™) to the Ethernet transceiver cable, acquires clock and data within 6 bit-times and decodes Manchester data up to ± 20 ns phase jitter at 10 MHz. SIA provides both guaranteed signal threshold limits and transient noise suppression circuitry in both data and collision paths to minimize false start conditions.

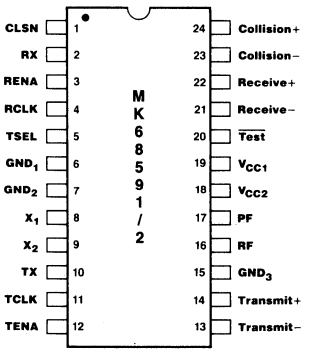


Figure 1. Pin Assignments

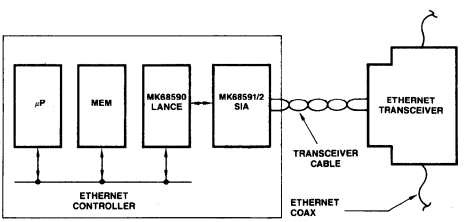


Figure 2. Typical Ethernet Node

LANCE is a trademark of Thomson Components - Mostek Corporation.

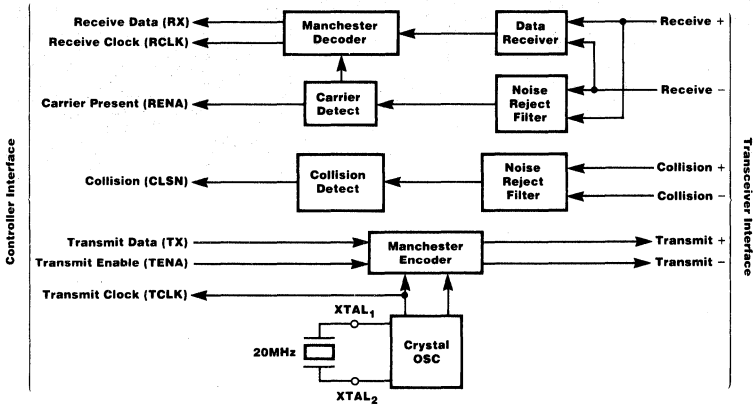


Figure 3. MK68591/2 Block Diagram

PIN DESCRIPTION

CLSN — **Collision (output).** A TTL active high output. Signals at the Collision ± terminals meeting threshold and pulse width requirements will produce a logic high at CLSN output. When no signal is present at Collision ±, CLSN output will be low.

RX — **Receive Data (output).** A MOS/TTL output, recovered data. When there is no signal at Receive ± and $\overline{\text{TEST}}$ is high, RX is high. RX is actuated with RCLK and remains activated until end of message. During reception, RX is synchronous with RCLK and changes after the rising edge of RCLK.

RENA — **Receive Enable (output).** A TTL active high output. When there is no signal at Receive ±, RENA is low. Signals at Receive± meeting threshold and pulse width requirements will produce a logic high at RENA. When Receive ± becomes idle, RENA returns to the low state synchronous with the rising edge of RCLK.

RCLK — **Receive Clock (output).** A MOS/TTL output recovered clock. When there is no signal at Receive ± and $\overline{\text{TEST}}$ is high, RCLK is low. RCLK is activated after the third negative data transition at Receive ±, and remains active until end of message. When $\overline{\text{TEST}}$ is low, RCLK is enabled.

TX — **Transmit (input).** TTL compatible input. When TENA is high, signals at TX meeting setup and hold time to TLCK will be encoded as normal Manchester at Transmit + and Transmit –.

TX High: Transmit + is negative with respect to Transmit – for first half of data bit cell.

TX Low: Transmit + is positive with respect to Transmit – for first half of data bit cell.

TENA — **Transmit Enable (input).** TTL compatible input. Active high data encoder enable. Signals meeting setup and hold time to TCLK allow encoding of Manchester data from TX to Transmit + and Transmit –.

TCLK — **Transmit Clock (output).** MOS/TTL output. TCLK provides symmetrical high and low clock signals at data rate for reference timing of data to be encoded. It also provides clock signals for the controller chip (MK68590 LANCE) and an internal timing reference for receive path voltage controlled oscillators.

Transmit +
Transmit – — **Transmit (outputs).** A differential line output. This line pair is intended to operate into terminated transmission lines. For signals meeting setup and hold time to TCLK at TENA and TX. The Manchester clock and data are outputted at Transmit +/Transmit –. When operating into a 78Ω terminated transmission line, signalling meets the required output

levels and skew for both Ethernet and IEEE-802.3 drop cables.

Receive +
Receive – **Receiver (inputs).** A differential input. A pair of internally biased line receivers consisting of a carrier detect receiver with offset threshold and noise filtering to detect the signal, and a data recovery receiver with no offset for Manchester data decoding.

Collision +
Collision – **Collision (inputs).** A differential input. An internally biased line receiver input with offset threshold and noise filtering. Signals at Collision ± have no effect on data path functions.

TSEL **Transmit Mode Select.** An open collector output and sense amplifier input.

TSEL Low: Idle transmit state Transmit + is positive with respect to Transmit –.

TSEL High: Idle transmit state Transmit + and Transmit – are equal, providing "zero" differential to operate transformer coupled loads.

When connected with an RC network, TSEL is held low during transmission. At the end of transmission, the open collector output is disabled, allowing TSEL to rise and provide a smooth transmission from logic high to "zero" differential idle. Delay and output return to zero are externally controlled by the RC time constant at TSEL. (See Figure 9.)

X_1, X_2 **Biased Crystal Oscillator.** X_1 is the input and X_2 is the bypass port. When connected for crystal operation, the system clock which appears at TCLK is half the frequency of the crystal oscillator. X_1 may be driven from an external source of two times the data rate. In which case X_2 should be left floating.

RF **Frequency Setting Voltage Controlled Oscillator (V_{CO}) Loop Filter.** This loop filter output is a reference voltage for the receive path phase detector. It also is a reference for timing noise immunity circuits in the collision and receive enable path. Nominal reference V_{CO} gain is 1.25 TCLK frequency MHz/V.

PF **Receive Path V_{CO} Phase Lock Loop Filter.** This loop filter input is the control for receive path loop damping. Frequency of the receive V_{CO} is internally limited to transmit frequency ± 12%. Nominal receive V_{CO} gain is 0.25 reference V_{CO} gain MHz/V.

$\overline{TEST}$ **Test Control (input).** A static input that is connected to V_{CC} for normal MK68591/2 operation and to ground for testing of receive path function. When $\overline{TEST}$ is grounded, RCLK and RX are enabled so that receive path loop may be functionally tested.

GND_1 **High Current Ground**

GND_2 **Logic Ground**

GND_3 **Voltage Controlled Oscillator Ground**

V_{CC1} **High Current and Logic Supply**

V_{CC2} **Voltage Controlled Oscillator Supply**

FUNCTIONAL DESCRIPTION

The MK68591/2 Serial Interface Adapter (SIA) has three basic functions. It is a Manchester Encoder/line driver in the transmit path, a Manchester Decoder with noise filtering and quick lock-on characteristics in the receive path, and a signal detect/converter (10 MHz differential to TTL) in the collision path. In addition, the SIA provides the interface between the TTL logic environment of the LANCE and the differential signaling environment in the transceiver cable.

TRANSMIT PATH

The transmit section encodes separate clock and NRZ* data input signals meeting the set up and hold time to TCLK at TENA and TX, into a standard Manchester II serial bit stream. The transmit outputs (Transmit +/ Transmit –) are designed to operate into terminated transmission lines. When operating into a 78Ω terminated transmission line, signaling meets the required output levels and skew for both Ethernet and IEEE-802.3.

Transmitter Timing and Operation

A 20 MHz fundamental mode crystal oscillator provides the basic timing reference in the SIA. It is divided by two to create the transmit clock reference (TCLK). Both 20 MHz and 10 MHz clocks are fed into the Manchester Encoder to generate the transitions in the encoded data stream. The 10 MHz clock, TCLK, is used by the SIA to internally synchronize transmit data (TX) and transmit

*Non-Return-to-Zero

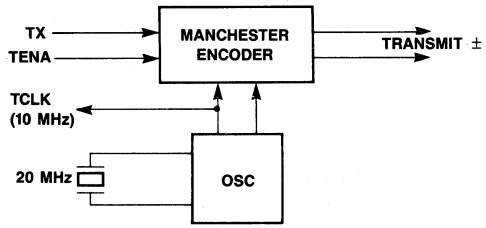


Figure 4. Transmit Section

enable (TENA). TCLK is also used as a stable bit-rate clock by the receive section of the SIA and by other devices in the system (the MK68590 LANCE uses TCLK to drive its internal state machine). The oscillator may use an external 0.005% crystal or an external TTL level input as a reference. Transmit accuracy of 0.01% is achieved (no external adjustments are required).

TENA is activated when the first bit of data is made available on TX. As long as TENA remains high, signals at TX will be encoded as Manchester and will appear at Transmit + and Transmit −. When TENA goes low, the differential transmit outputs go to one of the two idle states defined below:

- TSEL High: The idle state of Transmit +/ Transmit − yields "zero" differential to operate transformer coupled loads (see Figure 14a).

- TSEL Low: In this idle state, Transmit + is positive to Transmit − yielding logical high (see Figure 14b).

RECEIVE PATH

The principle function of the receiver is the separation of the Manchester encoded data stream into clock and NRZ data.

Input Signal Conditioning

Before the data and clock can be separated, it must be determined whether there is "real" data or unwanted noise at the transceiver interface. The MK68591/2 SIA carrier detection receiver provides a static noise margin of −175 to −275 mV for received carrier detection. These DC thresholds assure that no signal more positive than −175 mV is ever decoded and that signals more negative than −275 mV are always decoded. Transient noise of less than 10ns duration in the collision path and 20 ns duration in the data path are also rejected.

This signal conditioning prevents unwanted idle noise on the transceiver cable from causing "false starts" in the receiver. This helps assure a valid response to "real" data.

The receiver section, shown in Figure 6, consists of two data paths. The receive data path is designed to be a zero threshold, high bandwidth receiver. The carrier detection receiver has an additional bias generator. Only data amplitudes larger than the bias level are interpreted as valid data. The noise rejection filter prevents noise transients of less than 20 ns from enabling the data receiver output. The collision detector similarly rejects noise transients of less than 10 ns.

Receiver Section Timing

Receive Enable (RENA) is the "carrier present" indication established when a signal of sufficient amplitude (V_{IDC}) and duration (t_{RPWR}) is present at the receive inputs. Receive Clock (RCLK) and Receive Data (RX) become available after the third negative data transition

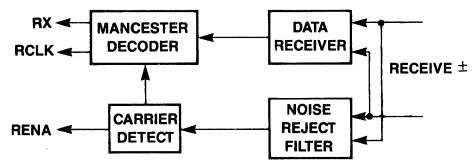


Figure 5. Receiver

at Receive +/ Receive − inputs, and stay active until the end of a packet. During reception, RX is synchronous with RCLK, changing after the rising edge of RCLK.

The receiver detects the end of a packet when the normal transition on the differential inputs cease. After the last low-to-high transition, RENA goes low and RCLK completes one last cycle, storing the last data bit. It then becomes and remains low (see Receive End of Packet Timing diagrams). When $\overline{TEST}$ is low, RCLK continues to run, tracking data (if available) or synchronizes with TCLK.

Receive Clock Control

To insure quick capture of incoming data, the receiver phase-locked-loop is frequency locked to the transmit oscillator and it phase locks to incoming data edges. Clock and data are available within 6 bit times (accurate to within ±3 ns). The SIA will decode jittered data of up to ±20 ns (see Figure 7).

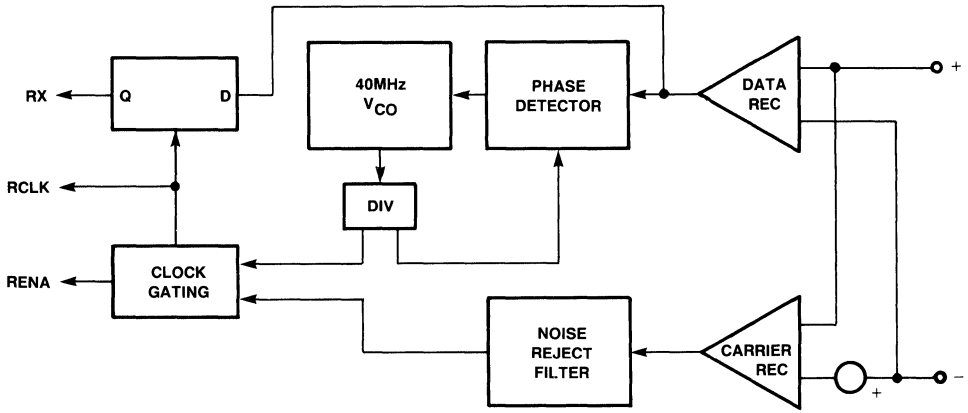


Figure 6. Receiver Section Detail

Differential I/O Terminations

The differential input for the Manchester data (receive ±) is externally terminated by two 40.2 Ω±1% resistors and one optional common mode bypass capacitor. The differential input impedance Z_{IDF} and the common mode input Z_{ICM} are specified so that the Ethernet specification for cable termination impedance is met using standard 1% resistor terminators. The Collision ± differential input is terminated in exactly the same way as the receive input (see Figure 8).

Collision Detection

The Ethernet Transceiver detects collisions on the Ethernet and generates a 10MHz signal on the transceiver cable (Collision +/ Collision –). This collision signal passes through an input stage which assures signal levels and pulse duration. When the signal is detected by the SIA, the SIA sets the CLSN line high. This condition continues for approximately 190ns after the last low-to-high transition on Collision +/ Collision –.

APPLICATION RECOMMENDATIONS

The differential input and output pins should be transformer coupled to meet the IEEE 802.3 16 volt fault tolerance specifications.

This device is not recommended for operation in wire wrapped boards.

This device should be handled with care to avoid electro-static-discharge (ESD) failures. Although this is a bipolar device, serial input and output circuits are designed to meet the IEEE 802.3 specifications and cannot be protected against ESD without affecting the performance of the device.

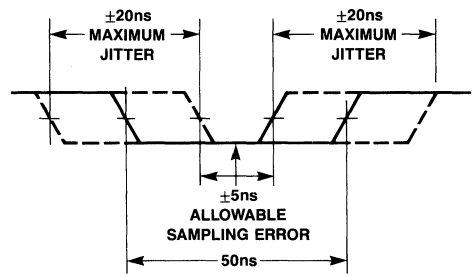
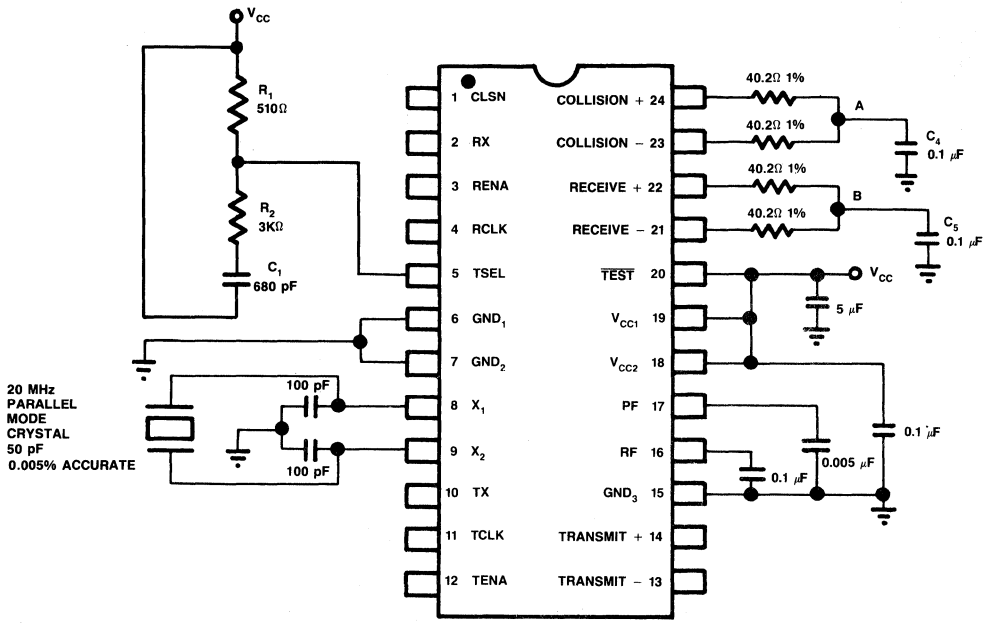


Figure 7. Maximum Jitter Impact On Sampling



NOTES:

1. Connect R_1, R_2, C_1 for 0 differential nontransmit. Connect to ground for logic 1 differential nontransmit. (See Figure 9.)
2. Pin 20 shown for normal device operation.
3. Nodes A and B may be connected directly to ground for proper decoder operations, or to the common mode bypass C_4 and C_5. Some direct coupled transceivers require C_4 and C_5 to ground for proper operation.

Figure 8. MK68591/2 External Component Diagram

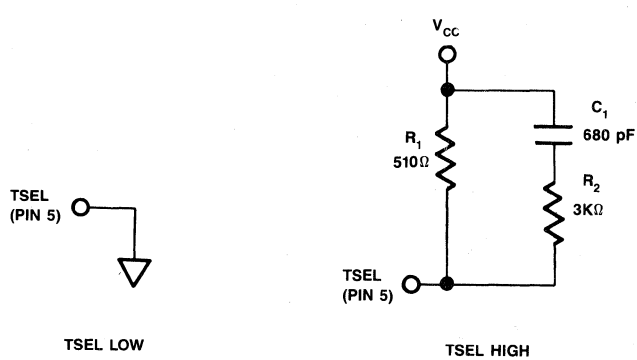


Figure 9. Transmit Mode Select (TSEL) Connection

ABSOLUTE MAXIMUM RATINGS*

Storage Temperature ..... −65 to +150°C
Temperature (Ambient) Under Bias ..... 0 to 70°C
Supply Voltage to Ground Potential Continuous ..... +7.0V
DC Voltage Applied to Outputs for High Output State ..... −0.5 to +V_{CC} max
DC Input Voltage (Logic Inputs) ..... +5.5V
DC Input Voltage (Receive/Collision) ..... −6 to +6 V
Transmit ± Output Current ..... −50 to +5 mA
DC Output Current, Into Outputs ..... 100 mA
DC Input Current (Logic Inputs) ..... ±30 mA

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE The following conditions apply unless otherwise specified:

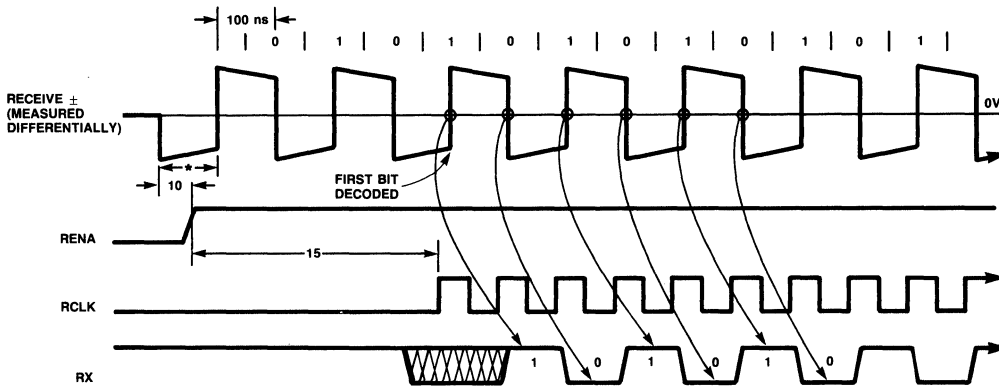
T_A = 0 to 70°C, V_{CC} = 5.0 V±10 percent, MIN = 4.5 V, MAX = 5.5 V, period of crystal oscillator (T_{OSC}) = 50 ns

Parameters	Description		Test Conditions	Min	Typ	Max	Units
V_{OH}	Output High Voltage RX, RENA, CLSN, TCLK, RCLK		I_{OH} = −1.0 mA	2.4	3.4		V
V_{OL}	Output Low Voltage RCLK, TCLK, RENA, RX, CLSN, TSEL		I_{OL} = 16 mA,		0.36	0.5	V
			I_{OL} = 1 mA		0.25	0.4	
V_{OD}	Differential Output Voltage	V_0	R_L = 78 Ω	550	670	770	mV
	(Transmit +) − (Transmit −)	$\overline{V_0}$	Figure 19	−550	−670	−770	
$V_{OD\ OFF}$	Transmit Differential Output Idle Voltage		R_L =78 Ω Figure 19 TSEL = HIGH	−20	0.5	20	mV
$I_{OD\ OFF}$	Transmit Differential Output Idle Current			−0.5	±0.1	0.5	mA
V_{CMT}	Common Mode Output Transmit Voltage		Figure 19	0	2.5	5	V
V_{ODI}	Differential Output Voltage Imbalance (Transmit ±) | | V_0 | − | $\overline{V_0}$ | |		R_L = 78 Ω		5	20	mV
V_{IH}	Input High Voltage TTL			2.0			V
I_{IH}	Input High Current TTL		V_{CC} = Max, V_{IN} = 2.7 V			+50	μA
V_{IL}	Input Low Voltage TTL					0.8	V
I_{IL}	Input Low Current TTL		V_{CC} = Max, V_{IN} = 0.4 V		−270	−400	μA
V_{IRD}	Differential Input Threshold (Rec Data)		Figure 20	−25	0	+25	mV
V_{IDC}	Differential Input Threshold (Carrier/Collision ±)		Figure 20	−175	−225	−275	mV
I_{CC}	Power Supply Current		t_{OSC} = 50 ns		125	180	mA
			t_{OSC} = 50 ns, T_A = Max			160	
V_{IB}	Input Breakdown Voltage V_I = +5.5 (TX, TENA, $\overline{TEST}$)		I_I = 1 mA	5.5			V
V_{IC}	Input Clamp Voltage		I_{IN} = −18 mA			−1.2	V
I_{SCO}	RX, TCLK, CLSN, RENA, RCLK Short Circuit Current			−40	−80	−150	mA
R_{IDF}	Differential Input Resistance		V_{CC} = 0 to Max	6k	8.4k	13k	ohm
R_{ICM}	Common Mode Input Resistance		V_{CC} = 0 to Max	1.5k	2.1k	7.5k	ohm
V_{ICM}	Receive and Collision Input Bias Voltage		I_{IN} = 0	1.5	3.5	4.2	V
I_{ILD}	Receive and Collision Input Low Curent		V_{IN} = −1 V	−0.6	−1.06	−1.64	mA
I_{IHD}	Receive and Collision Input High Current		V_{IN} = 6 V	+0.4	+0.6	+1.10	mA
I_{IHZ}	Receive and Collision Input High Current		V_{CC} = 0, V_{IN} = +6 V	0.4	1.28	1.86	mA

SWITCHING CHARACTERISTICS OVER OPERATING RANGE The following conditions apply unless otherwise specified: T_A = 0 to 70°C, V_{CC} = 5.0 V±10 percent, MIN = 4.5 V, MAX = 5.5 V, T_{OSC} = 50 ns

#	Signal	Parameters	Description	Test Conditions	Min	Typ	Max	Units
RECEIVER SPECIFICATION								
1	RCLK	t_{RCT}	RCLK Cycle Time	C_L = 50 pF Figure 17a (See note)	85	100	118	ns
2	RCLK	t_{RCH}	RCLK High Time		38	50		ns
3	RCLK	t_{RCL}	RCLK Low Time		38	50		ns
4	RCLK	t_{RCR}	RCLK Rise Time			2.5	8	ns
5	RCLK	t_{RCF}	RCLK Fall Time			2.5	8	ns
6	RX	t_{RDR}	RX Rise Time			2.5	8	ns
7	RX	t_{RDF}	RX Fall Time			2.5	8	ns
8	RX	t_{RDH}	RX Hold Time (RCLK to RX Change)		5	8		ns
9	RX	t_{RDS}	RX Prop Delay (RCLK to RX Stable)			8	25	ns
10	RENA	t_{DPH}	RENA Turn-On Delay (V_{IDC} Max on Receive ± to $RENA_H$)	Figures 10, 16a, and 20		50	80	ns
11	RENA	t_{DPO}	RENA Turn-Off Delay (V_{IDC} Min on Receive ± to $RENA_L$)	Figures 11 and 20		265	300	ns
12	RENA	t_{DPL}	RENA Low Time	Figure 11	120	200		ns
13	Rec ±	t_{RPWR}	Receive ± Input Pulse Width to Reject (Input<V_{IDC} Min)	Figures 16a and 20		30	20	ns
14	Rec ±	t_{RPWO}	Receive ± Input Pulse Width to Turn-On (Input>V_{IDC} Max)	Figures 16a and 20	45	30		ns
15	RCLK	t_{RLT}	Decoder Acquisition Time	Figure 10		390	450	ns
COLLISION SPECIFICATION								
16	Coll ±0	t_{CPWR}	Collision Input Pulse Width to Reject (Input<V_{IDC} Min)	Figures 16b and 20		18	10	ns
17	Coll ±	t_{CPWO}	Collision Input Pulse Width to Turn-On (Collision ± Exceeds V_{IDC} Max)		26	18		ns
18	Coll ±	t_{CPWE}	Collision Input to Turn-Off CLSN (Input<V_{IDC} Max)		80	117		ns
19	Coll ±	t_{CPWN}	Collision Input to Not Turn-Off CLSN (Input>V_{IDC} Min)			117	160	ns
20	CLSN	t_{CPH}	CLSN Turn-On Delay (V_{IDC} Max on Collision ± to $CLSN_H$)	Figures 15, 16b, and 20		33	50	ns
21	CLSN	t_{CPO}	CLSN Turn-Off Delay (V_{IDC} Min on Collision ± to $CLSN_L$)			133	160	ns
TRANSMITTER SPECIFICATION								
22	TCLK	t_{TCL}	TCLK Low Time	t_{OSC} = 50 ns Figures 17b and 18	45	50	55	ns
23	TCLK	t_{TCH}	TCLK High Time		45	50	55	ns
24	TCLK	t_{TCR}	TCLK Rise Time			2.5	8	ns
25	TCLK	t_{TCF}	TCLK Fall Time			2.5	8	ns
26	TX, TENA	t_{TDS}, t_{TES}	TX and TENA Setup Time to TCLK	Figures 13, 14a, 14b, and 17b	5	1.1		ns
27	TX, TENA	t_{TDH}, t_{TEH}	TX and TENA Hold Time to TCLK		5	−1.1		ns
28	TX ±	t_{TOCE}	Transmit ± Output, (Bit Cell Center to Edge)	Figures 14a, 14b, and 19	49.5	50	50.5	ns
29	TCLK	t_{OD}	TCLK High to Transmit ± Output			80	100	ns
30	TX ±	t_{TOR}	Transmit ± Output Rise Time	20 through 80 percent Figure 19		2	4	ns
31	TX ±	t_{TOF}	Transmit ± Output Fall Time			2	4	ns
32	TX ±	V_{OD}	Undershoot Voltage at Zero Differential Point on Transmit Return to Zero (End of Message)	Figure 14a			−100	mV

NOTE:
Assumes equal capacitance loading on RCLK and RX.



* PULSE WIDTH OF ≥ 45 ns IS ALWAYS RECOGNIZED.
HOWEVER, PULSE WIDTH OF ≤ 20 ns IS REJECTED.

Figure 10. Receiver Timing — Start of Packet

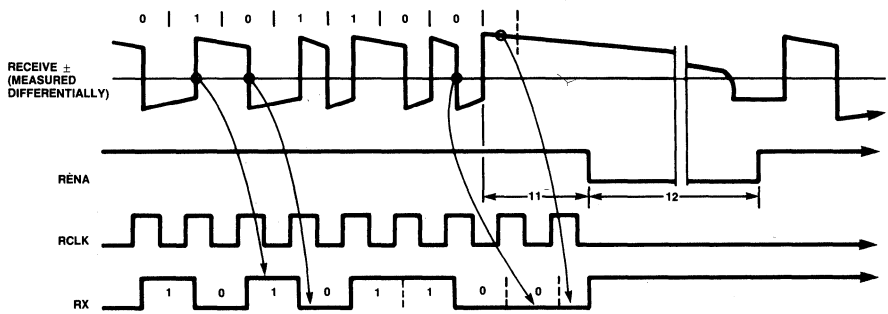


Figure 11. Receiver Timing — End of Packet (Last Bit = 0)

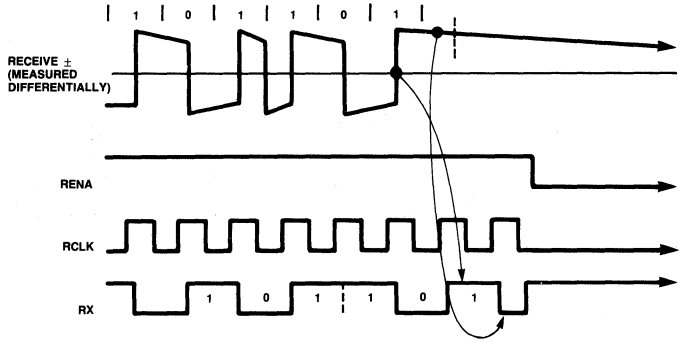


Figure 12. Receiver Timing — End of Packet (Last Bit = 1)

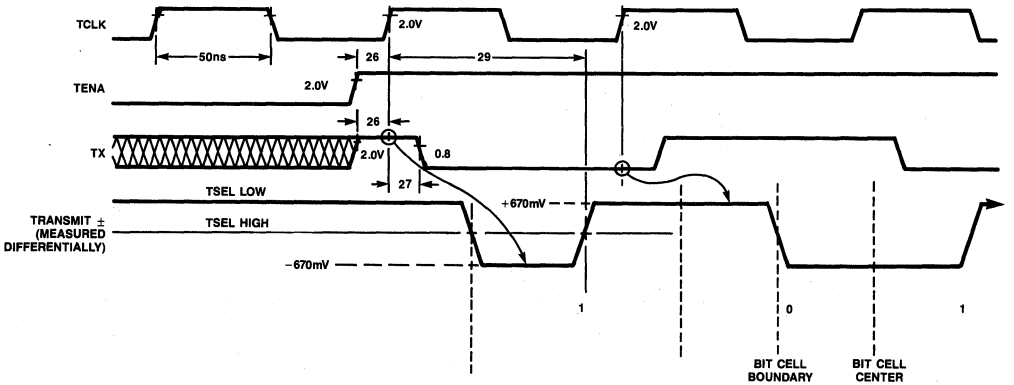


Figure 13. Transmitter Timing — Start of Transmission (TSEL Low, TSEL High)

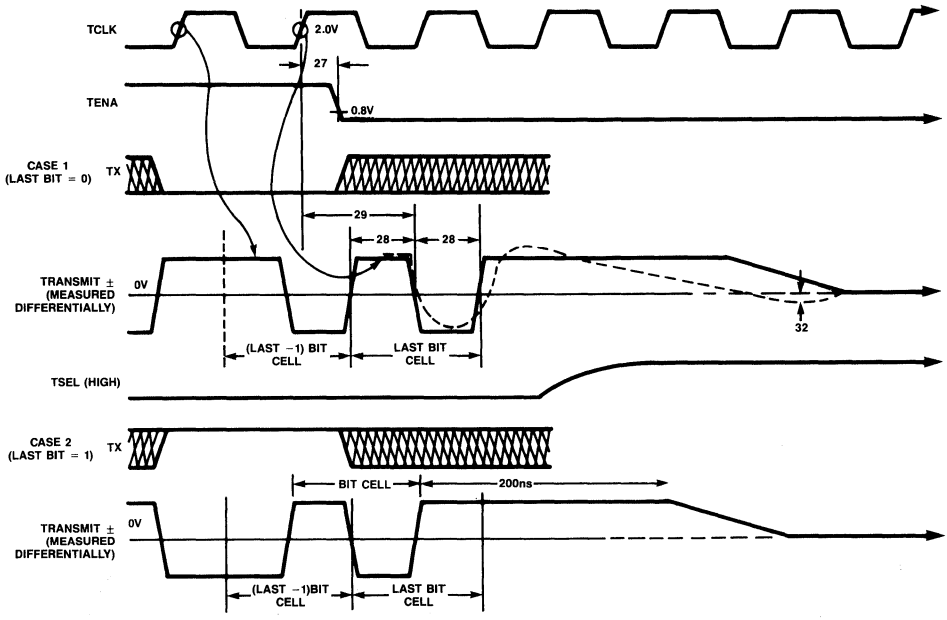


Figure 14a. Transmitter Timing — End of Transmission (TSEL High)

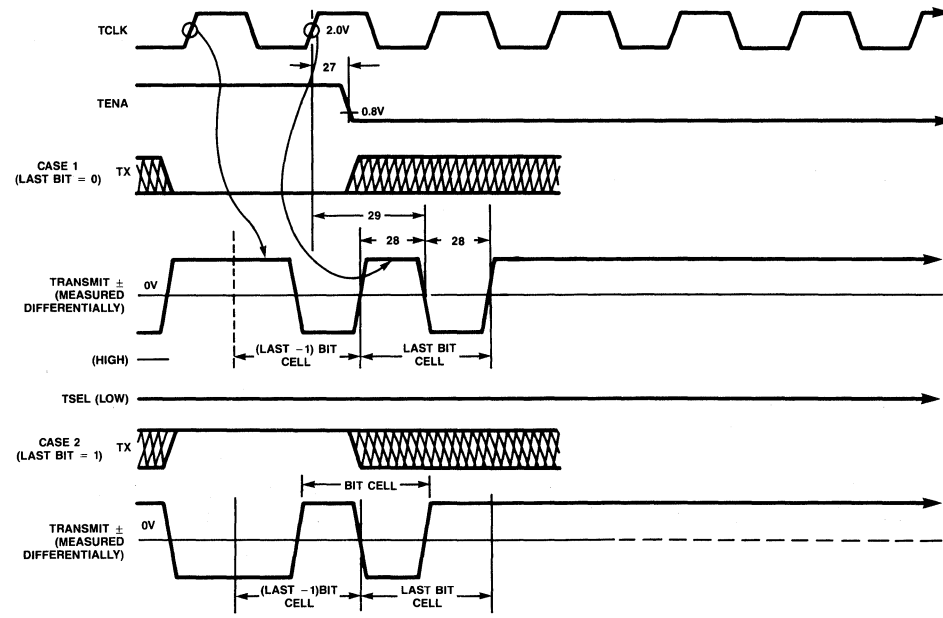
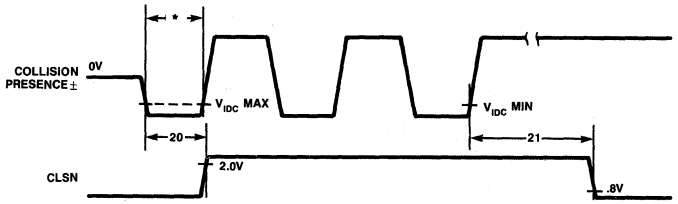


Figure 14b. Transmitter Timing — End of Transmission (TSEL Low)



* PULSE WIDTH OF −26 ns IS GUARANTEED TO BE RECOGNIZED: HOWEVER, PULSE WIDTH OF ≤ 10ns IS REJECTED

Figure 15. Collision Timing

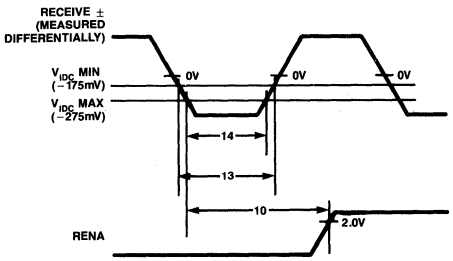


Figure 16a. Receive ± Input Pulse Width Timing

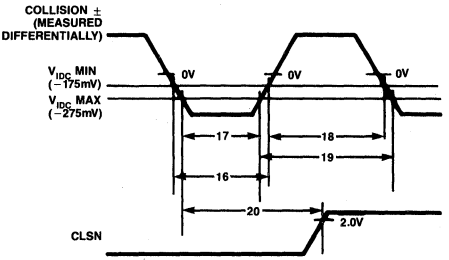


Figure 16b. Collision ± Input Pulse Width Timing

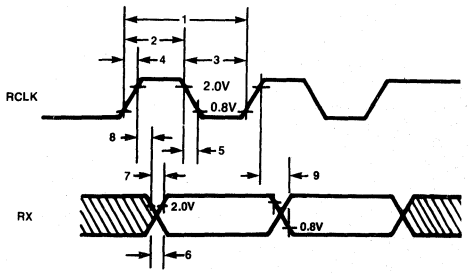


Figure 17a. RCLK and RX Timing

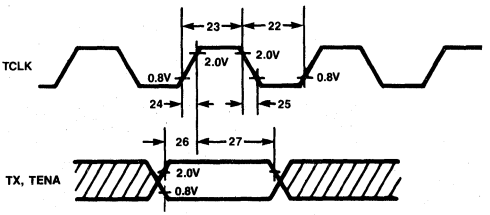


Figure 17b. TCLK and TX Timing

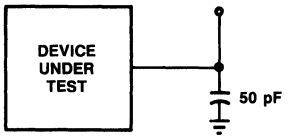


Figure 18. Test Load For RX, RENA, and TCLK

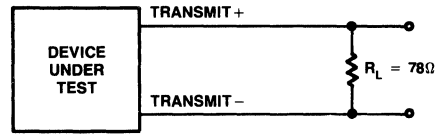


Figure 19. Transmit ± Output Test Circuit

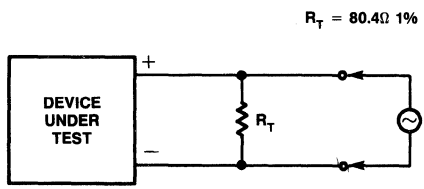
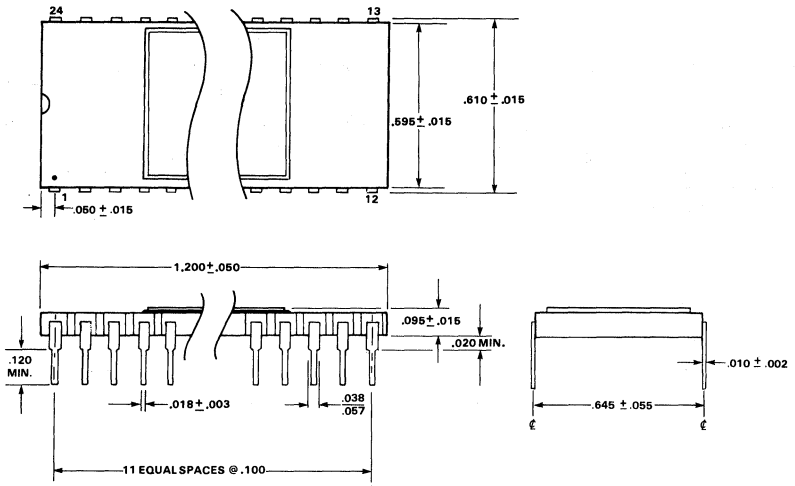


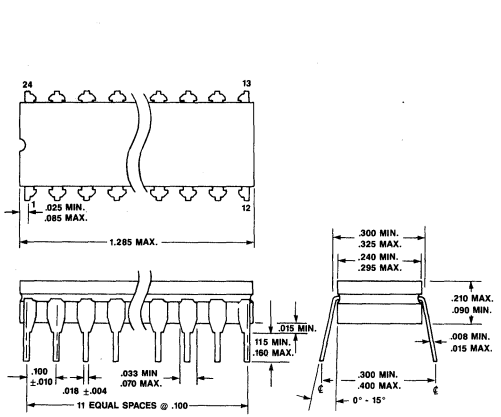
Figure 20. Receive ± and Collision ± Input Test Circuit

MK68591 (600 mil)

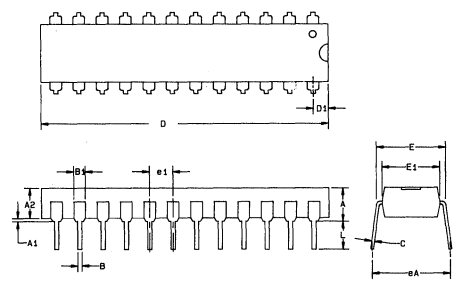


Ceramic Dual-In-Line Package (P)
24 Pin

MK68592 (300 mil)



Cerdip Hermetic Package (J)
24 Pin



NOTES

1. OVERALL LENGTH INCLUDES .010 IN. FLASH ON EITHER END OF THE PACKAGE.
2. PACKAGE STANDOFF TO BE MEASURED PER JEDEC REQUIREMENTS.
3. THE MAXIMUM LIMIT SHALL BE INCREASED BY .003 IN. WHEN SOLDER LEAD FINISH IS SPECIFIED.

DIM	INCHES		NOTES
	MIN	MAX	
A	–	.210	2
A1	.015	–	2
A2	.120	.140	
B	.015	.021	3
B1	.050	.070	
C	.008	.012	3
D	1.220	1.250	1
D1	.060	.075	
E	.300	.325	
E1	.240	.270	
e1	.090	.110	
eA	.300	.400	
L	.120	–	

Plastic Package (N)
24 Pin

THOMSON COMPONENTS
MOSTEK

MK5030P,K

StarLAN HUB CHIP

COMMUNICATIONS PRODUCTS

FEATURES

- ☐ Complete Hub Logic device which conforms to StarLAN specification.
- ☐ Supports Multi-point extension (MPE).
- ☐ Auto compensation for wiring reversal.
- ☐ 12 port HUB.
- ☐ Optional retime circuit.
- ☐ Cascadable. Two levels may be cascaded and still appear to the network as one yielding up to a 121 port HUB.
- ☐ Supports up to a 10 layer network.
- ☐ Auto preamble generation to eliminate bit loss.
- ☐ Selectable active carrier polarity sense.
- ☐ Jabber function isolates network failures.
- ☐ Optional minimum frame length enforcement.
- ☐ Collision detection:
  - multiple inputs
  - missing mid-bit transition
  - transitions too close together
  - transitions too far apart
  - AT&T release 1 collision presence signal.
- ☐ Digital phase lock loop.
- ☐ 6X clock yields 162 nS jitter tolerance.
- ☐ Transmit Data Trailer enforcement.
- ☐ Input protection at end of frame (20 μs).
- ☐ Pin selectable high-end HUB versus intermediate HUB.
- ☐ Optional internal pulse stretcher for carrier sense squelch.
- ☐ UPLINK and DOWNLINK active status outputs.

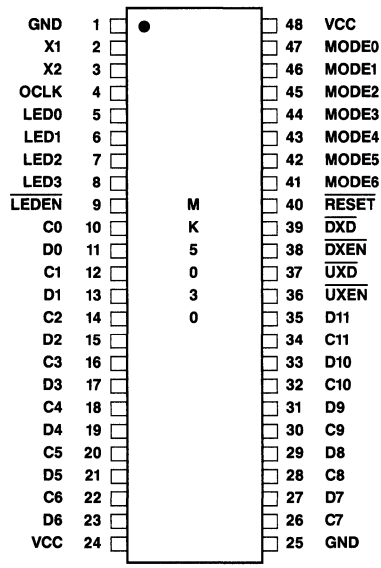


Figure 1. MK5030 Pin Assignment

- ☐ UPLINK and DOWNLINK collision status outputs.
- ☐ Per port jabber status output.
- ☐ On chip crystal oscillator circuitry.
- ☐ 35 mW typical power dissipation.
- ☐ CMOS technology.
- ☐ 48 pin DIP.
- ☐ Single 5-volt supply.
- ☐ All inputs and outputs TTL compatible.*
- ☐ Industrial version available.

GENERAL DESCRIPTION

The MK5030-HUB is a 48 pin CMOS VLSI device that simplifies the design and implementation of a StarLAN compatible HUB. This chip provides all the digital logic necessary in a HUB.

***NOTE:** Crystal inputs have CMOS thresholds.

PIN DESCRIPTION:

X1, X2 — Inputs. Either connect a 6.00 ±.005% MHz crystal between the pins, or leave X2 not connected and apply a 6.0 MHz ±.01% square wave to X1. (Refer to Figure 7.)

OCLK — Output. Provides a TTL CLK output from the above crystal oscillator. This is useful when cascading devices.

C0-C11 — Schmitt inputs. Carrier sense inputs. Active state is selectable. Refer to MODE4 below.

D0-D11 — Inputs. Received data streams.

$\overline{UXD}$ — Output. UPLINK data stream to the next UPPER HUB, if any, in the network hierarchy.

$\overline{UXEN}$ — Output. UPLINK transmit enable indicating that $\overline{UXD}$ contains valid data.

$\overline{DXD}$ — Output. Downlink data stream to all ports. If MODE1 = 1, then this data stream is derived from Port 11. If MODE1 = 0 then this data stream is identical to $\overline{UXD}$.

$\overline{DXEN}$ — Output. Downlink transmit enable to all ports. If MODE1 = 1, then this data stream is derived from Port 11. If MODE1 = 0, then this data stream is identical to $\overline{UXEN}$.

MODE0 — Input. Testmode. Should be tied high for normal operation. Testmode is useful only for semiconductor device production test.

MODE1 — Input. If MODE1 = 1, then the chip is an intermediate hub; and C0-10/D0-10 inputs will be used as UPLINK inputs and C11/D11 as the DOWNLINK input. If MODE1 = 0, then the chip is a high-end hub; C0-11/D0-11 inputs will be used as UPLINK inputs and DOWNLINK outputs ($\overline{DXD}$, $\overline{DXEN}$) will internally be connected to the UPLINK outputs ($\overline{UXD}$, $\overline{UXEN}$). See Figure 5.

MODE2 — Inputs. If MODE2 = 0, then the input carriers have been externally stretched and no internal stretcher is desired. This stretcher is required as part of the squelch function. Refer to Figure 2. If MODE2 = 1, then the input carriers are threshold set off the incoming data stream and an internal pulse stretcher must be used. With MODE2 = 1, users do not need to use one-shots externally for each port.

MODE3 — Input. If MODE3 = 1, then the retimer circuit is enabled as specified by IEEE 802.3. If MODE3 = 0, then the retimer circuit is disabled. This allows HUBs in close physical proximity to be cascaded together and appear to the network as one HUB. Refer to Figure 3.

MODE4 — Input. Selects carrier active state. If MODE4 = 0, then the carrier inputs (C0-C11) are active low. If MODE4 = 1 then the carrier inputs (C0-C11) are active high.

MODE5 — Input. If MODE5 = 1, then auto preamble generation is enabled. The chip will initiate preamble transmission once phase lock is obtained. Once the transmit FIFO is sufficiently full, transmit data is obtained from the FIFO. This decreases the amount of bits a HUB implementation will lose. Depending on the implementation, bits may actually be gained. If MODE5 = 0, then automatic preamble generation is disabled.

MODE6 — Input. If MODE 6 = 1, then minimum frame length of 96 bits is enforced. If MODE6 = 0, then no minimum frame length is enforced.

$\overline{RESET}$ — Schmitt input. Active low. A low causes the device to reset. Input must be high for normal operation.

$\overline{LEDEN}$ — Input/output open drain. If $\overline{LEDEN}$ is externally connected to GND, then the LED (0-3) provide static status information. Otherwise, $\overline{LEDEN}$ should be pulled high through a 2K ohm pullup resistor and LED (0-3) will provide an ID of an internal status monitoring point and will pull $\overline{LEDEN}$ low if that monitoring point is active. This allows connection of a single external multiplexer to drive indicating devices. Refer to Figure 4.

LED0-LED3 Output. If LEDEN is connected to GND:

LED0 UPLINK transmit enabled
LED1 UPLINK collision sense
LED2 DOWNLINK transmit enabled
LED3 DOWNLINK collision sense.

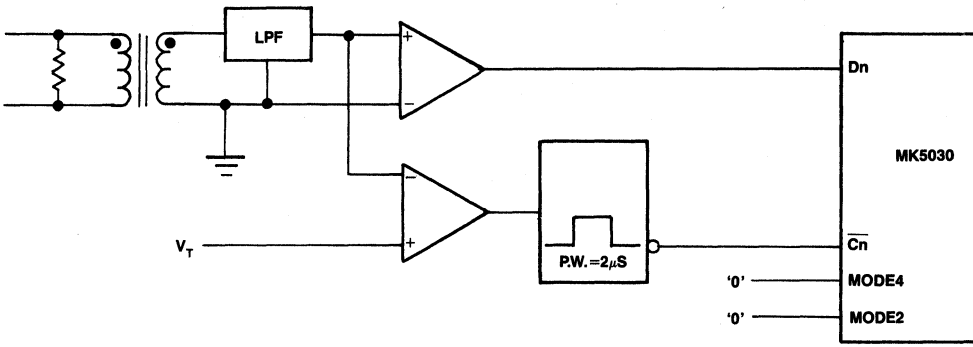
If $\overline{\text{LEDEN}}$ is not connected to GND, then $\overline{\text{LEDEN}}$ = 0 indicates that the LED (0-3) specified function is active:

LED3	LED2	LED1	LED0	DESCRIPTION	$\overline{\text{LEDEN}}$ = 0	$\overline{\text{LEDEN}}$ = 1
0	0	0	0	PORT 0 jabber	active	inactive
0	0	0	1	PORT 1 jabber	active	inactive
0	0	1	0	PORT 2 jabber	active	inactive
0	0	1	1	PORT 3 jabber	active	inactive
0	1	0	0	PORT 4 jabber	active	inactive
0	1	0	1	PORT 5 jabber	active	inactive
0	1	1	0	PORT 6 jabber	active	inactive
0	1	1	1	PORT 7 jabber	active	inactive
1	0	0	0	PORT 8 jabber	active	inactive
1	0	0	1	PORT 9 jabber	active	inactive
1	0	1	0	PORT 10 jabber	active	inactive
1	0	1	1	PORT 11 jabber	active	inactive
1	1	0	0	UPLINK	inactive	active
1	1	0	1	UPLINK collision	yes	no
1	1	1	0	DOWNLINK	inactive	active
1	1	1	1	DOWNLINK collision	yes	no

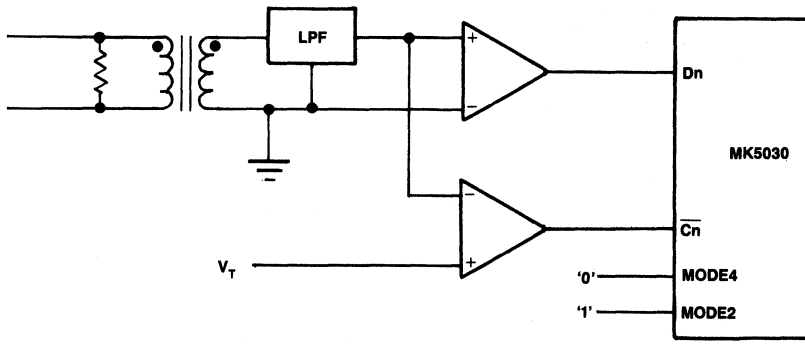
NOTE: 1. UPLINK and DOWNLINK status outputs are normally on and will blink off for 147mS when a frame is transmitted. LED on-time of 147mS is guaranteed between each off blink.
2. UPLINK and DOWLINK collision outputs are normally off and will blink on for 147 ms when a collision is detected. LED off time of 147 ms is guaranteed between each on blink.

VCC Power supply pin. +5 VDC ±5%

GND Ground. 0 VDC.

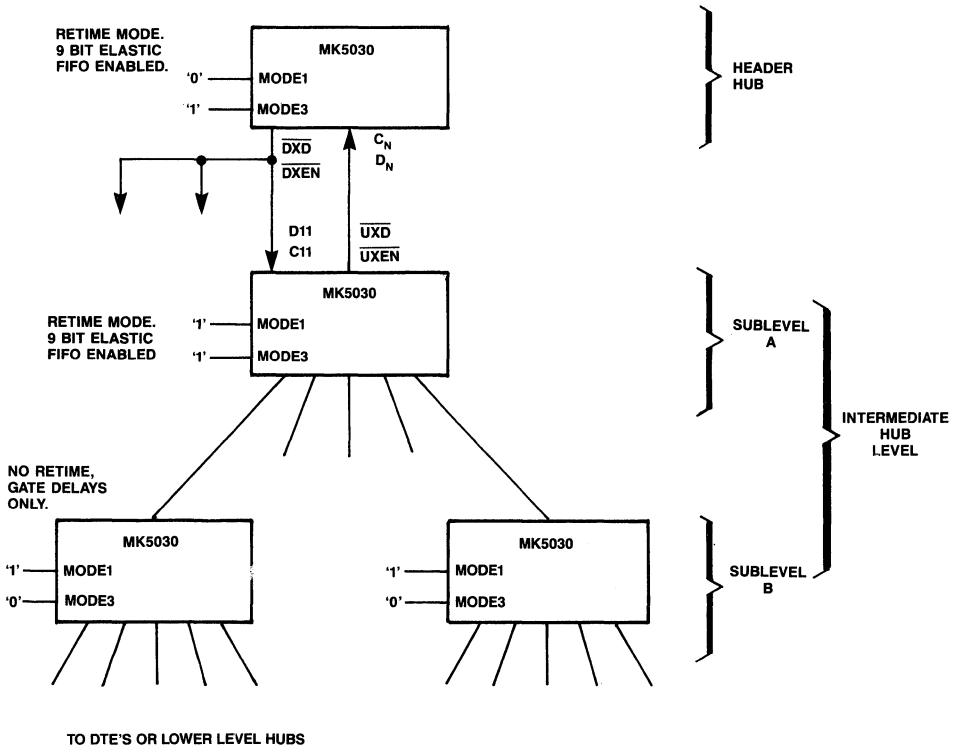


EXTERNAL SQUELCH



INTERNAL SQUELCH

Figure 2. Internal Versus External Time Squelch



NOTE: Sublevels A and B may either be on same circuit board or on separate boards located in close proximity.

Figure 3. Example Showing Retime and No-Retime Modes

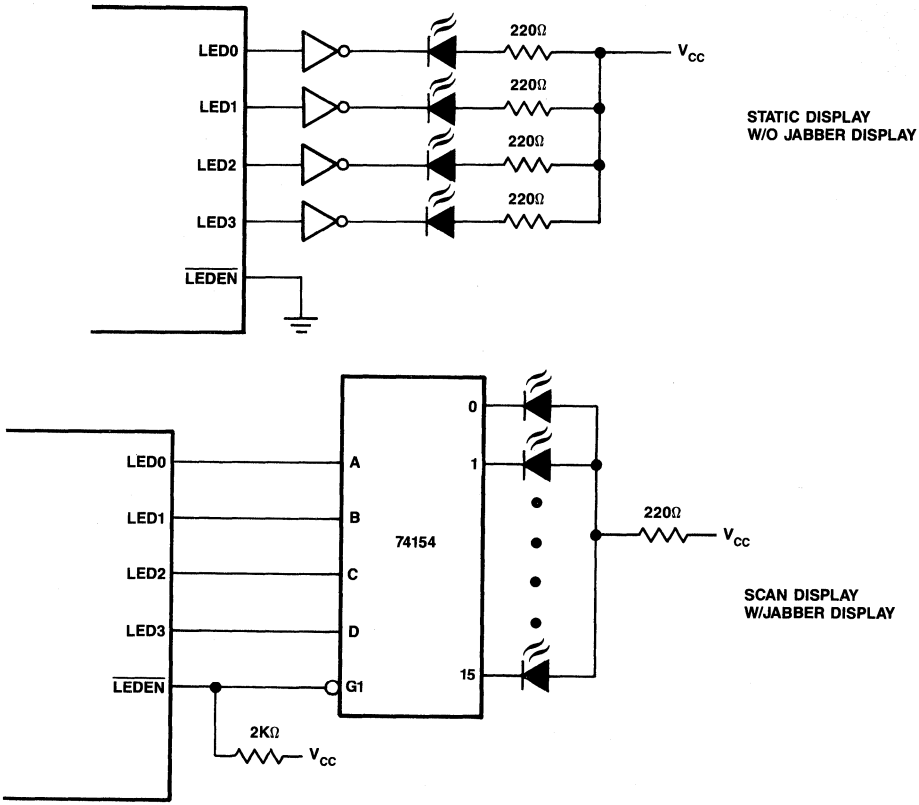


Figure 4. Status Display Modes

Overview of Circuit Description

The MK5030 HUB chip consists of three sub-modules: the uplink, the downlink, and the status display module.

The uplink module multiplexes twelve inputs from stations and/or "lower" HUBS (see Fig. 3) and retimes, if enabled, the multiplexed data to remove jitter. The uplink also handles several optional features including retiming, disabled auto-preamble generation, and collision detection/transmission. Refer to Figure 5, MK5030 HUB Block Diagram.

The downlink module is used only in the intermediate mode, and is nearly identical to the uplink (see Fig. 5).

The status display modules provide either static or scanned display of the line activity, detected collisions, and "jabbed" inputs.

The Uplink Module

The uplink module has a carrier processor which performs the following:

- Detects carrier and outputs a carrier presence signal.
- Detects collision and outputs a collision presence signal.
- Will ignore one, or more, inputs by the jabber or protection time functions.
- Provides time domain filtering to improve noise tolerance on carrier inputs.

- When in the retime mode:
  - — Automatically compensates for wiring reversal.
  - — Recovers clock using a DPLL (for internal HUB chip use only).
  - — Passes data through a serial 9 bit FIFO buffer.
  - — When in minimum frame length mode, the frame length is guaranteed to be greater than 96 bits.
  - — Will perform Automatic Preamble Generation (APG) if the optional APG is selected.
  - — Detects end-of-frame using the DPLL.
- When NOT in the retime mode, the DPLL, APG, and FIFO are bypassed, and the output is taken from the selected input without any flip-flop delays (gate delays only). Also, automatic compensation for wiring reversal is disabled when not in retime mode.

Carrier and Data Inputs

When an input has a signal present, the carrier will be detected on the appropriate pin (C0 - C11). The carrier input is user selected for either external squelch (with external one-shots) or internal squelch (a 2μS pulse stretcher is added by the HUB chip). MODE2 = 0 selects external squelch, and MODE2 = 1 selects internal.

Note, a carrier input must be active for at least three clock samples for it to be recognized by the chip. Any isolated pulse less than three clock samples wide will be ignored. However, when using internal carrier squelch, the carrier must be active for at least one clock sample time every 2μS to be considered valid beyond the initial carrier recognition. When not using internal squelch, the carrier must be active during the entire frame to avoid data loss. Ignoring carrier spikes provides extra noise protection and is also referred to as time domain filtering (TDF).

Retime Mode

The selected valid data input is fed to a digital phase locked loop (DPLL). The DPLL is implemented with a counter which clears on each transition. This gives a jitter tolerance of 162ns peak to peak (83ns peak). This is 40% more tolerance than required by the StarLAN specification.

The valid input is passed through a 9 bit FIFO. Output from the FIFO is prevented until the FIFO is 4 bits full. This is called the 4 bit watermark, and gives the FIFO 4 bits of elasticity which is more than sufficient to absorb the allowable 0.01% clock tolerance.

Automatic Preamble Generator

If APG is enabled, preamble generation at the outputs $\overline{DXD}$ and $\overline{UXD}$ is started as soon as the DPLL acquires lock. When the FIFO reaches the 4 bit watermark, the output data are taken from the FIFO. The APG keeps the preamble from "shrinking" as a frame is passed from HUB to HUB. Without APG, a HUB chip will lose an average of 2 preamble bits, but with APG, an average of 2 preamble bits are gained. This two bit gain should be taken into account by system designers.

Automatic Compensation For Wiring Reversal

When installing twisted pair telephone wiring, it is often difficult and expensive to maintain proper polarity on the wire pairs. The MK5030 will automatically compensate for this reversal on a per port basis. Any frame that is received with inverse polarity will be detected and will be transmitted on the $\overline{DXD}$ and $\overline{UXD}$ pins with the correct polarity. This polarity compensation is active only while in the retime mode (MODE3 = 1).

Minimum Frame Length Enforcement

When minimum frame length enforcement (FLE) is enabled (MODE6 = 1) and the MK5030 is in retime mode, the input carrier is assumed to be valid for at least 96 bit times. If either the incoming carrier goes inactive or EOF is detected prior to 96 bit times, the MK5030 will send collision presence (CP) for the remainder of the 96 bit times. This feature is important in multi-port environments where signal superposition may cause early carrier dropout. NOTE: IEEE standards committee is, at this printing, still defining FLE. The actual length guaranteed is subject to change.

No-Retime Mode

If the retime mode is disabled, then the DPLL, FIFO, and APG are bypassed. The outputs, $\overline{DXD}$ and $\overline{UXD}$, are taken from the selected input without clocked delays (i.e., flip-flops). There are gate delays only. End-of-frame is detected by a counter instead of the DPLL. The advantage of the no-retime mode is that two HUBs cascaded together will appear to the network as one. See Fig. 3. In no-retime mode, an average of 2 bits will be lost as outputs are enabled after the first rising edge of the incoming data.

Protection Time

At the end of each frame, all carrier inputs are ignored for 20μS. This is called the protection time and insures immunity to post end-of-frame spikes caused by transformer coupling.

Collision

A collision is defined when any one of the following five conditions exists: a. Multiple carrier inputs; b. Manchester code violations; c. FIFO underflow/overflow exception. d. PLL lock acquisition timeout; e. frame length violation. An IEEE defined collision presence (CP) code is placed on the $\overline{UXD}$ output. The starting point of the CP sequence is adjusted to allow faster CP detection by the remote station or HUB. The HUB chip is fully upward compatible with the existing AT&T release 1 CP signal. NOTE: b, c, and d are active collision sources only while in retime mode.

Jabber

If a station transmits data for greater than 27mS (which allows twice its normal maximum frame size) then the HUB will output a CP signal. This should correct the error in the station in most cases. However, if that station continues to transmit for up to a total time of 54mS, then the station is "jabbed". This means that the jabber function in the HUB chip will ignore that input and, in effect, remove the station from the network. If the "jabbed" station goes silent and then is the originator of new data, the station is allowed back onto the network by the HUB chip.

Thus, StarLAN networks automatically adjust as portions of the network fail and are repaired.

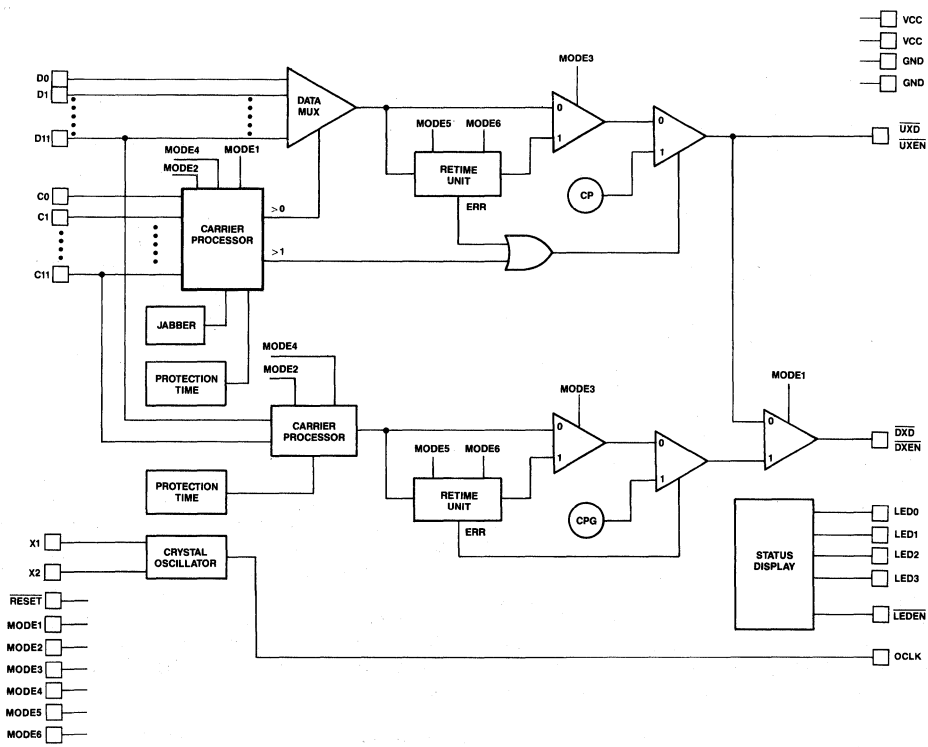


Figure 5. MK5030 HUB Block Diagram

The Downlink Module

The downlink is identical to the uplink except without the multiplexer, frame length enforcement, and jabber functions. In the intermediate mode (MODE1 = 1), port 11 is a downlink input connected to the next "higher" HUB downlink output. See Fig. 3. In the high-end mode (MODE1 = 0), all twelve ports feed the uplink, and $\overline{\text{DXD}}$-$\overline{\text{DXEN}}$ are internally connected to $\overline{\text{UXD}}$-$\overline{\text{UXEN}}$.

Status Display

Two display modes are supported: static and scan. When $\overline{\text{LEDEN}}$ is externally tied to GND, then LED0 - LED3 provide static status information. When $\overline{\text{LEDEN}}$ is externally tied to VCC through a pull-up resistor, then an external demultiplexer (such as a 74154) may be used to provide 16 lines of status information. See Figures 4 and 6, and also see the description of pins LED0 - LED3.

Oscillator

The MK5030 will accept two forms of clock input: a CMOS input or a crystal. If pin X2 is left unconnected, a 6.0MHz ± 0.01% CMOS clock may be applied to pin X1. Alternately, a crystal circuit may be connected between X1 and X2 to form the basis of an oscillator. Typically, a 6.0 ± 0.005% parallel resonant crystal is needed to insure the ± 0.01% frequency accuracy required for StarLAN. Refer to Figure 7. A fundamental mode, parallel resonance type crystal should be used with the manufacturer's suggested load capacitance.

OCLK provides a CMOS level clock output useful for cascading HUB chips or driving surrounding logic.

Reset Input

The reset pin is an active low Schmidt trigger input. A simple RC network may be used to insure correct operation upon power-up. Reset should be active for two clock cycles (334 nS) to insure proper operation. In addition, if the mode inputs are changed after the application of power, reset must be reapplied. If either MODE1 or MODE3 is changed, an internal reset is generated automatically. Refer to Fig. 8.

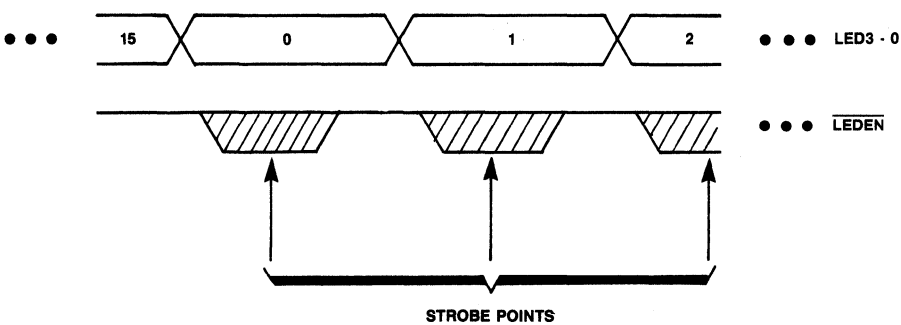


Figure 6. Scan Display Timing

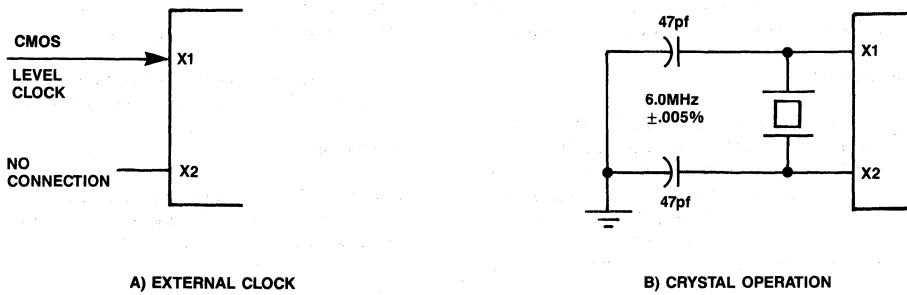


Figure 7. Oscillator Operation

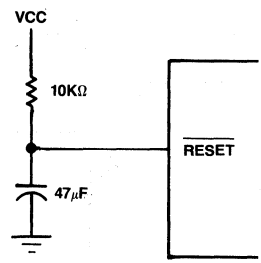


Figure 8. Typical RC Connection For Power-On Reset

System Performance Considerations Using the MK5030

The MK5030 has several modes of operation. This allows designers flexibility in their design. Figure 9 shows a typical circuit diagram.

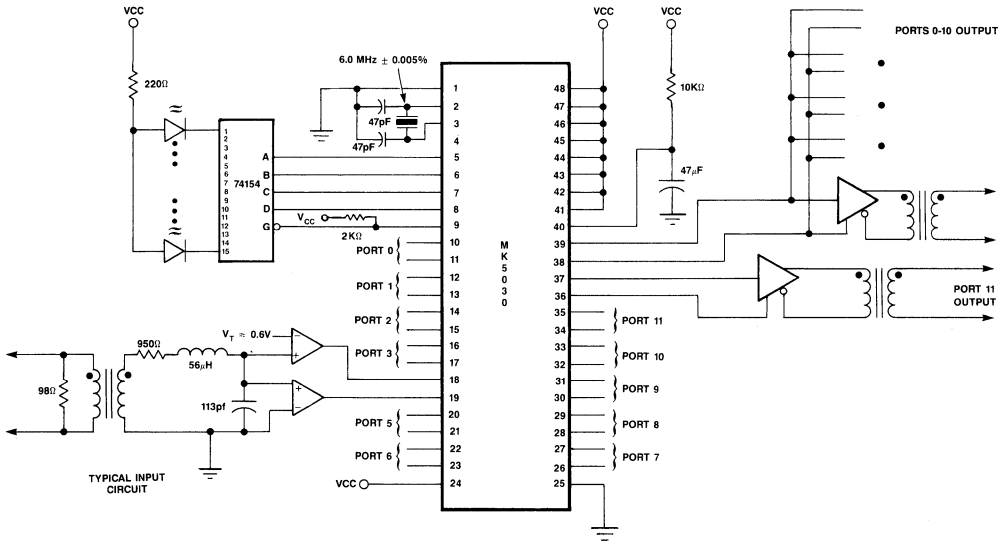


Figure 9. MK5030 External Component Diagram

ELECTRICAL SPECIFICATIONS

This chapter provides tabular presentations for Absolute Maximum Ratings, DC Characteristics, Capacitance, and AC Timing Specifications. In addition, illustrations are provided for an Output Load Diagram (Figure 14) and HUB Timing Diagrams.

ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias ..... −25°C to +100°C
Storage Temperature ..... −65°C to +150°C
Voltage on Any Pin with Respect to Ground ..... −0.5 V to V_{CC} +0.5 V
Power Dissipation (no load) 125mW

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = +5 V ±5% unless otherwise specified.

SYMBOL	CONDITIONS	MIN	MAX	UNITS
V_{IL}		−0.5	+0.8	V
V_{IH}	Except Pin X1	+2.0	V_{CC} +0.5	V
V_{IH}	Pin X1	+3.5	V_{CC} +0.5	V
V_{OL}	@ I_{OL} = 3.2 mA		+0.5	V
V_{OH}	@ I_{OH} = −0.4 mA	+2.4		V
I_{IL}	@ V_{IN} = 0.4 to V_{CC}		±10	μA
I_{CC}	@ T_{XI} = 6 MHz		25	mA

CAPACITANCE

F = 1 MHz

SYMBOL	CONDITIONS	MIN	MAX	UNITS
C_{IN}			10	pf
C_{OUT}			10	pf
C_{IO}			20	pf

AC TIMING SPECIFICATIONS

T_A = 0°C to 70°C, V_{CC} = +5 V ±5% unless otherwise specified, V_{TH} = 2.0 V, V_{TL} = 0.8 V.

#	SIGNAL	SYMBOL	PARAMETER	MIN ns	TYP ns	MAX ns
1	X_1	T_{XIT}	X1 period	160		
2	X_1	T_{XIL}	X1 low time	60		
3	X_1	T_{XIH}	X1 high time	60		
4	X_1	T_{XIR}	Rise time of X1	0		10
5	X_1	T_{XIF}	Fall time of X1	0		10

AC TIMING SPECIFICATIONS (cont.)

T_A = 0°C to 70°C, V_{CC} = +5 V ±5% unless otherwise specified.

#	SIGNAL	SYMBOL	PARAMETER	MIN ns	TYP ns	MAX ns
6	X2	T_{X2}	X2 delay from X1		30	
7	OCLK	T_{OCLK}	OCLK delay from X1			45
8	$\overline{UXD}$	$T_{\overline{UXD}}$	$\overline{UXD}$ delay from X1		45	65
9	$\overline{UXEN}$	$T_{\overline{UXEN}}$	$\overline{UXEN}$ delay from X1		48	75
10	$\overline{DXD}$	$T_{\overline{DXD}}$	$\overline{DXD}$ delay from X1		48	65
11	$\overline{DXEN}$	$T_{\overline{DXEN}}$	$\overline{DXEN}$ delay from X1		51	75
12	$\overline{UXD}$	J_{UXD}	Transmit jitter: $\lvert T_{\overline{UXD}}\uparrow - T_{\overline{UXD}}\downarrow \rvert \div 2$		2	4
13	$\overline{DXD}$	J_{DXD}	Transmit jitter: $\lvert T_{\overline{DXD}}\uparrow - T_{\overline{DXD}}\downarrow \rvert \div 2$		2	4
14	$C_{0\text{-}11}$	T_{CS}	$C_{0\text{-}11}$ Setup to X1	15		
15	$C_{0\text{-}11}$	T_{CH}	$C_{0\text{-}11}$ Hold from X1	15		
16	$D_{0\text{-}11}$	T_{DS}	$D_{0\text{-}11}$ Setup to X1	15		
17	$D_{0\text{-}11}$	T_{DH}	$D_{0\text{-}11}$ Hold from X1	15		
18	$D_{0\text{-}11}$	J_{DIN}	$D_{0\text{-}11}$ Incoming jitter tolerance			162
19	$\overline{UXD}$,$\overline{DXD}$	T_{PXD}	Delay from any D input		42	60
20	$\overline{UXD}$,$\overline{DXD}$	J_{NR}	No retime mode jitter: $\lvert T_{XD}\uparrow - T_{XD}\downarrow \rvert \div 2$		2	4
21	$LED_{0\text{-}3}$	T_{LED}	Delay from X1		50	
22	$\overline{LEDEN}$	T_{LEDENR}	Guaranteed release time until $LED_{0\text{-}3}$ change		2600	
23	$\overline{LEDEN}$	T_{LEDEN}	Delay from $LED_{0\text{-}3}$ transition		2660	

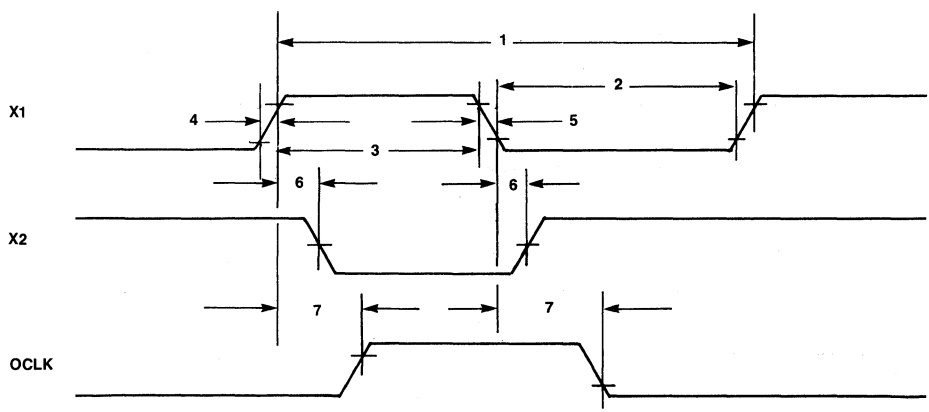


Figure 10. Oscillator Timing Diagram

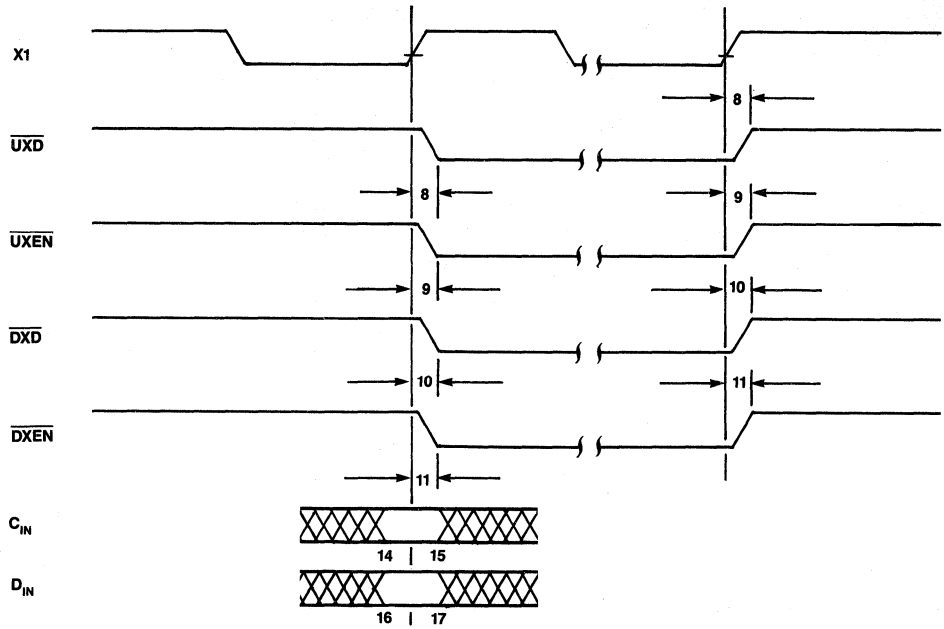


Figure 11. Retimer Enabled (MODE3 = 1) Timing Diagram

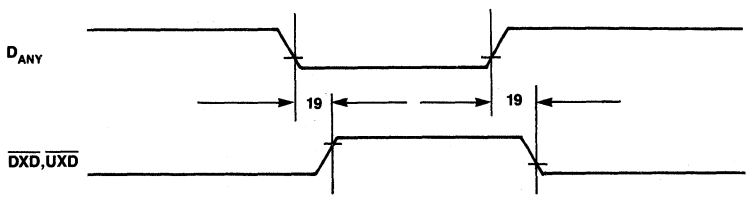


Figure 12. Retimer Disabled (MODE3 = 0) Timing Diagram

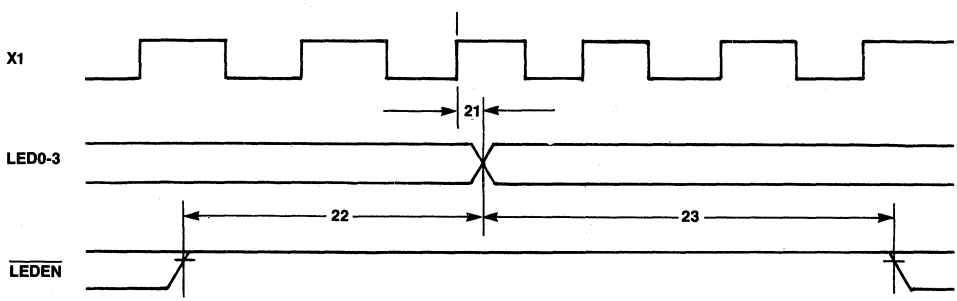


Figure 13. Status Display Timing Diagram

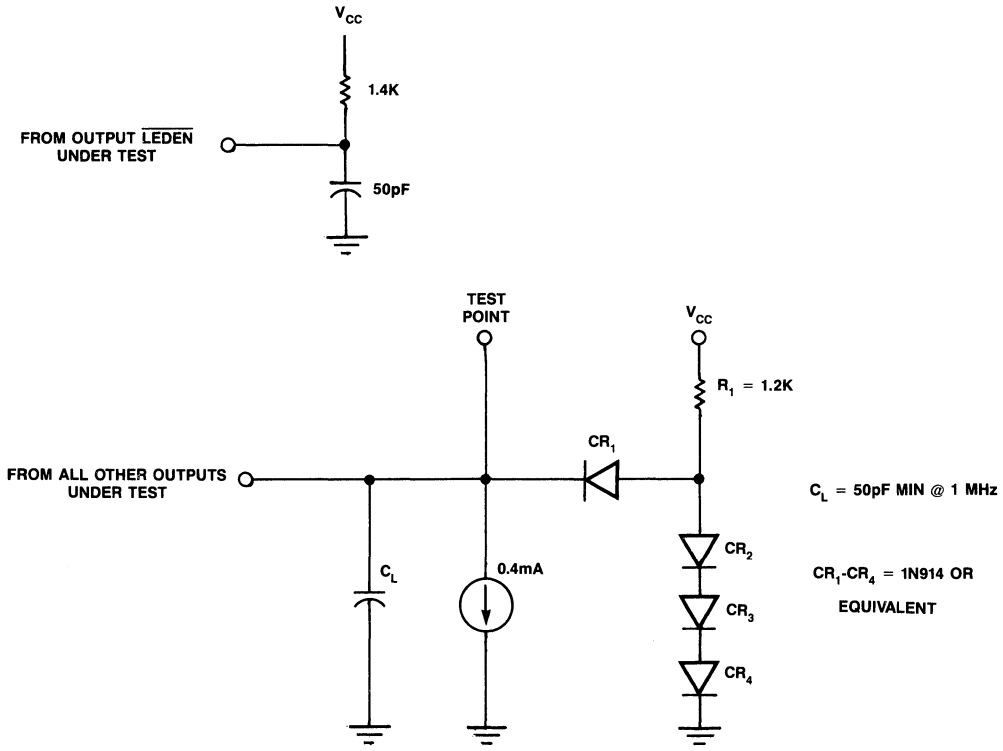


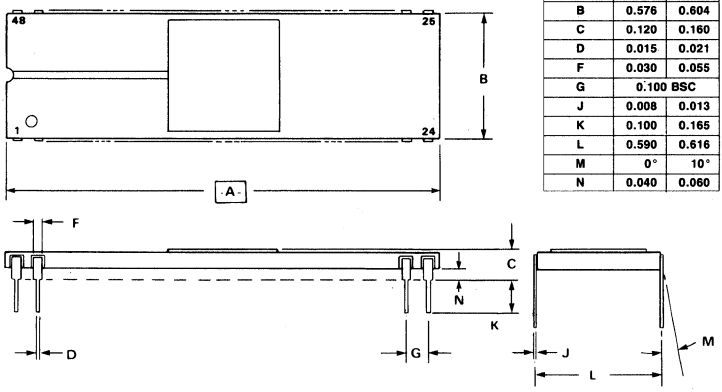
Figure 14. Output Load Diagram

GLOSSARY OF TERMS

automatic preamble generator (APG)	An optional circuit in the HUB chip which will begin preamble generation before the FIFO reaches the 4 bit watermark. The APG replaces a 2 bit loss in the preamble through a HUB with a 2 bit gain. See Retime Mode.
protection time	A 20μS period at the end of each frame where all carrier inputs are ignored. This protection insures immunity to post end-of-frame spikes caused by transformer coupling. See Protection Time.
downlink	The data path going from a "higher" HUB to the next "lower" HUB, or going from a HUB back to the stations.
high-end hub	A HUB that does not connect to another "higher" HUB. The downlink outputs, $\overline{DXD}$ and $\overline{DXEN}$, are internally connected to the uplink outputs, $\overline{UXD}$ and $\overline{UXEN}$.
intermediate hub	A HUB that connects to another "higher" HUB. Pins C11 and D11 must be used as downlink inputs.
jabber	A circuit module inside the HUB chip which protects the network from a station which is constantly transmitting. See Jabber.
uplink	The data path going from a "lower" HUB to the next "higher" HUB, or going from the stations to a HUB.

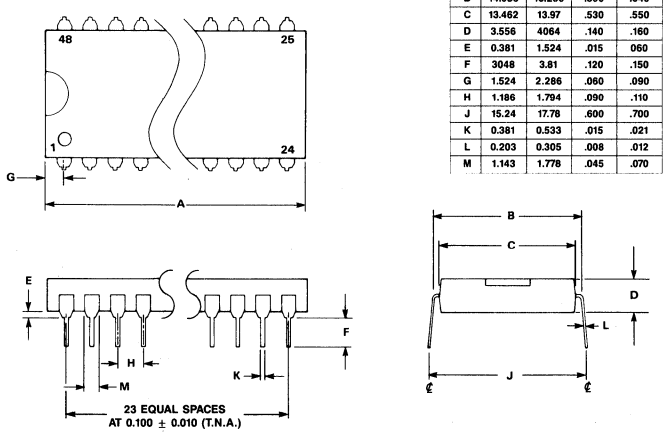
PACKAGE DESCRIPTION
48 Pin Ceramic
MK5030P

DIM.	INCHES	
	MIN	MAX
A	2.376	2.424
B	0.576	0.604
C	0.120	0.160
D	0.015	0.021
F	0.030	0.055
G	0.100 BSC	
J	0.008	0.013
K	0.100	0.165
L	0.590	0.616
M	0°	10°
N	0.040	0.060



PACKAGE DESCRIPTION
48 Pin Plastic
MK5030N

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	61.468	62.738	2.420	2.470
B	14.986	16.256	.590	.640
C	13.462	13.97	.530	.550
D	3.556	4064	.140	.160
E	0.381	1.524	.015	060
F	3048	3.81	.120	.150
G	1.524	2.286	.060	.090
H	1.186	1.794	.090	.110
J	15.24	17.78	.600	.700
K	0.381	0.533	.015	.021
L	0.203	0.305	.008	.012
M	1.143	1.778	.045	.070



FEATURES

- ☐ Identical pinout to MK68590 Ethernet Controller
- ☐ Supports LAN Standards: IEEE 802.3, Ethernet, Cheapernet, and StarLAN
- ☐ Supports data rates from 1 to 10 Mbps
- ☐ Supports system clocks from 1 to 10 MHz.
- ☐ On-chip DMA with buffer management using circular queues.
- ☐ Complete CSMA/CD data link controller (MAC).
- ☐ Preamble insertion and checking.
- ☐ CRC insertion and stripping.
- ☐ General purpose bus interface compatible with 8086 and 68000 buses.
- ☐ Cable fault detection.
- ☐ 48 pin DIP. +5V only. All inputs/outputs TTL compatible.
- ☐ Compatible with MK5033, MK5034, MK50351, and MK50361 Encoder/Decoder and with MK68591/2 Serial Interface Adaptor.

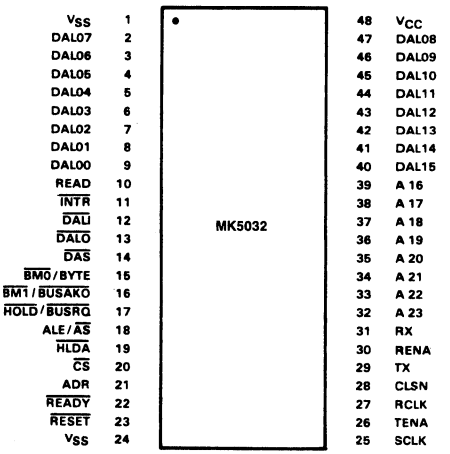


Figure 1. MK5032 Pin Assignment

DESCRIPTION

The 5032 Variable Bit-Rate LANCE is a 48-pin VLSI device that simplifies the interfacing of a microcomputer or a minicomputer to an IEEE 802.3 Local Area Network.

PIN DESCRIPTION

DAL00-DAL15
(Data/Address Bus)
Input/Output Three State. The time multiplexed Address/Data bus. These lines will be driven as a bus master and as a bus slave.

READ
Input/Output Three State. Indicates the type of operation to be performed in the current bus cycle. When it is a bus master, MK5032 drives this signal.

MK5032 as bus slave:
High - The chip places data on the DAL lines.
Low - The chip takes data off the DAL lines.
MK5032 as bus master:
High - The chip takes data off the DAL lines.
Low - The chip places data on the DAL lines.

$\overline{\text{INTR}}$
(Interrupt)
Output Open Drain. When enabled, an attention signal that indicates the occurrence of one or more of the following events: a message reception or transmission has completed or an error has occurred during the transaction; the initialization procedure has completed; or a memory error has been encountered. Setting INEA in CSR0 (bit 06) enables $\overline{\text{INTR}}$.

LANCE stands for Local Area Network Controller for Ethernet.
LANCE is a trademark of Thomson Components - Mostek Corporation

DALI
(Data/Address Line In)
Output Three State. An external bus transceiver control line. When MK5032 is a bus master and reads from the DAL lines, $\overline{DALI}$ is asserted during the data portion of the transfer.

$\overline{DALO}$
(Data/Address Line Out)
Output Three State. An external bus transceiver control line. When MK5032 is a bus master and drives the DAL lines, $\overline{DALO}$ is asserted during the address portion of a read transfer or for the duration of a write transfer.

$\overline{DAS}$
(Data/Strobe)
Input/Output Three State. Defines the data portion of the bus transaction. DAS is driven only as a bus master.

$\overline{BM0}$, $\overline{BM1}$ or BYTE, $\overline{BUSAKO}$
(Byte Mask)
Output Three State. Pins 15 and 16 are programmable through bit (00) of CSR3 (known as BCON). Asserting $\overline{RESET}$ clears CSR3.

CSR3(00) BCON = 0
PIN 16 = $\overline{BM1}$ (Output Three State)
PIN 15 = $\overline{BM0}$ (Output Three State)

BM0, BM1 Byte Mask. Indicates the byte(s) of a bus transaction to be read or written. The BM lines are ignored as a bus slave and assume word transfers only. The MK5032 drives the BM lines only when it is a bus master. Byte selection occurs as follows:

$\overline{BM1}$	$\overline{BM0}$	
Low	Low	Whole Word
Low	High	Byte of DAL 08 - DAL 15
High	Low	Byte of DAL 00 - DAL 07
High	High	None

CSR3(00) BCON = 1
PIN 16 = $\overline{BUSAKO}$ (Output)
PIN 15 = BYTE (Output Three State)

BYTE. An alternate byte selection line. Byte selection occurs when the BYTE and DAL (00) lines are latched during the address portion of the bus transaction. BYTE, $\overline{BM0}$ and $\overline{BM1}$ are ignored when MK5032 is a bus slave. There are two modes of ordering bytes depending on bit (02) of CSR3, (known as BSWP). This programmable ordering of upper and lower bytes when using BYTE and DAL (00) as selection signals is required to make the ordering compatible with various 16-bit microprocessors.

BSWP = 0		BSWP = 1		
BYTE	DAL(00)	BYTE	DAL(00)	
Low	Low	Low	Low	Whole Word
Low	High	Low	High	Illegal Condition
High	High	High	Low	Upper Byte
High	Low	High	High	Lower Byte

$\overline{BUSAKO}$. The DMA daisy chain output.

$\overline{HOLD}$/$\overline{BUSRQ}$
(Bus Hold Request)
Input/Output Open Drain. MK5032 asserts this signal when it requires access to memory. $\overline{HOLD}$ is held low for the entire bus transaction. This bit is programmable through bit (00) of CSR3 (known as BCON). In the daisy chain DMA mode (BCON = 1) $\overline{BUSRQ}$ is asserted only if $\overline{BUSRQ}$ is inactive prior to assertion. Bit (00) of CSR3 is cleared when $\overline{RESET}$ is asserted.

CSR3(00) BCON = 0
PIN 17 = $\overline{HOLD}$ (Output Open Drain)
CSR3(00) BCON = 1
PIN 17 = $\overline{BUSRQ}$ (Output Open Drain)
$\overline{BUSRQ}$ will be asserted only if PIN 17 is high prior to assertion.

ALE/$\overline{AS}$
(Address Latch Enable)
Output Three State. Used to demultiplex the DAL lines and define the address portion of the bus cycle. This pin is programmable through bit (01) of CSR3. As ALE, the signal transitions from high to low at the end of the address portion of the bus the address portion of the bus transaction and remains low during the entire data portion of the transaction. As $\overline{AS}$, the signal transitions from low to high at the end of the address portion of the bus transaction and remains high throughout the entire data portion of the transaction. The MK5032 drives the ALE/$\overline{AS}$ line only as a bus master.

CSR3(01) ACON = 0
PIN 18 = ALE
CSR3(01) ACON = 1
PIN 18 = $\overline{AS}$

$\overline{HLDA}$
(Bus Hold Acknowledge)
Input. A response to $\overline{HOLD}$ indicating that the MK5032 is the Bus Master. $\overline{HLDA}$ stops its response when $\overline{HOLD}$ ends its assertion.

$\overline{CS}$
(Chip Select)
Input. When asserted, $\overline{CS}$ indicates MK5032 is the slave device of the data transfer. $\overline{CS}$ must be valid throughout the data portion of the bus cycle.

ADR
(Register Address Port Select)
Input. When $\overline{CS}$ is asserted, ADR indicates which of the two register ports is selected. ADR must be valid throughout the data portion of the bus cycle.

ADR	PORT
Low	Register $\overline{Data}$ Port
High	Register Address Port

$\overline{READY}$
Input/Output Open Drain. When the MK5032 is a bus master, $\overline{READY}$ is an asynchronous acknowledgement from external memory that will complete the data transfer. As a bus slave, the chip asserts $\overline{READY}$ when it has put data on the bus, or is about to take data off the bus. $\overline{READY}$ is a response to $\overline{DAS}$. $\overline{READY}$ negates after $\overline{DAS}$ negates. Note: If $\overline{DAS}$ or $\overline{CS}$ deassert prior to the assertion of $\overline{READY}$, $\overline{READY}$ cannot assert.

$\overline{RESET}$
Input. Bus reset signal. Causes MK5032 to cease operation and to enter an idle state.

SCLK
(System Clock)
Input. A clock from 1 to 10 MHz.

TENA
(Transmit Enable)
Output. Transmit Output Stream Enable. A level asserted with the transmit output bit stream, TX, to enable the external transmit logic.

RCLK
(Receive Clock)
Input. Normally a 6 square wave synchronized to the receive data and present only while receiving an input bit stream.

CLSN
(Collision)
Input. A logical input that indicates that a collision is occurring on the channel.

TX
(Transmit)
Output. Transmit output bit stream. This pin is programmable through bit (07) of the MODE REGISTER (MAN). When this bit is a "zero" the output data stream will be NRZ. When MAN is set to a "one", the data will be Manchester Encoded starting at a zero level and ending at the end of packet in a marking condition. (Continuous one level.) This mode will function only when the data rate is programmed less than the rate of SCLK.

Three other bits in the MODE register provide a data rate divison of 1, 2, 4, 6, 8, or 10. This means that the data rate of TX will be a division of SCLK. For more details on the MODE register, see the technical manual.

RENA
(Receive Enable)
Input. A logical input that indicates the presence of data on the channel.

RX
(Receive)
Input. Receive input bit stream.

A16-A23
(High-Order Address Bus)
Output Three State. The additional address bits necessary to extend the DAL lines to produce a 24-bit address. These lines will be driven only as a bus master.

VCC
Power supply pin. +5 VDC ±5 percent.

Filtering: A power supply filter is recommended at the MK5032 between V_{CC} (48) and V_{SS} (1, 24). This filter consists of two capacitors in parallel having the values of 10 μf and .047 μf respectively.

VSS
Ground. 0 VDC.

FUNCTIONAL CAPABILITIES

The MK5032 interfaces to a microprocessor bus characterized by time-multiplexed address and data lines. Typically, data transfers are 16 bits wide but byte transfers occur if the buffer memory address boundaries are odd. The address bus is 24 bits wide.

The IEEE 802.3 packet format consists of 64-bit preamble, a 48-bit destination address, a 48-bit source address, a 16-bit type field, and from a 46 to 1500 byte data field terminated with a 32-bit CRC. The packets' variable widths accommodate both short-status command and terminal traffic packets and long data packets to printers and disks (1024-byte disk sectors, for example). Packets are spaced a minimum of 96 bit times apart to allow one node enough time to receive back-to-back packets.

The MK5032 operates in a minimal configuration that requires close coupling between local memory and a processor. The local memory provides packet buffering for the chip and serves as a communication link between chip and processor. During initialization, the control processor loads the starting address of the initialization block plus the operating mode of the chip via two ports that can access four control registers into MK5032. The host processor talks directly to MK5032 only during this initial phase. All further communications are handled via a Direct Memory Access (DMA) machine under microword control contained within MK5032. Figure 2 shows a block diagram of the MK5032 and PLS (MK68951, MK50351, MK50361, or MK5033) device used to create an IEEE 802.3 interface for a computer system.

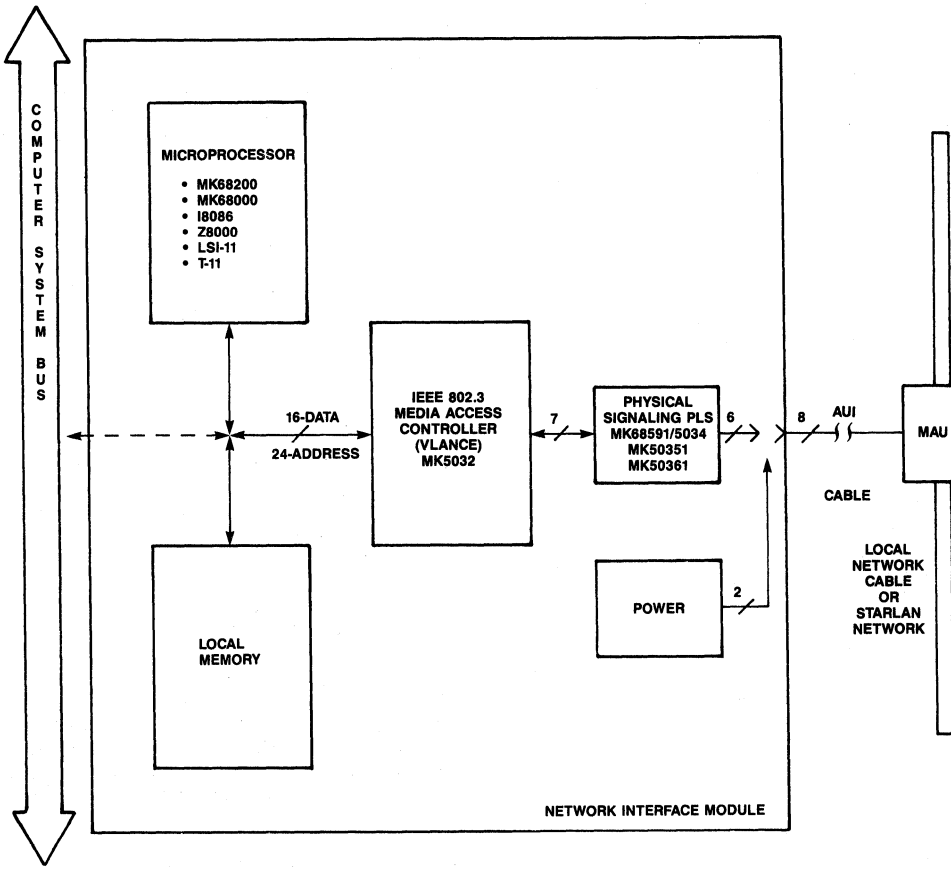


Figure 2. Ethernet Local Area Network System Block Diagram

FUNCTIONAL DESCRIPTION

SERIAL DATA HANDLING

MK5032 provides the IEEE 802.3 interface as follows. In the transmit mode (since there is only one transmission path, IEEE 802.3 is a half duplex system), the MK5032 reads data from a transmit buffer by using DMA and appends the preamble, sync pattern (two ones after alternating ones and zeros in the preamble), and calculates and appends the complement of the 32-bit CRC. In the receive mode, the destination address, source address, type, data, and CRC fields are transferred to memory via DMA cycles. The CRC is calculated as data and transmitted CRC is received. At the end of the packet, if this calculated CRC does not agree with a constant, an error bit is set in RDM1 of the receiver descriptor ring. In the receive mode, MK5032 accepts packets under four modes of operation. The first mode is a full comparison of the 48-bit destination address in the packet with the node address that was programmed into the MK5032 during an initialization cycle. There are two types of logical addresses. One is a group type mask where the 48-bit address in the packet is put through a hash filter in order to map the 48-bit physical addresses into 1 of 64 logical groups. This mode can be useful if simultaneously sending packets to all of one type of a device on the network. (i.e., send a packet to all file servers or all printer servers). The second logical address is a multicast address where all nodes on the network receive the packet. The last receive mode of operation is the so called "promiscuous mode" in which a node will accept all packets on the cable regardless of their destination address.

COLLISION DETECTION AND IMPLEMENTATION

The IEEE 802.3 CSMA/CD network access algorithm is implemented completely within MK5032. In addition to listening for a clear network cable before transmitting, IEEE 802.3 handles collisions in a predetermined way. Should two transmitters attempt to seize the network cable at the same time, they will collide, and the data on the network cable will be garbled. MK5032 is constantly monitoring the Collision (CLSN) pin. This signal is generated by the MAU when the signal level on the network cable indicates the presence of signals from two or more transmitters. If MK5032 is transmitting when CLSN is asserted, it will continue to transmit the preamble (collisions normally occur while the preamble is being transmitted), then will "jam" the network for 32 bit times. This jamming ensures that all nodes have enough time to detect the collision. The transmitting nodes then delay a random amount of time according to the "truncated binary backoff" algorithm defined in the IEEE 802.3 specification to minimize the probability of the colliding nodes having multiple collisions with each other. After 16 abortive attempts to transmit a packet, MK5032 will report a RTRY error due to excessive collisions and step over the transmitter buffer. During reception, the detection of a collision causes that reception to be aborted. Depending on when the collision occurred, MK5032 will treat this packet as an error packet if the packet has an address mismatch, as a runt packet (a packet that has less than 64 bytes), or as a legal length packet with a CRC error.

Fatal error reporting is provided by the MK5032 through a microprocessor interrupt and error flags in CSR0. These error conditions are collision error (the failure of the MAU to send a signal-quality-error message at the conclusion of a normal transmission), transmitter ON longer than 1518 bytes, a missed packet, and a memory error (failure of a memory transaction to complete within 256 sys clocks).

Additional errors are reported through bits in the descriptor rings (on a buffer by buffer basis). Receive error conditions include framing, CRC and buffer errors, and overflow. Transmit descriptor rings have error bits indicating buffer, underflow, late collision, and loss of carrier. Additionally, transmit descriptor rings have a bit indicating that the transmitter has unsuccessfully tried to transmit over a busy communication link.

Transmit descriptor rings also have ten bits reserved for a Time Domain Reflectometry counter (TDR). On the occurrance of a collision, the value in the TDR will give the number of system clocks until the collision, which can be used to determine the distance to the fault.

BUFFER MANAGEMENT

A key feature of the MK5032 and its DMA channel is the flexibility and speed of communication between the MK5032 and the host microprocessor through common memory locations. The basic organization of the buffer management is a circular queue of tasks in memory called descriptor rings, as shown in Figure 3. These rings control both transmit and receive operations. Up to 128 tasks may be queued on a descriptor ring for execution by the MK5032. Each entry in a descriptor ring holds a pointer to a data memory buffer and an entry for the data buffer length. Data buffers can be chained or cascaded to handle a long packet in multiple data buffer areas. The MK5032 searches the descriptor rings to determine the next empty buffer. This enables it to chain buffers together or to handle back-to-back packets. As each buffer is filled, an "own" bit is reset, signaling the host processor to empty this buffer.

MICROPROCESSOR INTERFACE

The parallel interface of MK5032 has been designed to be "friendly", or easy to interface, to many popular 16-bit microprocessors. These microprocessors include the MK68000, Z8000, 8086, LSI-11, T-11, and MK68200 (the MK68200 is a 16-bit single chip microcomputer produced by Mostek, the architecture of which is modeled after the MK68000). MK5032 has a wide 24-bit linear address space when in the Bus Master Mode,

allowing it to DMA the entire address space of the above microprocessors. MK5032 uses no segmentation or paging methods. As such, MK5032 addressing is closest to MK68000 addressing, but is compatible with the other microprocessors. When MK5032 is a bus master, a programmable mode of operation allows byte addressing, either by employing a Byte/Word control signal (much like that used on the 8086 or the Z8000) or by using an Upper Data Strobe/Lower Data Strobe much like that used on the MK68000, LSI-11 and MK68200 microprocessors. A programmable polarity on the Address Strobe signal eliminates the need for external logic. MK5032 interfaces with multiplexed and demultiplexed data busses and features control signals for address/data bus transceivers.

After the initialization routine, packet reception or transmission, transmitter timeout error, a missed packet, or memory error, the MK5032 generates an interrupt to the host microprocessor.

The cause of the interrupt is ascertained by reading CSR0. Bit (06) of CSR0, INEA, enables or disables interrupts to the microprocessor. In the polling mode, BIT (07) of CSR0 is sampled to determine if an interrupt causing condition has occurred.

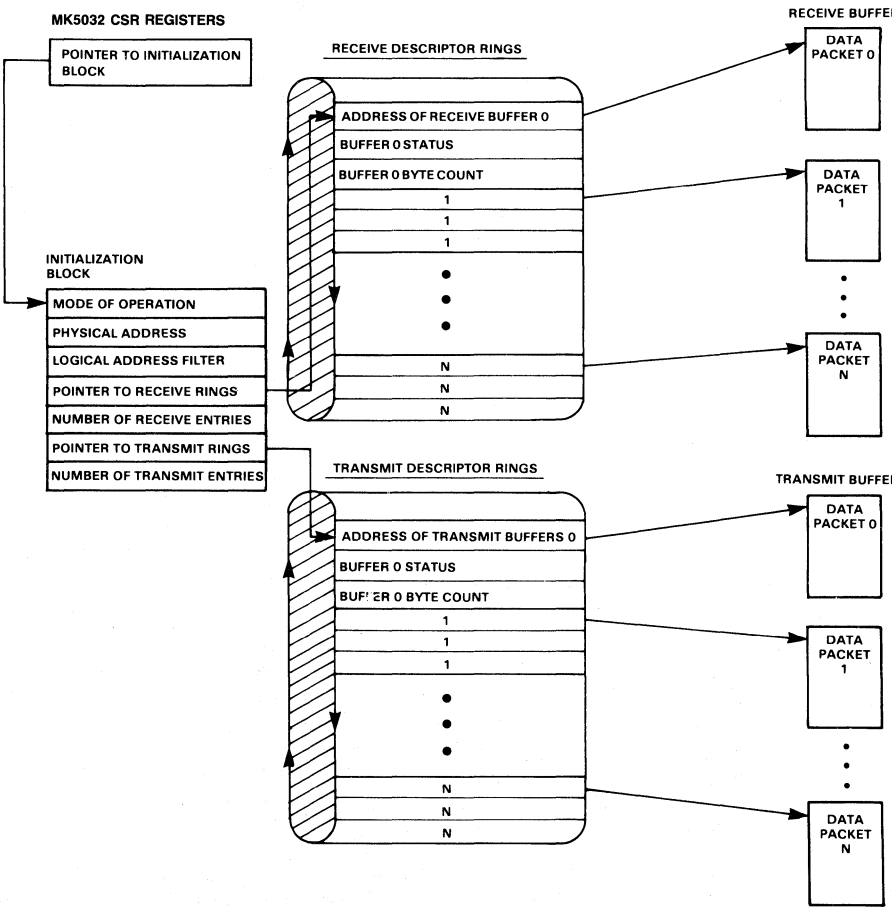


Figure 3. MK5032 Memory Management

MK5032 INTERFACE DESCRIPTION

ALE, $\overline{DAS}$ and $\overline{READY}$ time all data transfers from the MK5032 in the Bus Master mode. The automatic adjustment of the MK5032 cycle by the $\overline{READY}$ signal allows synchronization with variable cycle time memory due either to memory refresh or to dual port access. Bus cycles are a minimum of 600 ns long and can be increased in 100 ns increments.

READ SEQUENCE

At the beginning of a read cycle, valid addresses are placed on DAL00-DAL15 and A16-A21. The BYTE Mask signals ($\overline{BM0}$ and $\overline{BM1}$) become valid at the beginning of this cycle as does READ, indicating the type of cycle. The trailing edge of ALE or $\overline{AS}$ strobes the addresses A0-A15 into the external latches. Approximately 100 ns later, DAL00-DAL15 go into a three state mode. There is a 50 ns delay to allow for transceiver turnaround, then DAS falls low to signal the beginning of the data portion of the cycle. At this point in the cycle, the MK5032 stalls waiting for the memory device to assert $\overline{READY}$. Upon assertion of $\overline{READY}$, $\overline{DAS}$ makes a transition from a zero to a one, latching memory data. ($\overline{DAS}$ is low for a minimum of 200 ns).

The bus transceiver controls, $\overline{DALI}$ and $\overline{DALO}$, control the bus transceivers. DALI signals to strobe data toward the MK5032 and DALO signals to strobe data or addresses away from the MK5032. During a read cycle, $\overline{DALO}$ goes inactive before $\overline{DALI}$ goes active to avoid "spiking" of bus transceivers.

WRITE SEQUENCE

The write cycle begins exactly like a read cycle with the READ line remaining inactive. After ALE or $\overline{AS}$ pulse, the DAL00-DAL15 change from addresses to data. $\overline{DAS}$ goes active when the DAL00-DAL15 are stable. This data remains valid on the bus until the memory device asserts $\overline{READY}$. At this point, $\overline{DAS}$ goes inactive, latching data into the memory device. Data is held for 75 ns after the negation of $\overline{DAS}$.

MK5032 INTERFACE DESCRIPTION — BUS SLAVE MODE

The MK5032 enters the Bus Slave Mode whenever $\overline{CS}$ becomes active. This mode must be entered whenever writing or reading the four status control registers (CSR0, CSR1, CSR2, and CSR3) and the register address pointer (RAP). RAP and CSR0 may be read or written to at any time, but the MK5032 must be stopped (CSR0 bit 02) when CSR1, CSR2, or CSR3 is to be written to or read.

MK5032 ELECTRICAL SPECIFICATION

ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias ..... −25°C to +125°C
Storage Temperature ..... −65°C to +150°C
Voltage on Any Pin with Respect to Ground ..... −0.3 V to +7 V
Power Dissipation ..... 2.0 W

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

T_A=0°C to 70°C, V_{CC} = +5 V ±5 percent unless otherwise specified.

SYMBOL	PARAMETER	MIN	MAX	UNITS
V_{IL}		−0.5	+0.8	V
V_{IH}		+2.0	V_{CC} +0.5	V
V_{OL}	@ I_{OL} = 3.2 mA		+0.5	V
V_{OH}	@ I_{OH} = −0.4 mA	+2.4		V
I_{IL}	@ V_{in} = 0.4 to V_{CC}		±10	μA

CAPACITANCE

F=1 MHz

SYMBOL	PARAMETER	MIN	MAX	UNITS
C_{IN}			10	pf
C_{OUT}			10	pf
C_{IO}			20	pf

AC TIMING SPECIFICATIONS

T_A = 0°C to 70°C, V_{CC} = +5 V ±5 percent, unless otherwise specified.

NO.	SIGNAL	SYMBOL	PARAMETER	TEST CONDITIONS	MIN (ns)	TYP (ns)	MAX (ns)
1	SCLK	T_{SCT}	SCLK period		99		101
2	SCLK	T_{SCL}	SCLK low time		45		55
3	SCLK	T_{SCH}	SCLK high time		45		55
4	SCLK	T_{SCR}	Rise time of SCLK		0		8
5	SCLK	T_{SCF}	Fall time of SCLK		0		8
6	TENA	T_{TEP}	TENA propagation delay after the rising edge of SCLK	CL = 50 pf			75
7	TENA	T_{TEH}	TENA hold time after the rising edge of SCLK	CL = 50 pf	5		

AC TIMING SPECIFICATIONS (Continued)

T_A = 0°C to 70°C, V_{CC} = +5 V ±5 percent, unless otherwise specified.

NO.	SIGNAL	SYMBOL	PARAMETER	TEST CONDITIONS	MIN (ns)	TYP (ns)	MAX (ns)
8	TX	T_{TDP}	TX data propagation delay after the rising edge of SCLK (See Note 1)	CL=50 pf			75
8A	TX	T_{TDTT}	TX Transition - Transition (See Note 2)	CL=50 pF	B_t−7		B_t+7
9	TX	T_{TDH}	TX data hold time after the rising edge of SCLK (See Note 1)	CL=50 pf	5		
10	RCLK	T_{RCT}	RCLK period		85		118
11	RCLK	T_{RCH}	RCLK high time		38		
12	RCLK	T_{RCL}	RCLK low time		38		
13	RCLK	T_{RCR}	Rise time of RCLK		0		8
14	RCLK	T_{RCF}	Fall time of RCLK		0		8
15	RX	T_{RDR}	RX data rise time		0		8
16	RX	T_{RDF}	RX data fall time		0		8
17	RX	T_{RDH}	RX data hold time (RCLK to RX data change)		5		
18	RX	T_{RDS} (See Note 3)	RX data setup time (RX data stable to the rising edge of RCLK)		See Note 3		
19	RENA	T_{DPL}	RENA low time		120		
20	RENA	T_{RENH}	RENA hold time after rising edge of RCLK		40		
21	CLSN	T_{CPH}	CLSN high time		80		
22	A/DAL	T_{DOFF}	Bus master driver disable after rising edge of $\overline{HOLD}$		0		50
23	A/DAL	T_{DON}	Bus master driver enable after falling edge of $\overline{HLDA}$		0		150
24	$\overline{HLDA}$	T_{HHA}	Delay to falling edge of $\overline{HLDA}$ from falling edge of $\overline{HOLD}$ (bus master)		0		
25	$\overline{RESET}$	T_{RW}	$\overline{RESET}$pulse width low		200		
26	A/DAL	T_{CYCLE}	Read/write, address/data cycle time		600		
27	A	T_{XAS}	Address setup time to the falling edge of ALE		75		
28	A	T_{XAH}	Address hold time after the rising edge of $\overline{DAS}$		35		
29	DAL	T_{AS}	Address setup time to the falling edge of ALE		75		
30	DAL	T_{AH}	Address hold time after the falling edge of ALE		35		
31	DAL	T_{RDAS}	Data setup time to the rising edge of $\overline{DAS}$ (bus master read)		50		

NOTE: 1. This timing is for the NRZ mode only.
2. B_t = Bit time. This measurement is during preamble; valid for Manchester Mode only.
3. $T_{RDS\ (min)} = T_{RCT} - 25$ ns. Therefore, T_{RCT} = 100 ns when $T_{RDS\ (min)}$ = 75 ns.

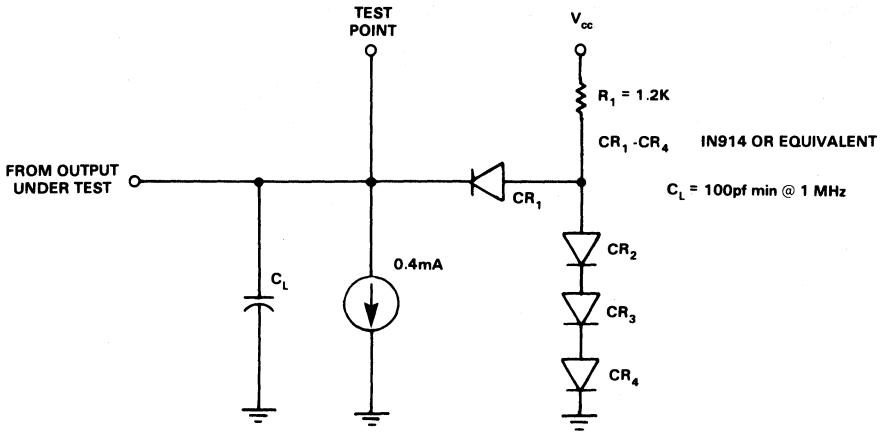
AC TIMING SPECIFICATIONS (Continued)

T_A = 0°C to 70°C, V_{CC} = +5 V ±5 percent, unless otherwise specified.

NO.	SIGNAL	SYMBOL	PARAMETER	TEST CONDITIONS	MIN (ns)	TYP (ns)	MAX (ns)
32	DAL	T_{RDAH}	Data hold time after the rising edge of $\overline{DAS}$ (bus master read)		0		
33	DAL	T_{DDAS}	Data setup time to the falling edge of $\overline{DAS}$ (bus master write)		0		
34	DAL	T_{WDS}	Data setup time to the rising edge of $\overline{DAS}$ (bus master write)		200		
35	DAL	T_{WDH}	Data hold time after the rising edge of $\overline{DAS}$ (bus master write)		35		
36	DAL	T_{SDO1}	Data driver delay after the falling edge of $\overline{DAS}$ (bus slave read)	(CSR 0,3, RAP)		400	
37	DAL	T_{SDO2}	Data driver delay after the falling edge of $\overline{DAS}$ (bus slave read)	(CSR 1,2)		1200	
38	DAL	T_{SRDH}	Data hold time after the rising edge of $\overline{DAS}$ (bus slave read)		0		35
39	DAL	T_{SWDH}	Data hold time after the rising edge of $\overline{DAS}$ (bus slave write)		0		
40	DAL	T_{SWDS}	Data setup time to the falling edge of $\overline{DAS}$ (bus slave write)		0		
41	ALE	T_{ALEW}	ALE width high		120		150
42	ALE	T_{DALE}	Delay from rising edge of $\overline{DAS}$ to the rising edge of ALE		70		
43	$\overline{DAS}$	T_{DSW}	$\overline{DAS}$ width low		200		
44	$\overline{DAS}$	T_{ADAS}	Delay from the falling edge of ALE to the falling edge of $\overline{DAS}$		80		130
45	$\overline{DAS}$	T_{RIDF}	Delay from the rising edge of $\overline{DALO}$ to the falling edge of $\overline{DAS}$ (bus master read)		15		
46	$\overline{DAS}$	T_{RDYS}	Delay from the falling edge of $\overline{READY}$ to the rising edge of $\overline{DAS}$	Taryd= 300 ns	75		250
47	$\overline{DALI}$	T_{ROIF}	Delay from the rising edge of $\overline{DALO}$ to the falling edge of $\overline{DALI}$ (bus master read)		15		
48	$\overline{DALI}$	T_{RIS}	$\overline{DALI}$ setup time to the rising edge of $\overline{DAS}$ (bus master read)		135		
49	$\overline{DALI}$	T_{RIH}	$\overline{DALI}$ hold time after the rising edge of $\overline{DAS}$ (bus master read)		0		
50	$\overline{DALI}$	T_{RIOF}	Delay from the rising edge of $\overline{DALI}$ to the falling edge of $\overline{DALO}$ (bus master read)		55		
51	$\overline{DALO}$	T_{OS}	$\overline{DALO}$ setup time to the falling edge of ALE (bus master read)		110		
52	$\overline{DALO}$	T_{ROH}	$\overline{DALO}$ hold time after the falling edge of ALE (bus master read)		35		
53	$\overline{DALO}$	T_{WDSI}	Delay from the rising edge of $\overline{DAS}$ to the rising edge of $\overline{DALO}$ (bus master write)		35		

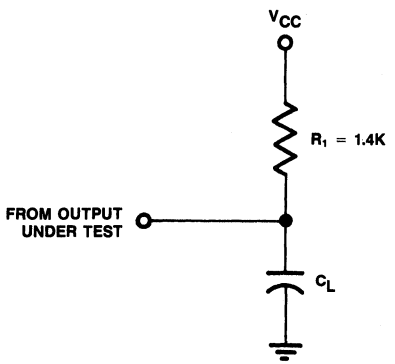
AC TIMING SPECIFICATIONS (Continued)
T_A = 0°C to 70°C, V_{CC} = +5 V ±5 percent, unless otherwise specified.

NO.	SIGNAL	SYMBOL	PARAMETER	TEST CONDITIONS	MIN (ns)	TYP (ns)	MAX (ns)
54	$\overline{CS}$	T_{CSH}	$\overline{CS}$ hold time after the rising edge of $\overline{DAS}$ (Bus slave)		0		
55	$\overline{CS}$	T_{CSS}	$\overline{CS}$ setup time to the falling edge of $\overline{DAS}$ (Bus slave)		0		
56	ADR	T_{SAH}	ADR hold time after the rising edge of $\overline{DAS}$ (Bus slave)		0		
57	ADR	T_{SAS}	ADR setup time to the falling edge of $\overline{DAS}$ (Bus slave)		0		
58	$\overline{READY}$	T_{ARYD}	Delay from the falling edge of ALE to the falling edge of $\overline{READY}$ to insure a minimum bus cycle time (600 ns)				80
59	$\overline{READY}$	T_{SRDS}	Data setup time to the falling edge of $\overline{READY}$ (Bus slave read)		75		
60	$\overline{READY}$	T_{RDYH}	$\overline{READY}$ hold time after the rising edge of $\overline{DAS}$ (Bus master)		0		
61	$\overline{READY}$	T_{SRO1}	$\overline{READY}$ driver turn on after the falling edge of $\overline{DAS}$ (Bus slave)	(CSR 0,3, RAP)		600	
62	$\overline{READY}$	T_{SRO2}	$\overline{READY}$ driver turn on after the falling edge of $\overline{DAS}$ (Bus slave)	(CSR 1,2)		1400	
63	$\overline{READY}$	T_{SRYH}	$\overline{READY}$ hold time after the rising edge of $\overline{DAS}$ (Bus slave)		0		35
64	READ	T_{SRH}	READ hold time after the rising edge of $\overline{DAS}$ (Bus slave)		0		
65	READ	T_{SRS}	READ setup time to the falling edge of $\overline{DAS}$ (Bus slave)		0		



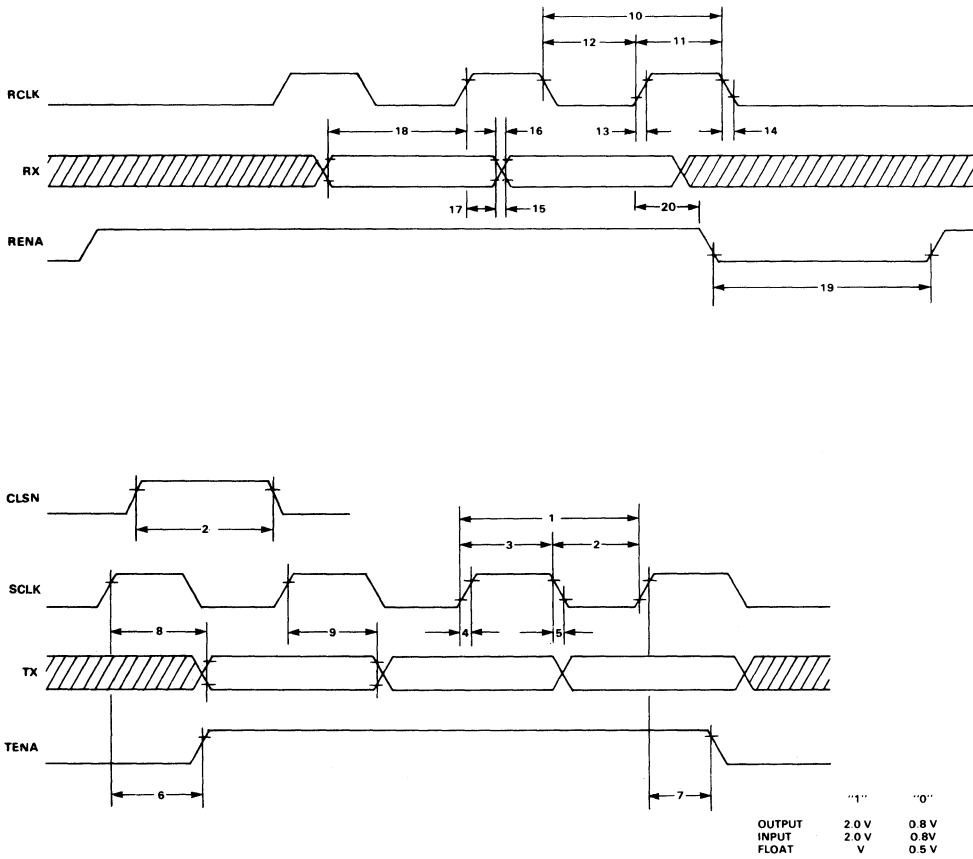
NOTE: This load is used on DAL00 through DAL15, READ, DALI, DALO, DAS, BM0, BM1, ALE/AS, A16 through A23, TENA, and TX.

Figure 4. Output Load Diagram



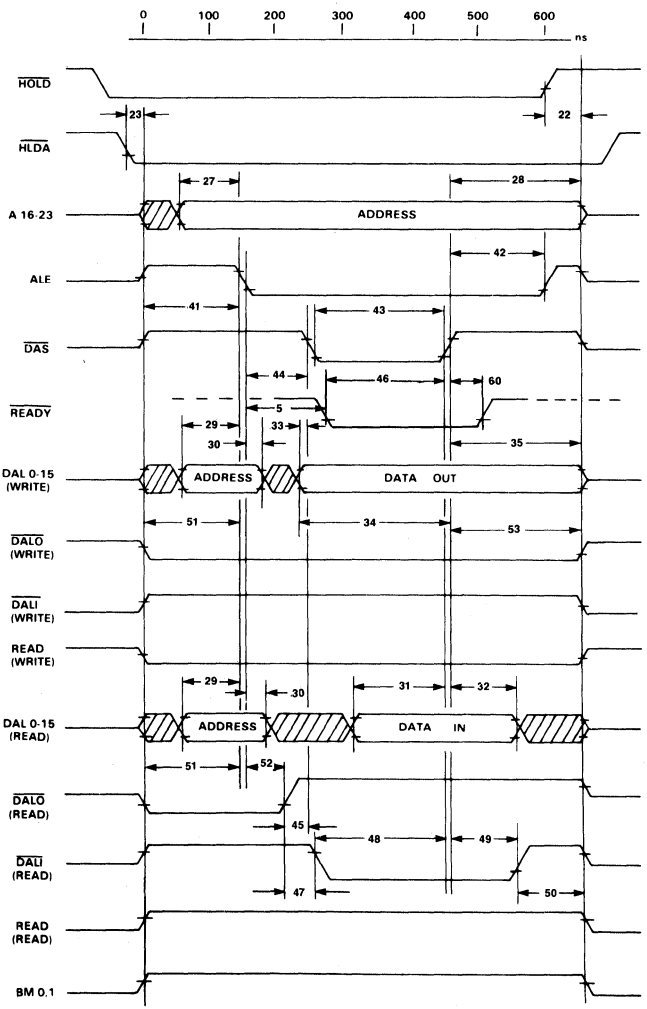
NOTE: This load is used on open drain outputs $\overline{\text{INTR}}$, $\overline{\text{HOLD}}$/$\overline{\text{BUSRQ}}$, and $\overline{\text{READY}}$.

Figure 5. Open Drain Output Load Diagram



NOTE: Timing measurements are made at the following voltages unless otherwise specified.

Figure 6. Physical Link Signaling Timing Diagram - PLS-VMAC Interface Signals



NOTE: The Bus Master cycle time will increase from a minimum of 600 ns in 100 ns steps until the slave device returns $\overline{\text{READY}}$.

Figure 7. MK5032 Bus Master Timing Diagram

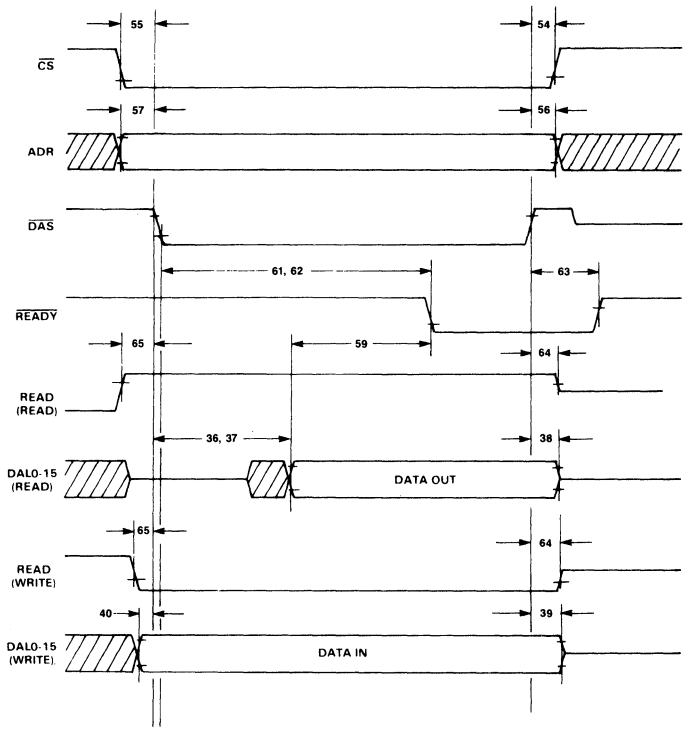


Figure 8. MK5032 Bus Slave Timing Diagram

THOMSON COMPONENTS MOSTEK

MK5033N

MANCHESTER ENCODER/DECODER

COMMUNICATIONS PRODUCTS

FEATURES

- ☐ Conforms to StarLAN specifications.
- ☐ Supports multi-point extension.
- ☐ Auto compensation for line reversal.
- ☐ Compatible with most Ethernet controller chips.
- ☐ Data rates DC to 2.66Mbps supported.
- ☐ Manchester or Differential Manchester data encoding/decoding.
- ☐ Full duplex or half duplex operation.
- ☐ Supports Star, Bus, or Point-to-Point network topologies.
- ☐ Collision detection circuitry with the following features:
  - Detects missing mid-bit transitions
  - Transitions too close together
  - Transitions too far apart
  - External collision input pin
  - Carrier dropout
  - Watchdog timer
  - AT&T Release 1 collision presence signal
  - Echo timeout
- ☐ Optional end-of-frame detection.
  - Input protection at end-of-frame
- ☐ Loopback capability.
- ☐ Receive carrier automatically converted to a level signal.
- ☐ Optional Watchdog timer to prevent continuous transmission.
- ☐ Optional Echo timer to signal error if transmitted frame is not received.
- ☐ Optional Heartbeat generation.
- ☐ In 82586/82588 mode, insensitive to extra bits ahead of preamble.

*Crystal inputs have CMOS thresholds.

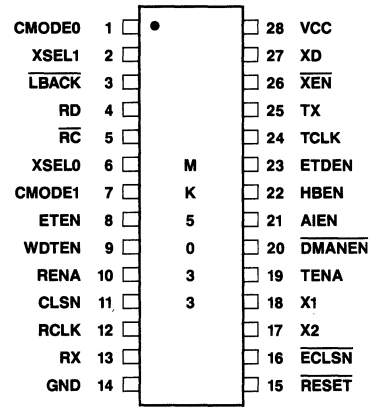


Figure 1. MK5033 Pin Assignment

- ☐ Digital phase-locked loop.
- ☐ On chip crystal oscillator, 16, 10, 8, or 6X operation.
- ☐ CMOS technology.
- ☐ 28-pin DIP.
- ☐ Single 5-volt supply.
- ☐ All inputs and outputs TTL compatible.*
- ☐ Outputs are also CMOS compatible.
- ☐ Industrial version available.

GENERAL DESCRIPTION

The MK5033 is a general purpose Manchester Encoder/Decoder. It incorporates several features that make it an ideal StarLAN station chip. The MK5033 performs three functions. It encodes data from a controller chip into Manchester or Differential data. It decodes Manchester or Differential Manchester data from the line transceiver and produces NRZ data and clock for the controller chip. It also detects collision and signals the controller chip that a collision has occurred.

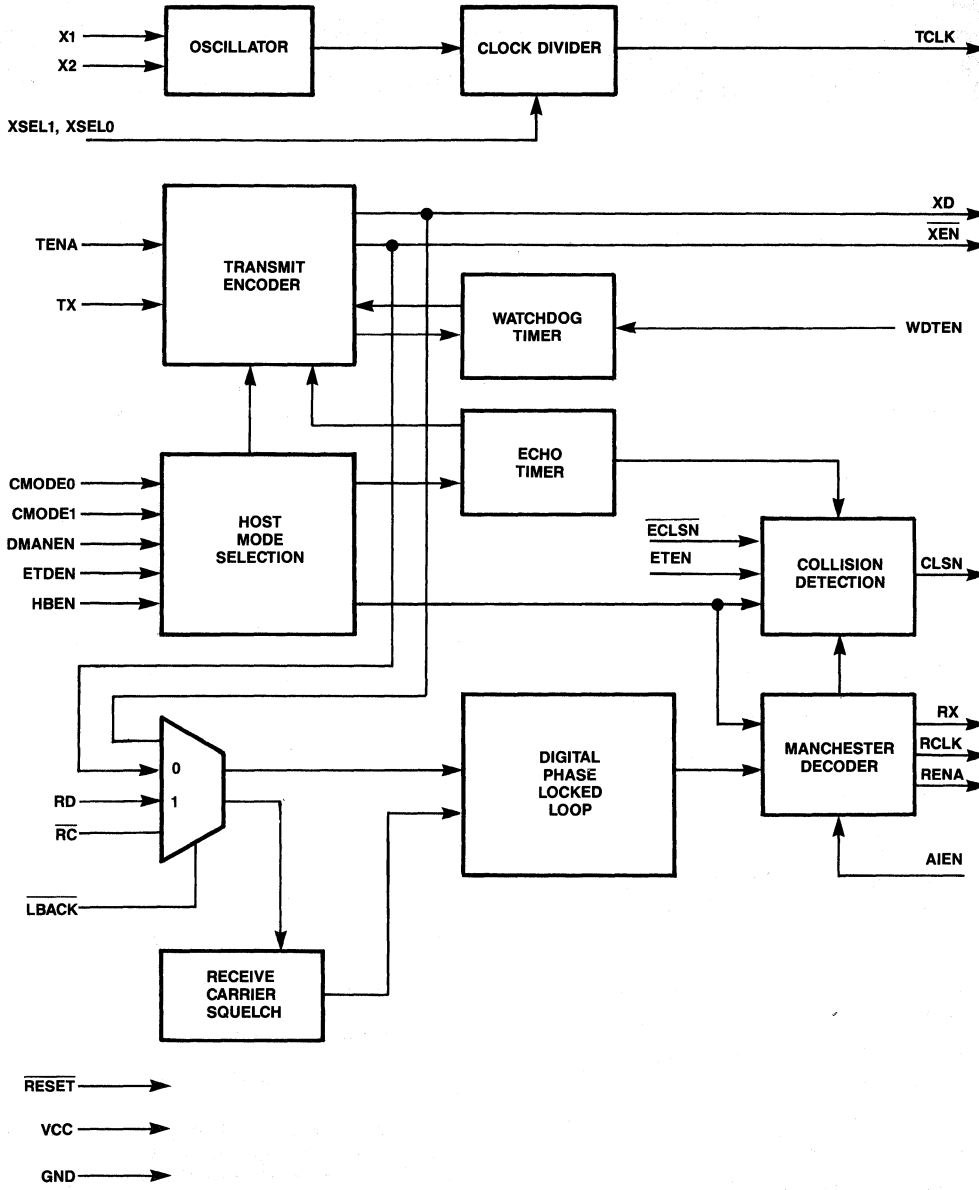


Figure 2. Manchester Encoder/Decoder Block Diagram

PIN DESCRIPTIONS:

CONTROLLER INTERFACE

RX	Output	RX is the serial receive data after decoding.
RENA	Output	This signal indicates that data is available to the controller on the RX output.
RCLK	Output	This is the receive data clock recovered from incoming data on the RD pin.
TX	Input	This is the serial data to be transmitted. It is clocked into the chip by TCLK.
TENA	Input	This signal indicates that data is valid on the TX input. It goes active with the first bit of transmission.
TCLK	Output	This is the transmit data clock. All transmit interface signals are synchronized to this clock. This clock is always active.
CLSN	Output	This signal is asserted when a Manchester violation is detected on the RD line or when the external collision input ($\overline{ECLSN}$) goes active. It is also asserted if either of the timers expire. It is deasserted when line idle is detected on the RD line and TENA goes inactive.

TRANSCEIVER INTERFACE

XD	Output	Transmit data output.
$\overline{XEN}$	Output	Transmit output enable. This signal goes low to signal XD active. It goes high at the end of transmission. NOTE: If ETDEN is active XD will remain high for 2-bit times at the end of a frame and $\overline{XEN}$ will remain low during this time.
RD	Input	Receive data input.
$\overline{RC}$	Input	Receive carrier input. Receive carrier can be either a pulse stream or an active low signal to indicate carrier active. The chip contains internal squelch circuitry, as shown in Figure 3, to convert a pulse signal to a level signal.
$\overline{ECLSN}$	Input	External collision input. When this pin is held low for at least 20 nS an external collision is signaled.

MISCELLANEOUS

CMODE1, CMODE0 Inputs — These two mode bits allow the chip to be used with a variety of controller chips.

CMODE1 = 1, CMODE0 = 0 (10) 82586/82588 (See Note)

Transmit data (TX) is sampled on the rising edge of TCLK.

Receive data (RX) transitions on the rising edge of RCLK.

TENA - active low
RENA - active low - goes active when phase locked loop is locked
CLSN - active low

CMODE1 = 1 CMODE0 = 1 (11) MOSTEK LANCE MK68590

Transmit data (TX) is sampled on the falling edge of TCLK.
Receive data (RX) transitions on the falling edge of RCLK.

TENA - active high
RENA - active high - goes active when receive carrier goes active
CLSN - active high

CMODE1 = 0 CMODE0 = 0 (00) TEST Mode

This mode is only useful for production testing.

NOTE: Compatibility with controller chips based on preliminary controller data sheets.

CMODE1 = 0 CMODE0 = 1 (01) Mostek Variable Bit Rate LANCE MK5032 (See note)

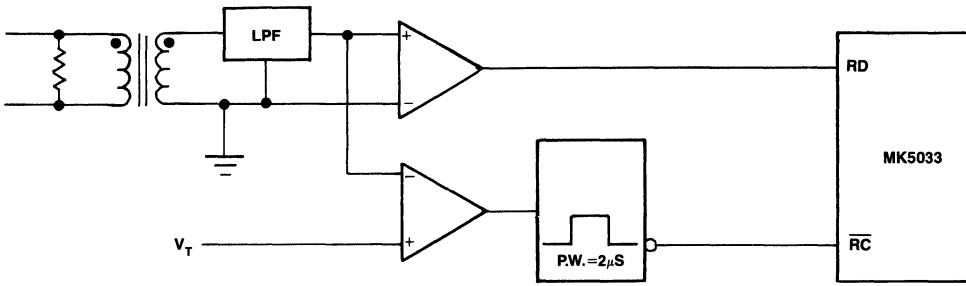
TENA - active high
RENA - active high - goes active when receive carrier goes active
CLSN - active high

$\overline{\text{DMANEN}}$	Input	When this pin is low the chip encodes and decodes serial data using Differential Manchester. When this pin is high it uses Manchester.
HBEN	Input	When this pin is high the chip will signal CLSN after TENA is deasserted at the end of transmission. CLSN remains active until link idle is received on RD.
ETDEN	Input	When this pin is high the chip will recognize end-of-frame as specified in the StarLAN specification. It will also ignore incoming data on RD for 20 data bits after the end of a received frame.
AIEN	Input	Auto Inversion Enable. If both frame recognition is enabled and Manchester is selected, then if AIEN is high the frame polarity is sensed and corrected if necessary. If AIEN is low, ETDEN is low, or $\overline{\text{DMANEN}}$ is low, then auto compensation for line reversal is disabled.
ETEN	Input	When ETEN is high the echo timer is activated. The echo timer starts at the beginning of a transmitted frame. If a receive carrier is not received with 510 TCLKS, then collision will be asserted.
WDTEN	Input	When WDTEN is high the watchdog timer is activated. The timer starts when TENA is asserted. If TENA goes inactive before the timer expires, the timer is reset. If the timer expires, transmission is aborted and collision asserted.
$\overline{\text{LBACK}}$	Input	When this pin is low the chip will be put into internal loopback. The transmit data will be internally looped back into the input RD. The outputs XD and $\overline{\text{XEN}}$ will be held idle during loopback.
$\overline{\text{RESET}}$	Input	When this pin is low the chip is in reset mode. All interface signals will be inhibited except TCLK. $\overline{\text{RESET}}$ must remain active for at least three TCLK periods.
XSEL0, XSEL1	Inputs	These inputs select which frequency clock or crystal is to be connected to X1 and X2.

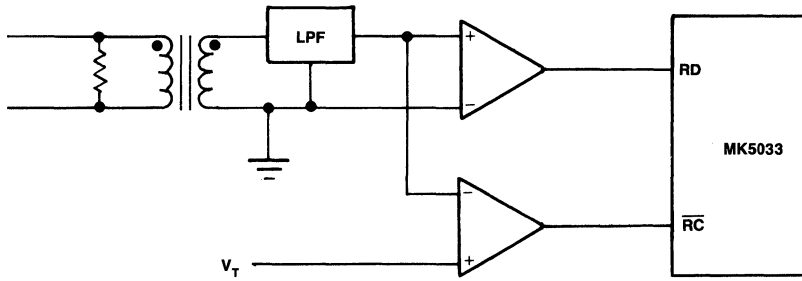
XSEL1	XSEL0	CLOCK DIVISOR
0	0	16 X
0	1	8 X
1	0	10 X
1	1	6 X

X1, X2	Inputs	Crystal oscillator inputs. A crystal can be connected between these inputs, or a CMOS level square wave can be connected to X1 while X2 is left unconnected.
VCC	Input	+5V ± 5%
GND		

NOTE: Compatibility with controller chips based on preliminary controller data sheets.



EXTERNAL SQUELCH



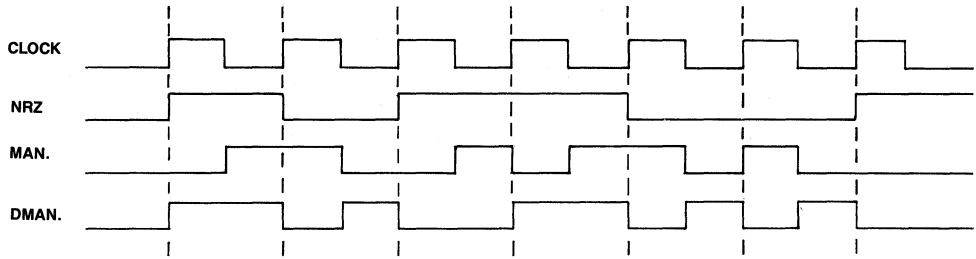
INTERNAL SQUELCH

Figure 3. Internal Versus External Squelch

CIRCUIT DESCRIPTION

TRANSMITTER

The transmitter encodes NRZ data from the controller chip into Manchester or Differential Manchester Space data. The diagram below shows the two encoding schemes.



Data encoding and transmission begin when the controller chip brings TENA active. The start of data encoding is delayed by two bits when in 82586/82588 mode. TX data is sampled using TCLK as the clock. Data is encoded into Manchester or Differential Manchester Space, as shown above, depending upon the state of $\overline{\text{DMANEN}}$. The encoded data is output on XD. $\overline{\text{XEN}}$ goes low with the first bit of data output on XD. The transmit delay, delay from TENA active to $\overline{\text{XEN}}$ active, is less than 2 TCLKs in LANCE modes (4 TCLKS in 82586/82588 mode). The controller chip signals end of data by bringing TENA inactive. The pin ETDEN controls how the MK5033 handles the end transmission.

If ETDEN is high the MK5033 will add a delimiter to the data stream after the last bit is transmitted. In Manchester mode XD will be held high for 1.5 TCLKs if the last data bit is a one and for 2 TCLKs if the last data bit is a zero. During this time $\overline{\text{XEN}}$ is held active. In Differential Manchester, XD is toggled after the last data bit and held in that state for 2 TCLKs. $\overline{\text{XEN}}$ is active during this time. After the delimiter has been sent, $\overline{\text{XEN}}$ is brought inactive.

If ETDEN is low the MK5033 will not add any delimiter to the data stream. $\overline{\text{XEN}}$ will be brought inactive after the last data bit has been output.

RECEIVER

The receiver consists of four major sections:

1) Receive carrier squelch
2) Internal loopback
3) Digital phase locked loop
4) Manchester/Differential Manchester decoder

Depending on the state of $\overline{\text{DMANEN}}$, the receiver decodes Manchester or Differential Manchester space data from pin RD into NRZ form. It also extracts timing (RCLK) from the data. The NRZ data is output to the controller on pin RX.

RECEIVE CARRIER SQUELCH

The Receive carrier pin has internal squelch logic that allows the signal to be either a level signal or a pulse train. Receive carrier is active low. The receive carrier must be present for 3 clock samples to be considered a valid carrier. Once the carrier is considered valid then it must be active for only one clock sample time every two bit times to remain valid. (See Figure 3.)

LOOPBACK

When loopback is enabled ($\overline{\text{LBACK}}$ low) RD and $\overline{\text{RC}}$ are ignored. Transmit data is internally looped back as receive data. The transmitter outputs XD and $\overline{\text{XEN}}$ are disabled during loopback.

DIGITAL PHASE LOCKED LOOP (DPLL)

The digital phase locked loop is implemented with a counter that clears on each transition of the receive data. The phase locked loop will declare "lock" after receiving data that has two "long transitions". A long transition occurs when the receive data does not change for at least 4/6 of a bit time in 6X mode (5/8 in 8X, 7/10 in 10X, and 11/16 in 16X). The phase locked loop generates a clock frequency that is 2 times the data rate.

AUTOMATIC COMPENSATION FOR WIRING REVERSAL

When installing twisted pair telephone wiring, it is often difficult and expensive to maintain proper polarity on the wire pairs. The MK5033 will automatically compensate for this reversal. If Manchester coding is selected with both ETDEN = 1 and AIEN = 1 then any frame that is received with inverse polarity will be detected and correct polarity established prior to data decoding.

MANCHESTER/DIFFERENTIAL MANCHESTER DECODER

The receive data (after inversion if enabled) is fed into the decoder along with the recovered 2x clock from the DPLL. The decoder changes the receive data to NRZ

data. The NRZ data is output on RX. RENA signals the controller chip that data is available. (See mode pin descriptions.) RCLK is a 1x clock output that is synchronous with the data on RX.

PROTECTION TIME

After the end of a received frame the receiver is disabled for 20 bit times. This protection time guarantees immunity to spikes caused by transformer coupling after the end of frame.

COLLISION

CLSN is an output to the controller chip that indicates a possible problem with the data. There are several sources of collision.

1) Transitions too close together
   Collision is signaled if the receive data stream transitions a second time in less than 2/6 bit times in 6X mode (3/8 in 8X, 3/10 in 10X, and 5/16 in 16X)

2) Transitions too far apart
   Collision is signaled if the receive data stream does not transition again within 9/6 in 6X mode (10/8 in 8X, 12/10 in 10X, and 20/16 in 16X).

3) Manchester violation
   If the data violates Manchester or Differential Manchester coding rules, depending on DMANEN, then collision is signaled.

4) Watchdog timer
   If the watchdog timer expires, then collision will be signaled, if WDTEN is high.

5) Echo timer
   If the echo timer expires, then collision will be signaled, if ETEN is high.

6) External collision
   If the external collision pin ($\overline{\text{ECLSN}}$) goes low for at least 20ns, then collision will be signaled.

7) Receive carrier lost during transmission
   If the MK5033 is transmitting and the receive carrier goes active and then inactive before it is through transmitting, then collision is signaled.

8) Heartbeat
   Heartbeat is enabled when HBEN is high. If it is enabled, then collision will be signaled 8 TCLKs after TENA goes away, and collision will remain active for at least 8 TCLKs.

Once CLSN is activated it remains active until both TENA and RENA go inactive. The exception to this is heartbeat. If heartbeat signals collision, then collision is guaranteed to remain for 8 TCLKs or until TENA or RENA go inactive, whichever is longer.

WATCHDOG TIMER

When enabled, the watchdog timer ensures that the MK5033 will not transmit for more than 101K bit times. The timer is enabled by bringing WDTEN high and disabled by bringing WDTEN low. If WDTEN is high, the timer is activated when TENA goes active. The timer resets when TENA goes inactive. If TENA remains active for more than 101K bit times, then the timer will time out causing collision to be asserted and $\overline{\text{XEN}}$ to go inactive. If loopback is enabled, watchdog timeout will occur after 325 bit times. This permits run time testing of the watchdog timer.

ECHO TIMER

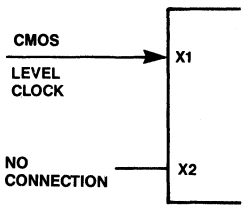
When the echo timer is enabled the MK5033 expects the data that it is transmitting to be received on RD within 510 bit times. The echo timer is activated when TENA goes active. If 510 bit times elapse before RENA goes active, then the timer will time out causing collision to be activated.

Oscillator

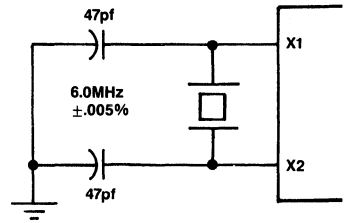
The MK5033 will accept two forms of clock input: a CMOS input or a crystal. If pin X2 is left unconnected, a 6.0/8.0/10.0/16.0 MHz $\pm$ 0.01% CMOS clock may be applied to pin X1. Alternately, a crystal circuit may be connected between X1 and X2 to form the basis of an oscillator. Typically, a 6.0/8.0/10.0/16.0 $\pm$ 0.005% parallel resonant crystal is needed to insure the $\pm$0.01% frequency accuracy required for StarLAN. Refer to Figure 4. A fundamental mode, parallel resonance type crystal should be used with the manufacturer's suggested load capacitance.

Reset Input

The reset pin is an active low Schmidt trigger input. A simple RC network may be used to insure correct operation upon power-up. Refer to Fig. 5.



A) EXTERNAL CLOCK



B) CRYSTAL OPERATION

Figure 4. Oscillator Operation

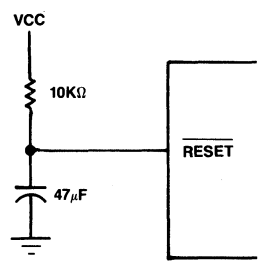


Figure 5. Typical RC Connection For Power-On Reset

ELECTRICAL SPECIFICATIONS

This chapter provides tabular presentations for Absolute Maximum Ratings, DC Characteristics, Capacitance and AC Timing Specifications. In addition, illustrations are provided for an Output Load Diagram (Figure 9) and Station Timing Diagrams.

ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias ..... −25°C to +100°C
Storage Temperature ..... −65°C to +150°C
Voltage on Any Pin with Respect to Ground ..... −0.5 V to V_{CC} +0.5 V
Power Dissipation (no load) 50mW

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = +5 V ±5% unless otherwise specified.

SYMBOL	CONDITIONS	MIN	MAX	UNITS
V_{IL}		−0.5	+0.8	V
V_{IH}	Except X1	+2.0	V_{CC} +0.5	V
V_{IH}	X1	+3.5	V_{CC} +0.5	V
V_{OL}	@ I_{OL} = 3.2 mA, except X2		+0.5	V
V_{OH}	@ I_{OH} = −0.4 mA, except X2	+2.4		V
V_{OH}	@ I_{OH} = −40 μA, except X2	+3.2		V
I_{IL}	@ V_{IN} = 0.4 to V_{CC}, except XSEL0, CMODE1, ETEN WDTEN, $\overline{\text{DMANEN}}$, AIEN, HBEN, ETDEN		±10	μA
I_{IL}	@ V_{IN} = 0.4 to V_{CC}, XSEL0, CMODE1, ETEN WDTEN, $\overline{\text{DMANEN}}$, AIEN, HBEN, ETDEN		±100	μA
I_{CC}			8	mA

CAPACITANCE

F = 1 MHz

SYMBOL	CONDITIONS	MIN	MAX	UNITS
C_{IN}			10	pf
C_{OUT}			10	pf
C_{IO}			20	pf

AC TIMING SPECIFICATIONS

T_A = 0°C to 70°C, V_{CC} = +5 V ±5% unless otherwise specified, V_{TH} = 2.0 V, V_{TL} = 0.8 V.

#	SIGNAL	SYMBOL	PARAMETER	MIN ns	TYP ns	MAX ns
1	X1	T_{X1T}	X1 period	62		
2	X1	T_{X1L}	X1 low time	24		
3	X1	T_{X1H}	X1 high time	24		
4	X1	T_{X1R}	Rise time of X1	0		8
5	X1	T_{X1F}	Fall time of X1	0		8

AC TIMING SPECIFICATIONS (cont.)

T_A = 0°C to 70°C, V_{CC} = +5 V ±5% unless otherwise specified, V_{TH} = 2.0 V, V_{TL} = 0.8 V.

#	SIGNAL	SYMBOL	PARAMETER	MIN ns	TYP ns	MAX ns
6	$\overline{XEN}$	$T_{\overline{XEN}}$	$\overline{XEN}$ delay from X1		40	65
7	XD	T_{XD}	XD delay from X1		40	65
8	XD	J_{XD}	Transmit jitter $\lvert T_{XD}\uparrow - T_{XD}\downarrow \rvert \div 2$		4	6
9	TCLK	T_{CLK}	TCLK delay from X1			70
10	TX	T_{TXST1}	TX setup to falling edge of TCLK, CMODE = 1	90		
11	TX	T_{TXHT1}	TX hold from falling edge of TCLK, CMODE = 1	15		
12	TX	T_{TXS}	TX setup to X1	15		
13	TX	T_{TXH}	TX hold from X1	15		
14	TENA	T_{TNAST1}	TENA setup to falling edge of TCLK, CMODE = 1	90		
15	TENA	T_{TNAST1}	TENA hold from falling edge of TCLK, CMODE = 1	15		
16	TENA	T_{TENAS}	TENA setup to X1	15		
17	TENA	T_{TENAH}	TENA hold from X1	15		
18	TX	T_{TXST0}	TX setup to rising edge of TCLK, CMODE = 0	90		
19	TX	T_{TXHT0}	TX hold from rising edge of TCLK, CMODE = 0	15		
20	TX	T_{TXS}	TX setup to X1, CMODE = 0	15		
21	TX	T_{TXH}	TX hold from X1, CMODE = 0	15		
22	TENA	T_{TNAST0}	TENA setup to positive edge of TCLK, CMODE = 0	90		
23	TENA	T_{TNAHT0}	TENA hold from positive edge of TCLK, CMODE = 0	15		
24	TENA	T_{TNAS}	TENA setup to X1, CMODE = 0	15		
25	TENA	T_{TNAH}	TENA hold from X1, CMODE = 0	15		
26	CLSN	T_{CLSN}	CLSN delay from X1			70
27	$\overline{ECLSN}$	$T_{\overline{ECLSN}}$	Minimum detected pulse width		5	20
28	$\overline{RC}$	$T_{\overline{RCS}}$	$\overline{RC}$ setup to X1	15		
29	$\overline{RC}$	$T_{\overline{RCH}}$	$\overline{RC}$ hold from X1	15		
30	RD	T_{RDS}	RD setup to X1	15		
31	RD	T_{RDH}	RD hold from X1	15		
32	RD	J_{RD6}	RD Incoming Jitter Tolerance, 6X mode, X1 = 6 MHz, $T_{X1T} - \lvert T_{RDS}\uparrow - T_{RDS}\downarrow \rvert$		165	161
33	RD	J_{RD8}	RD Incoming Jitter Tolerance, 8X mode, X1 = 8 MHz, $T_{X1T} - \lvert T_{RDS}\uparrow - T_{RDS}\downarrow \rvert$		123	119
34	RD	J_{RD10}	RD Incoming Jitter Tolerance, 10X mode, X1 = 10 MHz, $T_{X1T} - \lvert T_{RDS}\uparrow - T_{RDS}\downarrow \rvert$		198	194
35	RD	J_{RD16}	RD Incoming Jitter Tolerance, 16X mode, X1 = 16 MHz, $T_{X1T} - \lvert T_{RDS}\uparrow - T_{RDS}\downarrow \rvert$		186	182
36	RCLK	T_{RCLK}	RCLK delay from X1, CMODE = 1		40	65
37	RX	T_{RXRCK1}	RX delay from falling RCLK, CMODE = 1	−30		30
38	RX	T_{RX}	RX delay from X1, CMODE = 1		40	65

AC TIMING SPECIFICATIONS (cont.)

T_A = 0°C to 70°C, V_{CC} = +5 V ±5% unless otherwise specified, V_{TH} = 2.0 V, V_{TL} = 0.8 V.

#	SIGNAL	SYMBOL	PARAMETER	MIN ns	TYP ns	MAX ns
39	RENA	$T_{RNARCK1}$	RENA delay from falling RCLK, CMODE = 1	−30		30
40	RENA	T_{RENA}	RENA delay from X1, CMODE = 1		45	65
41	CLSN	$T_{CSNRCK1}$	CLSN delay from falling edge RCLK, CMODE = 1	−30		30
42	CLSN	T_{CLSN}	CLSN delay from X1, CMODE = 1			70
43	RCLK	T_{RCLK0}	RCLK delay from X1, CMODE = 0		40	65
44	RCLK	P_{RCLK}	RCLK pulse width, CMODE = 0	T_{X1T} −20		T_{X1T}+20
45	RCLK	T_{RXCLK}	RCLK delay from RX stable, CMODE = 0	T_{X1T} −20		
46	RX	T_{CLKRX}	RX hold from falling edge of RCLK, CMODE = 0	$2*T_{X1T}-20$		
47	RCLK	T_{RNACLK}	RCLK delay from RENA stable, CMODE = 0	T_{X1T} −20		
48	RENA	T_{CLKRNA}	RENA hold from falling edge of RCLK, CMODE = 0	$2*T_{X1T}-20$		
49	RCLK	T_{CSNCLK}	Rising RCLK delay from CLSN stable, CMODE = 0	$2*T_{X1T}-20$		
50	CLSN	T_{CLKCSN}	CLSN delay from rising edge of RCLK, CMODE = 0	T_{X1T} −20		

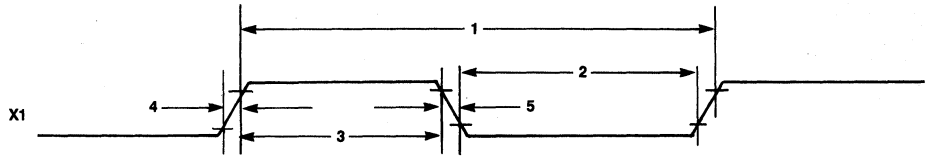


Figure 6. External X1 Timing Diagram

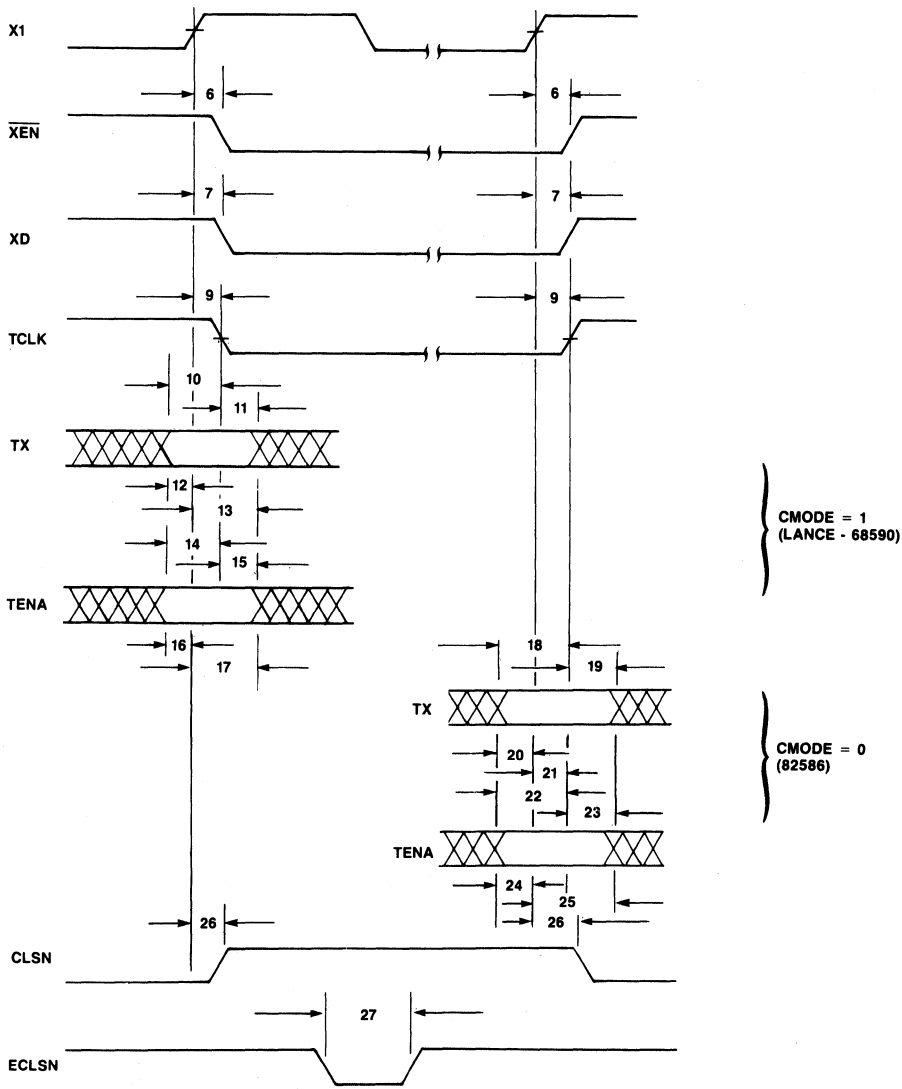


Figure 7. Transmit Timing Diagram

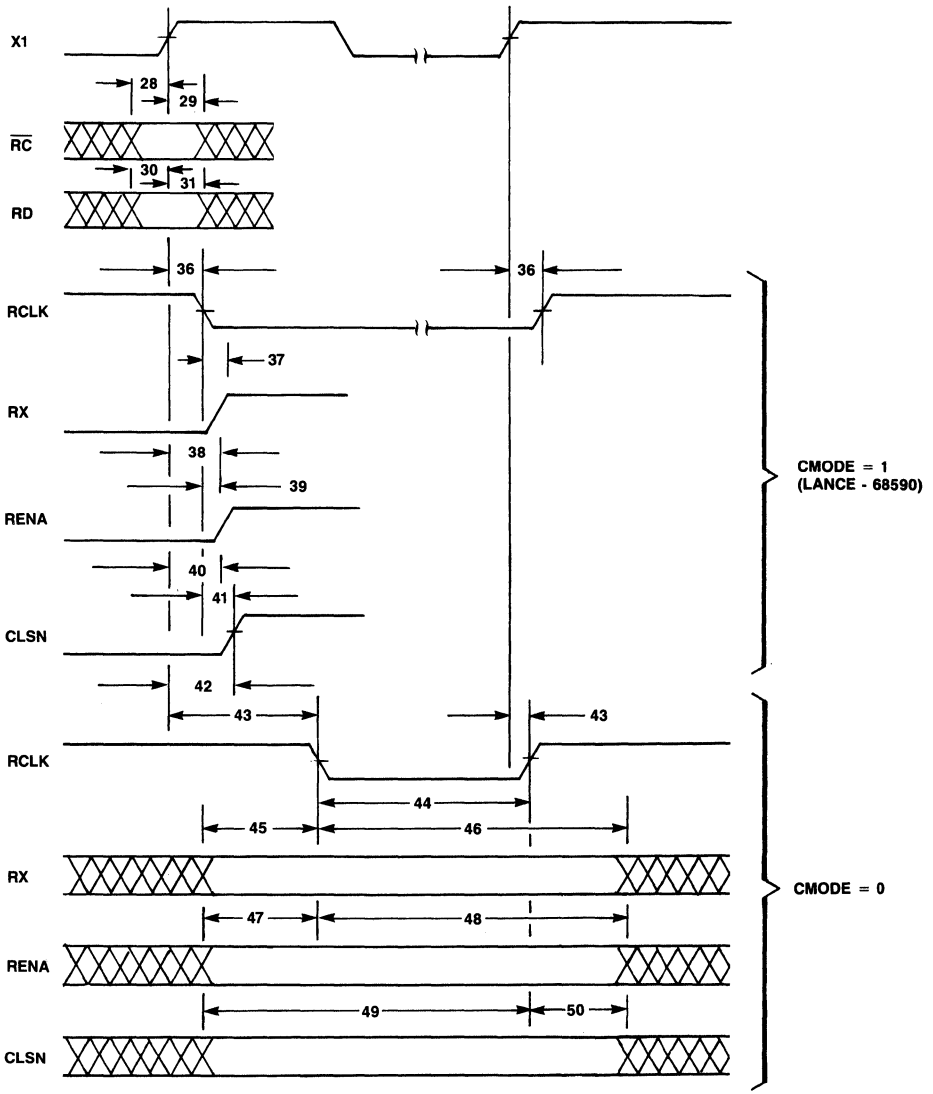


Figure 8. Receiver Timing Diagram

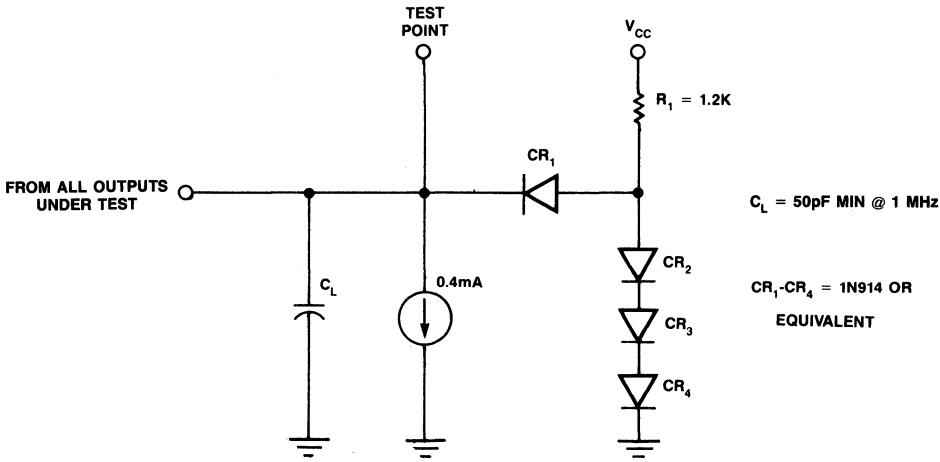
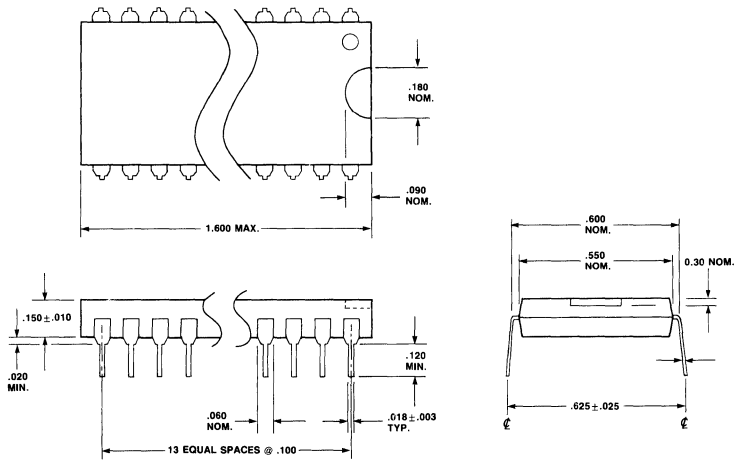


Figure 9. Output Load Diagram

PACKAGE DESCRIPTION
Plastic Dual-In-Line (N)
28-Pin
MK5033N



THOMSON COMPONENTS MOSTEK

MK5035N

StarLAN ENCODER DECODER

COMMUNICATIONS PRODUCTS

FEATURES

- ☐ Conforms with StarLAN specification.
- ☐ Supports multi-point extension.
- ☐ Auto compensation for line reversal.
- ☐ Compatible with Mostek MK68590 LANCE and Intel 82586/82588.
- ☐ Close pin compatibility with SEEQ8023.
- ☐ Data rates to 2.66Mbps supported.
- ☐ Manchester data encoding/decoding.
- ☐ Collision detection circuitry with the following features:
  - Detects missing mid-bit transitions
  - Transitions too close together
  - Transitions too far apart
  - External collision input pin
  - Carrier dropout
  - Watchdog timer
  - AT&T Release 1 collision presence signal
  - Echo timeout
- ☐ Receive end-of-frame detection.
  - Input protection at end-of-frame
- ☐ Loopback capability.
- ☐ Receive carrier automatically converted to a level signal.
- ☐ Echo timer to signal error if transmitted frame is not received.
- ☐ Heartbeat generation.
- ☐ In 82586 mode, insensitive to extra bits ahead of preamble
- ☐ Digital phase-locked loop.
- ☐ On chip crystal oscillator, 8X or 6X operation.

*Crystal inputs have CMOS thresholds.

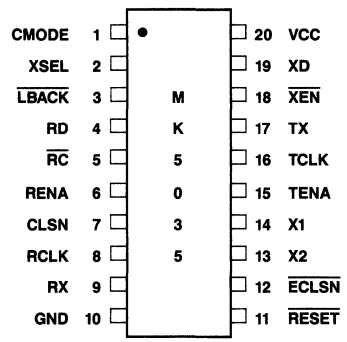


Figure 1. MK5035 Pin Assignment

- ☐ CMOS technology.
- ☐ 20-pin DIP.
- ☐ Single 5-volt supply.
- ☐ All inputs and outputs TTL compatible.*
- ☐ Outputs are also CMOS compatible.
- ☐ Industrial version available.

GENERAL DESCRIPTION

The MK5035 is a Manchester Encoder/Decoder chip incorporating several features that make it an ideal StarLAN station chip. The MK5035 performs three functions. It encodes data from a controller chip into Manchester data. It decodes Manchester data from the line transceiver and produces NRZ data and clock for the controller chip. It also detects collisions and signals the controller chip that a collision has occurred.

The MK5035 has several enhancements for StarLAN and Multi-Point extension (MPE) StarLAN. These include auto compensation for wiring reversal, echo timer, external collision detect, watchdog timer, and heartbeat, among others.

PIN DESCRIPTIONS:

CONTROLLER INTERFACE

RX	Output	RX is the serial receive data after decoding.
RENA	Output	This signal indicates that data is available to the controller on the RX output.
RCLK	Output	RCLK is the receive data clock recovered from the incoming data RD.
TX	Input	TX is the serial data to be transmitted. It is clocked into the chip by TCLK.
TENA	Input	This signal indicates that data is valid on the TX input. It goes active with the first bit of transmission.
TCLK	Output	TCLK is the transmit data clock. All transmit interface signals are synchronized to this clock.
CLSN	Output	This signal is asserted when a manchester violation is detected on the RD line or when the external collision input ($\overline{ECLSN}$) goes active.

TRANSCEIVER INTERFACE

XD	Output	Encoded transmit data output.
$\overline{XEN}$	Output	Transmit output enable. This signal goes low to indicate XD active. It goes high at the end of transmission.
RD	Input	Encoded receive data input.
$\overline{RC}$	Input	Receive carrier input. Receive carrier can be either a pulse stream or an active low signal to indicate carrier active. The chip contains internal squelch circuitry, as shown in Figure 3, to convert a pulse signal to a level signal.
$\overline{ECLSN}$	Input	External collision input. When this pin is held low for at least 20 nS, an external collision is signaled.

OTHER PINS

CMODE Input — This input allows the part to be used with either Mostek or Intel controllers:

CMODE = 0, 82586/82588 (See Note)

Transmit data (TX) is sampled on the rising edge of TCLK.
Receive data (RX) transitions on the rising edge of RCLK.

TENA - active low
RENA - active low - goes active when phase lock loop is locked.
CLSN - active low

CMODE = 1, MOSTEK LANCE MK68590

Transmit data (TX) is sampled on the falling edge of TCLK.
Receive data (RX) transitions on the falling edge of RCLK.

TENA - active high
RENA - active high - goes active when phase lock loop is locked.
CLSN - active high

$\overline{LBACK}$	Input	When this input is low the part will be put into internal loopback. The transmit data will be internally looped back as receive data. See Figure 2. The outputs XD and $\overline{XEN}$ will be held inactive during loopback.
$\overline{RESET}$	Input	When this pin is low the chip is in reset mode. All interface signals will be inhibited except TCLK. $\overline{RESET}$ should remain active for three TCLK periods.
XSEL	Input	This input selects the clock divider. If XSEL = 0, it is 8X. If XSEL = 1, it is 6X.

NOTE: Compatibility with controller chips based on preliminary controller data sheets.

X1,X2	Inputs	Crystal oscillator inputs. A crystal can be connected between these inputs, or a CMOS level square wave can be connected to X1 while X2 is left unconnected.	VCC	Input	+5V ± 5%
			GND		

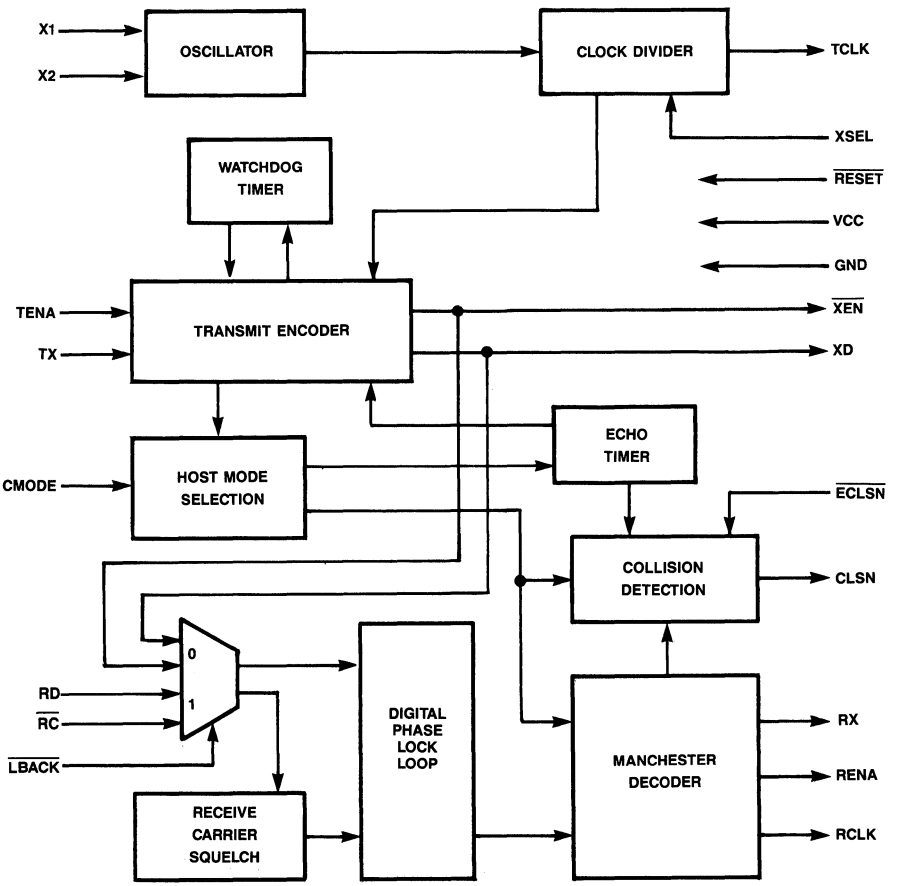
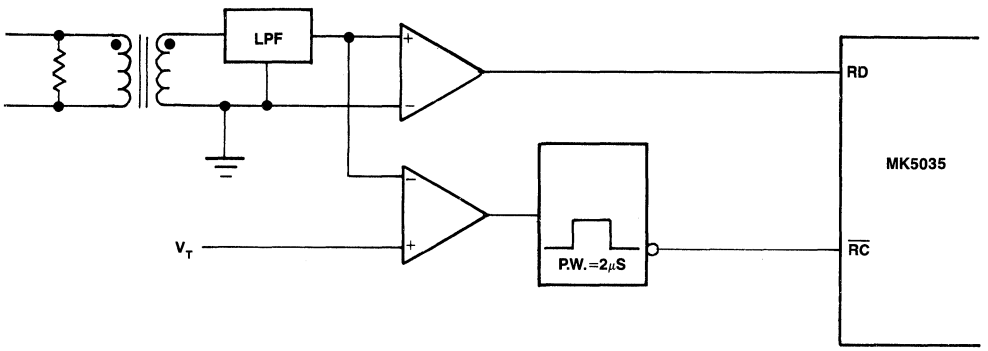
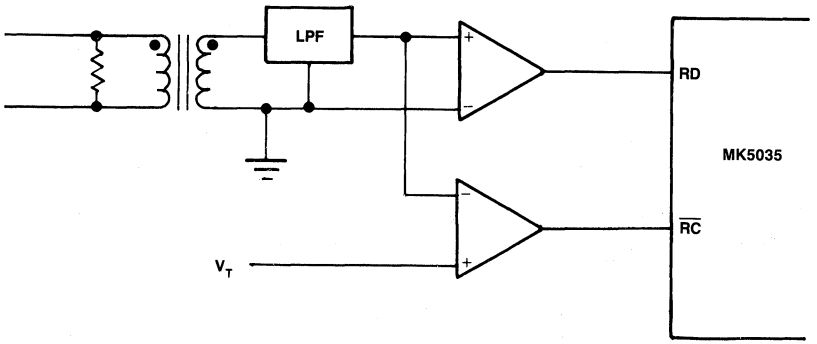


Figure 2. StarLAN Encoder Decoder. MK5035



EXTERNAL SQUELCH



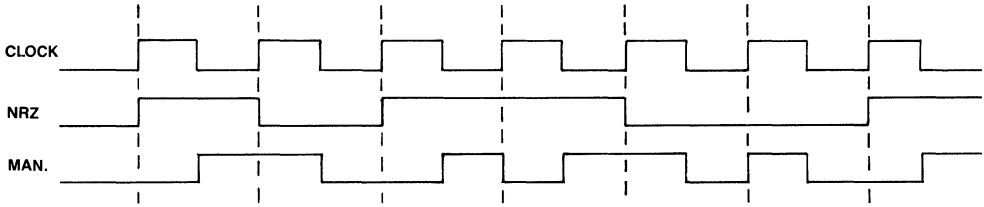
INTERNAL SQUELCH

Figure 3. Internal Versus External Time Squelch

CIRCUIT DESCRIPTION

TRANSMITTER

The transmitter encodes NRZ data from the controller chip into the Manchester data. The diagram below shows the two encoding schemes.



Data encoding and transmission begin when the controller chip brings TENA active. The start of data encoding is delayed by two bits when in 82586/82588 mode. TX is sampled using TCLK as the clock. The encoded data is output on XD. $\overline{XEN}$ goes low with the first bit of data output on XD. The transmit delay, delay from TENA active to $\overline{XEN}$ active, is less than 2 TCLKs in LANCE mode (4 TCLKs in 82586/82588 mode). The controller chip signals end of data by bringing TENA inactive.

XD will be held high for an additional 1.5 TCLKs if the last data bit is a one, and for 2 TCLKs if the last data bit is a zero. During this time $\overline{XEN}$ is held active.

RECEIVER

The receiver consists of four major sections.

1) Receive carrier squelch
2) Internal loopback
3) Digital phase locked loop
4) Manchester decoder

The receiver takes Manchester data in on RD, when receive carrier ($\overline{RC}$) is active, and decodes the data into NRZ data and also produces clock (RCLK) from the data. The NRZ data is output to the controller on RX.

RECEIVE CARRIER SQUELCH

The Receive carrier pin has internal squelch logic that allows the signal to be either a level signal or a pulse train. Receive carrier is active low. The receive carrier must be present for 3 clock samples to be considered a valid carrier. Once the carrier is considered valid then it must be active for only one clock sample time every two bit times to remain valid. (See Figure 3.)

Automatic Compensation For Wiring Reversal

When installing twisted pair telephone wiring, it is often difficult and expensive to maintain proper polarity on the wire pairs. The MK5035 will automatically compensate for this reversal. Any frame that is received with inverse polarity will be detected and decoded with the correct polarity.

LOOPBACK

When loopback is enabled ($\overline{LBACK}$ low), RD and $\overline{RC}$ are ignored. Transmit data is internally looped back as receive data. The transmitter outputs XD and $\overline{XEN}$ are disabled during loopback.

DIGITAL PHASE LOCKED LOOP (DPLL)

The digital phase locked loop is implemented with a counter that clears on each transition of the receive data. The phase locked loop will declare "lock" after receiving data that has two "long transitions". A long transition occurs when the receive data does not change for at least 4/6 (5/8 in 8X mode) of a bit time.

MANCHESTER DECODER

The receive data (after inversion if needed) is fed into the decoder along with the recovered 2X clock from the DPLL. The decoder changes the receive data to NRZ data. The NRZ data is output on RX. RENA signals the controller chip that data is available. (See mode pin descriptions.) RCLK is a 1X clock output that is synchronous with the data on RX.

PROTECTION TIME

After the end of a received frame the receiver is disabled for 20 bit times. This protection time guarantees immunity to spikes caused by transformer coupling after the end of frame.

COLLISION

CLSN is an output to the controller chip that indicates a possible problem with the data. There are several sources of collision.

1) Transitions too close together
   Collision is signaled if the receive data stream tran-

sitions a second time in less than 2/6 (3/8 in 8X mode) bit times.

2) Transitions too far apart
Collision is signaled if the receive data stream does not transition again within 9/6 (10/8 in 8X mode) bit times.

3) Manchester violation
If the data violates Manchester coding rules, then collision is signaled.

A Manchester violation is a missing mid-bit transition.

4) Watchdog timer
If the watchdog timer expires, then collision will be signaled.

5) Echo timer
If the echo timer expires without receive carrier going active, then collision will be signaled.

6) External collision
If the external collision pin ($\overline{\text{ECLSN}}$) goes low for at least 20ns, then collision will be signaled.

7) Receive carrier lost during transmission
If the MK5035 is transmitting and the receive carrier goes active and then inactive before it is through transmitting, then collision is signaled.

8) Heartbeat
Collision, as a result of heartbeat, will be signaled 8 TCLKs after TENA goes away, and collision will remain active for at least 8 TCLKs.

Once CLSN is activated it remains active until both TENA and RENA go inactive. The exception to this is heartbeat. If heartbeat signals collision, then collision is guaranteed to remain for 8 TCLKs.

WATCHDOG TIMER

The watchdog timer ensures that the MK5035 will not transmit for more than 101K bit times. The timer is started when TENA goes active. The timer resets when TENA goes inactive. If TENA remains active for more than 101K bit times, then the timer will time-out causing collision to be asserted and $\overline{\text{XEN}}$ to go inactive. If loopback is enabled, watchdog timeout will occur after 325 bit times. This particular timer value allow StarLAN HUBs to activate their own jabber functions, thereby alerting net management.

ECHO TIMER

The MK5035 expects the data that it is transmitting to be received on $\overline{\text{RC}}$/RD within 510 bit times. The echo timer is activated when TENA goes active. If 510 bit times elapse before RENA goes active, then the timer will time out causing collision to be activated.

Oscillator

The MK5035 will accept two forms of clock input: a CMOS input or a crystal. If pin X2 is left unconnected, a 6.0/8.0 MHz $\pm$ 0.01% CMOS clock may be applied to pin X1. Alternately, a crystal circuit may be connected between X1 and X2 to form the basis of an oscillator. Typically, a 6.0/8.0 $\pm$ 0.005% parallel resonant crystal is needed to insure the $\pm$ 0.01% frequency accuracy required for StarLAN. Refer to Figure 4. A fundamental mode, parallel resonance type crystal should be used with the manufacturer's suggested load capacitance.

Reset Input

The reset pin is an active low Schmidt trigger input. A simple RC network may be used to insure correct operation upon power-up. Refer to Fig. 5.

Figure 4. Oscillator Operation

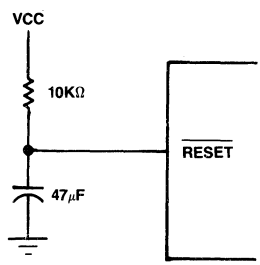


Figure 5. Typical RC Connection For Power-On Reset

ELECTRICAL SPECIFICATIONS

This chapter provides tabular presentations for Absolute Maximum Ratings, DC Characteristics, Capacitance and AC Timing Specifications. In addition, illustrations are provided for an Output Load Diagram (Figure 9) and Station Timing Diagrams.

ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias ..... −25°C to +100°C
Storage Temperature ..... −65°C to +150°C
Voltage on Any Pin with Respect to Ground ..... −0.5 V to V_{CC} +0.5 V
Power Dissipation (no load) 50mW

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = +5 V ±5% unless otherwise specified.

SYMBOL	CONDITIONS	MIN	MAX	UNITS
V_{IL}		−0.5	+0.8	V
V_{IH}	Except X1	+2.0	V_{CC} +0.5	V
V_{IH}	X1	+3.5	V_{CC} +0.5	V
V_{OL}	@ I_{OL} = 3.2 mA, except X2		+0.5	V
V_{OH}	@ I_{OH} = −0.4 mA, except X2	+2.4		V
V_{OH}	@ I_{OH} = −40 μA, except X2	+3.2		V
I_{IL}	@ V_{IN} = 0.4 to V_{CC}		±10	μA
I_{CC}			8	mA

CAPACITANCE

F = 1 MHz

SYMBOL	CONDITIONS	MIN	MAX	UNITS
C_{IN}			10	pf
C_{OUT}			10	pf
C_{IO}			20	pf

AC TIMING SPECIFICATIONS

T_A = 0°C to 70°C, V_{CC} = +5 V ±5% unless otherwise specified, V_{TH} = 2.0 V, V_{TL} = 0.8 V.

#	SIGNAL	SYMBOL	PARAMETER	MIN ns	TYP ns	MAX ns
1	X1	T_{X1T}	X1 period	62		
2	X1	T_{X1L}	X1 low time	24		
3	X1	T_{X1H}	X1 high time	24		
4	X1	T_{X1R}	Rise time of X1	0		8
5	X1	T_{X1F}	Fall time of X1	0		8

AC TIMING SPECIFICATIONS (cont.)

T_A = 0°C to 70°C, V_{CC} = +5 V ±5% unless otherwise specified, V_{TH} = 2.0 V, V_{TL} = 0.8 V.

#	SIGNAL	SYMBOL	PARAMETER	MIN ns	TYP ns	MAX ns
6	$\overline{XEN}$	$T_{\overline{XEN}}$	$\overline{XEN}$ delay from X1		40	65
7	XD	T_{XD}	XD delay from X1		40	65
8	XD	J_{XD}	Transmit jitter $\lvert T_{XD}\uparrow - T_{XD}\downarrow \rvert \div 2$		4	6
9	TCLK	T_{CLK}	TCLK delay from X1			70
10	TX	T_{TXST1}	TX setup to falling edge of TCLK, CMODE = 1	90		
11	TX	T_{TXHT1}	TX hold from falling edge of TCLK, CMODE = 1	15		
12	TX	T_{TXS}	TX setup to X1	15		
13	TX	T_{TXH}	TX hold from X1	15		
14	TENA	T_{TNAST1}	TENA setup to falling edge of TCLK, CMODE = 1	90		
15	TENA	T_{TNAST1}	TENA hold from falling edge of TCLK, CMODE = 1	15		
16	TENA	T_{TENAS}	TENA setup to X1	15		
17	TENA	T_{TENAH}	TENA hold from X1	15		
18	TX	T_{TXST0}	TX setup to rising edge of TCLK, CMODE = 0	90		
19	TX	T_{TXHT0}	TX hold from rising edge of TCLK, CMODE = 0	15		
20	TX	T_{TXS}	TX setup to X1, CMODE = 0	15		
21	TX	T_{TXH}	TX hold from X1, CMODE = 0	15		
22	TENA	T_{TNAST0}	TENA setup to positive edge of TCLK, CMODE = 0	90		
23	TENA	T_{TNAHT0}	TENA hold from positive edge of TCLK, CMODE = 0	15		
24	TENA	T_{TNAS}	TENA setup to X1, CMODE = 0	15		
25	TENA	T_{TNAH}	TENA hold from X1, CMODE = 0	15		
26	CLSN	T_{CLSN}	CLSN delay from X1			70
27	$\overline{ECLSN}$	$T_{\overline{ECLSN}}$	Minimum detected pulse width		5	20
28	$\overline{RC}$	$T_{\overline{RCS}}$	$\overline{RC}$ setup to X1	15		
29	$\overline{RC}$	$T_{\overline{RCH}}$	$\overline{RC}$ hold from X1	15		
30	RD	T_{RDS}	RD setup to X1	15		
31	RD	T_{RDH}	RD hold from X1	15		
32	RD	J_{RD6}	RD Incoming Jitter Tolerance, 6X mode, X1 = 6 MHz, $T_{X1T} - \lvert T_{RDS}\uparrow - T_{RDS}\downarrow \rvert$		165	161
33	RD	J_{RD8}	RD Incoming Jitter Tolerance, 8X mode, X1 = 8 MHz, $T_{X1T} - \lvert T_{RDS}\uparrow - T_{RDS}\downarrow \rvert$		123	119
34	RCLK	T_{RCLK}	RCLK delay from X1, CMODE = 1		40	65
35	RX	T_{RXRCK1}	RX delay from falling RCLK, CMODE = 1	−30		30
36	RX	T_{RX}	RX delay from X1, CMODE = 1		40	65
37	RENA	$T_{RNARCK1}$	RENA delay from falling RCLK, CMODE = 1	−30		30
38	RENA	T_{RENA}	RENA delay from X1, CMODE = 1		45	65
39	CLSN	$T_{CSNRCK1}$	CLSN delay from falling edge RCLK, CMODE = 1	−30		30
40	CLSN	T_{CLSN}	CLSN delay from X1, CMODE = 1			70

AC TIMING SPECIFICATIONS (cont.)

T_A = 0°C to 70°C, V_{CC} = +5 V ±5% unless otherwise specified, V_{TH} = 2.0 V, V_{TL} = 0.8 V.

#	SIGNAL	SYMBOL	PARAMETER	MIN ns	TYP ns	MAX ns
41	RCLK	T_{RCLK0}	RCLK delay from X1, CMODE = 0		40	65
42	RCLK	P_{RCLK}	RCLK pulse width, CMODE = 0	T_{X1T} −20		T_{X1T}+20
43	RCLK	T_{RXCLK}	RCLK delay from RX stable, CMODE = 0	T_{X1T} −20		
44	RX	T_{CLKRX}	RX hold from falling edge of RCLK, CMODE = 0	$2*T_{X1T}$−20		
45	RCLK	T_{RNACLK}	RCLK delay from RENA stable, CMODE = 0	T_{X1T} −20		
46	RENA	T_{CLKRNA}	RENA hold from falling edge of RCLK, CMODE = 0	$2*T_{X1T}$−20		
47	RCLK	T_{CSNCLK}	Rising RCLK delay from CLSN stable, CMODE = 0	$2*T_{X1T}$−20		
48	CLSN	T_{CLKCSN}	CLSN delay from rising edge of RCLK, CMODE = 0	T_{X1T} −20		

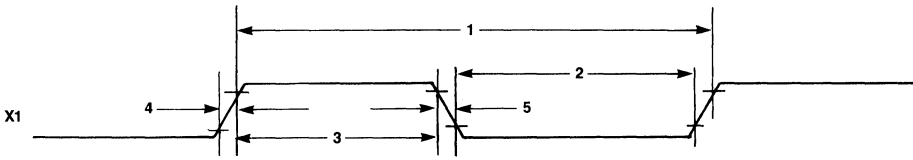


Figure 6. External X1 Timing Diagram

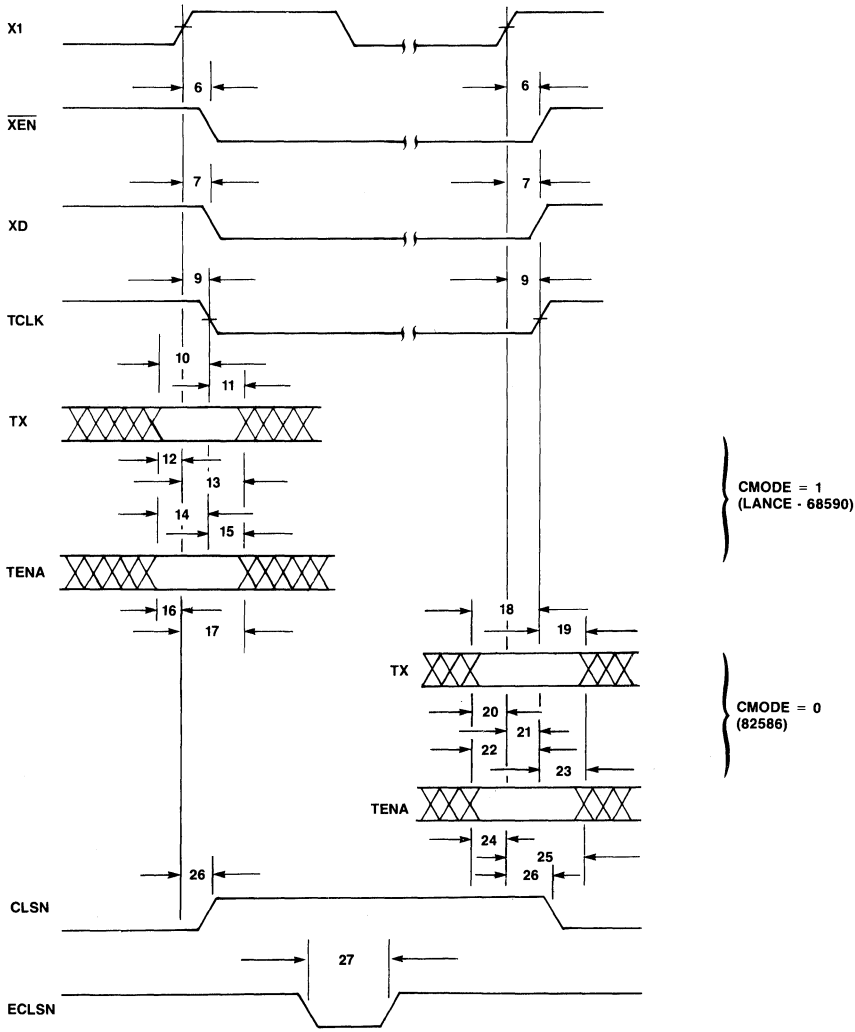


Figure 7. Transmit Timing Diagram

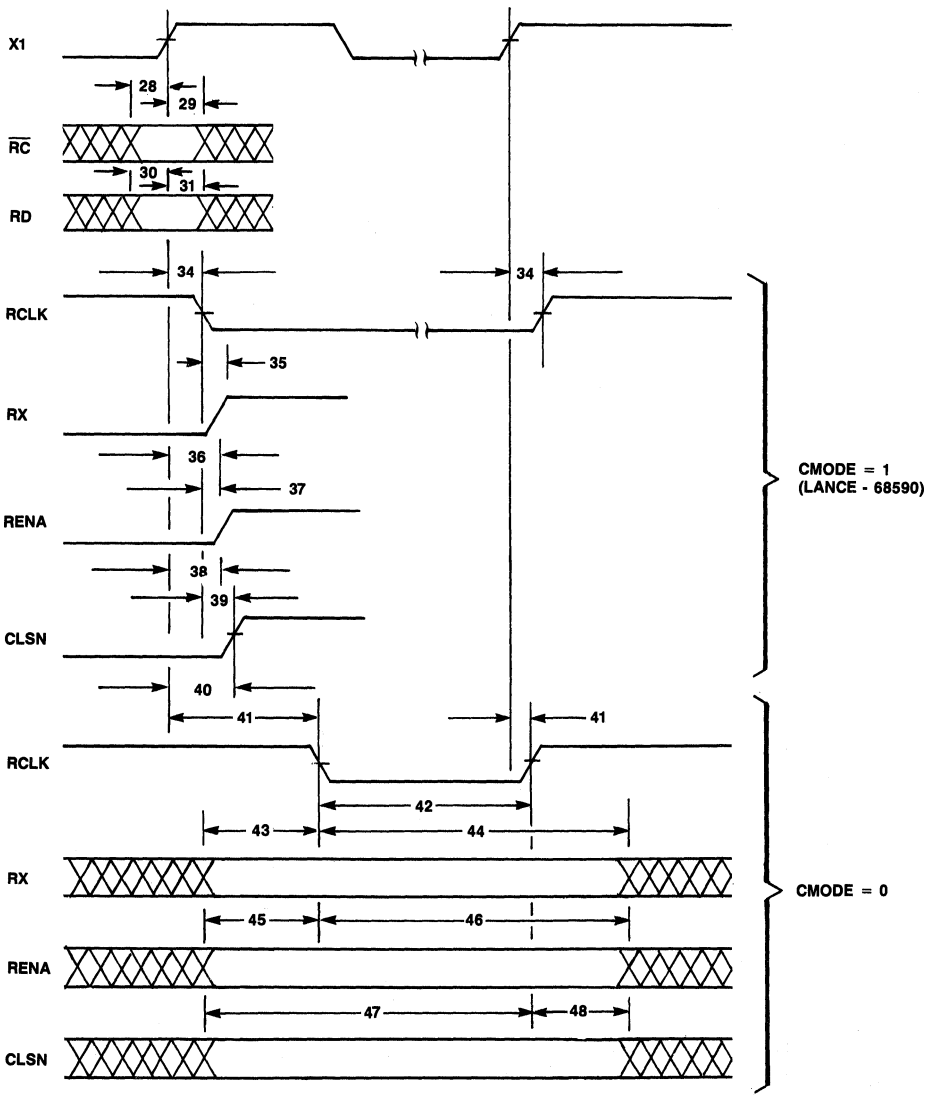


Figure 8. Receiver Timing Diagram

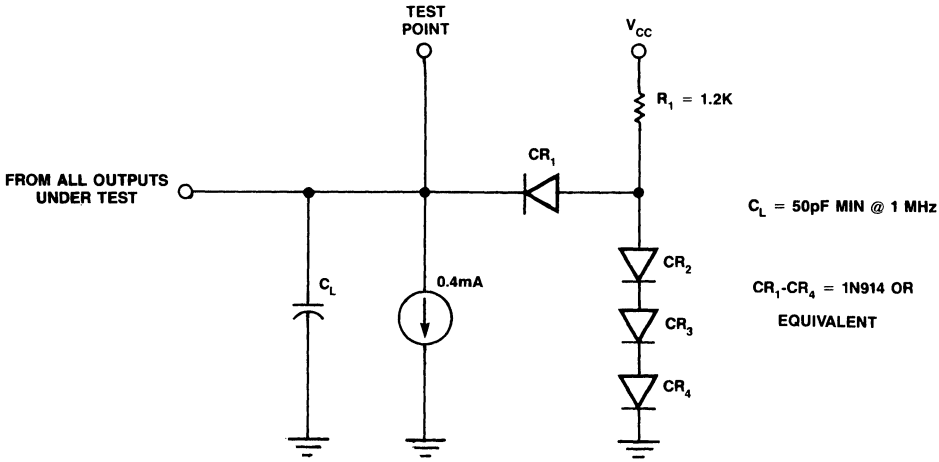
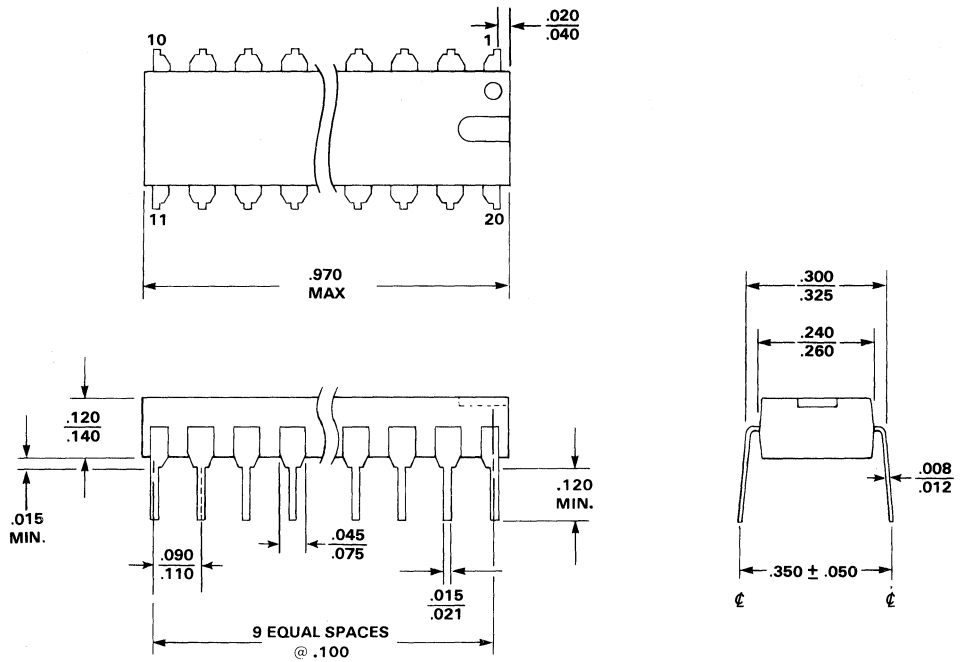


Figure 9. Output Load Diagram

PACKAGE DESCRIPTION
20 Pin Plastic
MK5035N



NOTE: Overall length includes .010 flash on either end of package

THOMSON COMPONENTS
MOSTEK

MK50351N

StarLAN ENCODER DECODER

COMMUNICATIONS PRODUCTS

FEATURES

- ☐ Conforms with StarLAN specification.
- ☐ Supports multi-point extension.
- ☐ Auto compensation for line reversal.
- ☐ Compatible with Mostek MK5032 Variable Bit Rate LANCE and Intel 82586/82588.
- ☐ Close pin compatibility with SEEQ8023.
- ☐ Data rates to 2.66Mbps supported.
- ☐ Manchester data encoding/decoding.
- ☐ Collision detection circuitry with the following features:
  - Detects missing mid-bit transitions
  - Transitions too close together
  - Transitions too far apart
  - External collision input pin
  - Carrier dropout
  - Watchdog timer
  - AT&T Release 1 collision presence signal
  - Echo timeout
- ☐ Receive end-of-frame detection.
  - Input protection at end-of-frame
- ☐ Loopback capability.
- ☐ Receive carrier automatically converted to a level signal.
- ☐ Echo timer to signal error if transmitted frame is not received.
- ☐ Heartbeat generation.
- ☐ In 82586 mode, insensitive to extra bits ahead of preamble
- ☐ Digital phase-locked loop.
- ☐ On chip crystal oscillator, 8X or 10X operation.

*Crystal inputs have CMOS thresholds.

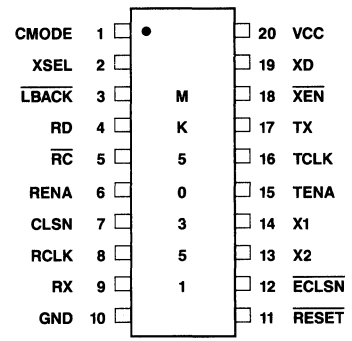


Figure 1. MK50351 Pin Assignment

- ☐ CMOS technology.
- ☐ 20-pin DIP.
- ☐ Single 5-volt supply.
- ☐ All inputs and outputs TTL compatible.*
- ☐ Outputs are also CMOS compatible.
- ☐ Industrial version available.

GENERAL DESCRIPTION

The MK50351 is a Manchester Encoder/Decoder chip incorporating several features that make it an ideal StarLAN station chip. The MK50351 performs three functions. It encodes data from a controller chip into Manchester data. It decodes Manchester data from the line transceiver and produces NRZ data and clock for the controller chip. It also detects collisions and signals the controller chip that a collision has occurred.

The MK50351 has several enhancements for StarLAN and Multi-Point extension (MPE) StarLAN. These include auto compensation for wiring reversal, echo timer, external collision detect, watchdog timer, and heartbeat, among others.

PIN DESCRIPTIONS:

CONTROLLER INTERFACE

RX	Output	RX is the serial receive data after decoding.
RENA	Output	This signal indicates that data is available to the controller on the RX output.
RCLK	Output	RCLK is the receive data clock recovered from the incoming data RD.
TX	Input	TX is the serial data to be transmitted. It is clocked into the chip by TCLK.
TENA	Input	This signal indicates that data is valid on the TX input. It goes active with the first bit of transmission.
TCLK	Output	TCLK is the transmit data clock. All transmit interface signals are synchronized to this clock.
CLSN	Output	This signal is asserted when a manchester violation is detected on the RD line or when the external collision input ($\overline{ECLSN}$) goes active.

TRANSCEIVER INTERFACE

XD	Output	Encoded transmit data output.
$\overline{XEN}$	Output	Transmit output enable. This signal goes low to indicate XD active. It goes high at the end of transmission.
RD	Input	Encoded receive data input.
$\overline{RC}$	Input	Receive carrier input. Receive carrier can be either a pulse stream or an active low signal to indicate carrier active. The chip contains internal squelch circuitry, as shown in Figure 3, to convert a pulse signal to a level signal.
$\overline{ECLSN}$	Input	External collision input. When this pin is held low for at least 20 nS, an external collision is signaled.

OTHER PINS

CMODE Input — This input allows the part to be used with either Mostek or Intel controllers:

CMODE = 0, 82586/82588 (See Note)

Transmit data (TX) is sampled on the rising edge of TCLK.
Receive data (RX) transitions on the rising edge of RCLK.

TENA - active low
RENA - active low - goes active when phase lock loop is locked.
CLSN - active low

CMODE = 1, MOSTEK Variable Bit Rate LANCE MK5032

TENA - active high
RENA - active high - goes active when phase lock loop is locked.
CLSN - active high

$\overline{LBACK}$ Input — When this input is low the part will be put into internal loopback. The transmit data will be internally looped back as receive data. See Figure 2. The outputs XD and $\overline{XEN}$ will be held inactive during loopback.

$\overline{RESET}$ Input — When this pin is low the chip is in reset mode. All interface signals will be inhibited except TCLK. $\overline{RESET}$ should remain active for three TCLK periods.

XSEL Input — This input selects the clock divider.

If XSEL = 0, it is 8X.
If XSEL = 1, it is 10X.

NOTE: Compatibility with controller chips based on preliminary controller data sheets.

X1,X2	Inputs	Crystal oscillator inputs. A crystal can be connected between these inputs, or a CMOS level square wave can be connected to X1 while X2 is left unconnected.	VCC GND	Input	+5V ± 5%

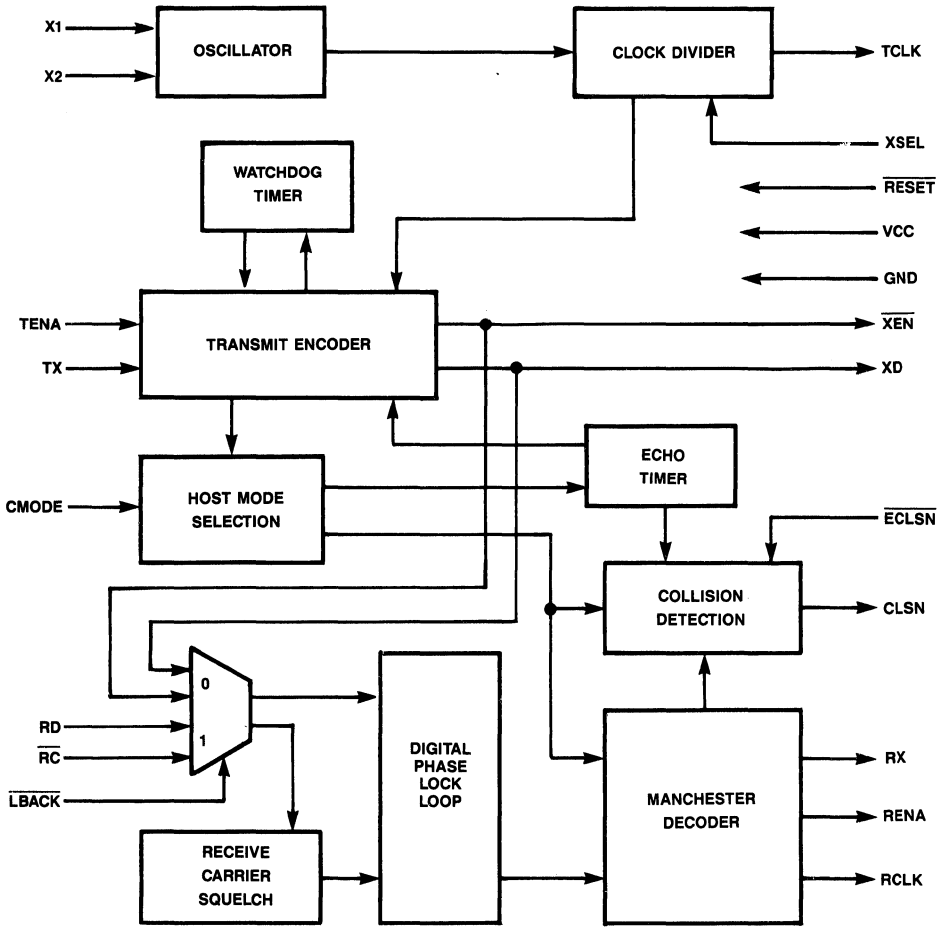
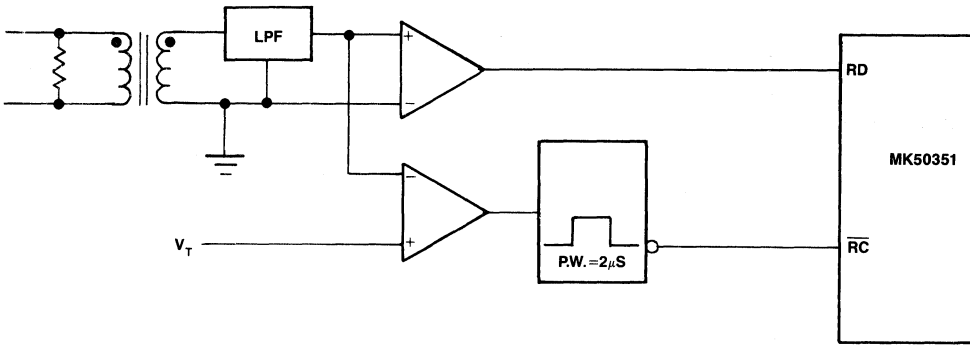
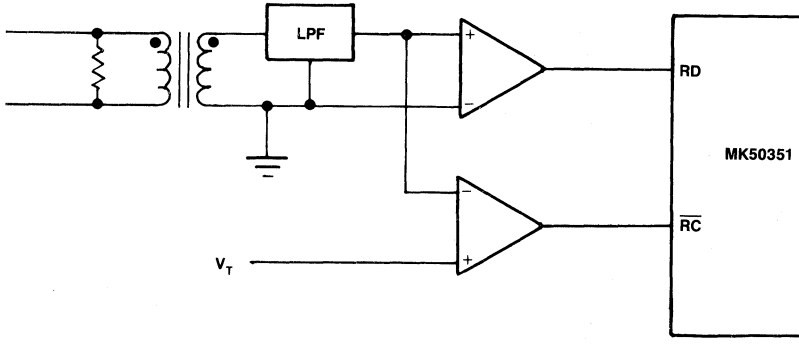


Figure 2. StarLAN Encoder Decoder. MK50351



EXTERNAL SQUELCH



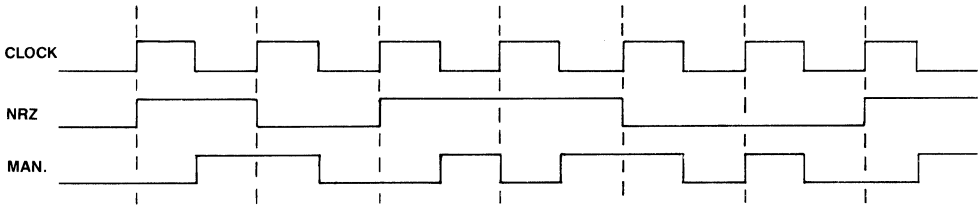
INTERNAL SQUELCH

Figure 3. Internal Versus External Time Squelch

CIRCUIT DESCRIPTION

TRANSMITTER

The transmitter encodes NRZ data from the controller chip into the Manchester data. The diagram below shows the two encoding schemes.



Data encoding and transmission begin when the controller chip brings TENA active. The start of data encoding is delayed by two bits when in 82586/82588 mode. TX is sampled using TCLK as the clock. The encoded data is output on XD. $\overline{XEN}$ goes low with the first bit of data output on XD. The transmit delay, delay from TENA active to $\overline{XEN}$ active, is less than 2 TCLKs. The controller chip signals end of data by bringing TENA inactive.

XD will be held high for an additional 1.5 TCLKs if the last data bit is a one, and for 2 TCLKs if the last data bit is a zero. During this time $\overline{XEN}$ is held active.

RECEIVER

The receiver consists of four major sections.

1) Receive carrier squelch
2) Internal loopback
3) Digital phase locked loop
4) Manchester decoder

The receiver takes Manchester data in on RD, when receive carrier ($\overline{RC}$) is active, and decodes the data into NRZ data and also produces clock (RCLK) from the data. The NRZ data is output to the controller on RX.

RECEIVE CARRIER SQUELCH

The Receive carrier pin has internal squelch logic that allows the signal to be either a level signal or a pulse train. Receive carrier is active low. The receive carrier must be present for 3 clock samples to be considered a valid carrier. Once the carrier is considered valid then it must be active for only one clock sample time every two bit times to remain valid. (See Figure 3.)

Automatic Compensation For Wiring Reversal

When installing twisted pair telephone wiring, it is often difficult and expensive to maintain proper polarity on the wire pairs. The MK50351 will automatically compensate for this reversal. Any frame that is received with inverse polarity will be detected and decoded with the correct polarity.

LOOPBACK

When loopback is enabled ($\overline{LBACK}$ low), RD and $\overline{RC}$ are ignored. Transmit data is internally looped back as receive data. The transmitter outputs XD and $\overline{XEN}$ are disabled during loopback.

DIGITAL PHASE LOCKED LOOP (DPLL)

The digital phase locked loop is implemented with a counter that clears on each transition of the receive data. The phase locked loop will declare "lock" after receiving data that has two "long transitions". A long transition occurs when the receive data does not change for at least 5/8 (7/10 in 10X mode) of a bit time.

MANCHESTER DECODER

The receive data (after inversion if needed) is fed into the decoder along with the recovered 2X clock from the DPLL. The decoder changes the receive data to NRZ data. The NRZ data is output on RX. RENA signals the controller chip that data is available. (See mode pin descriptions.) RCLK is a 1X clock output that is synchronous with the data on RX.

PROTECTION TIME

After the end of a received frame the receiver is disabled for 20 bit times. This protection time guarantees immunity to spikes caused by transformer coupling after the end of frame.

COLLISION

CLSN is an output to the controller chip that indicates a possible problem with the data. There are several sources of collision.

1) Transitions too close together
   Collision is signaled if the receive data stream tran-

sitions a second time in less than 3/8 (3/10 in 10X mode) bit times.

2) Transitions too far apart
Collision is signaled if the receive data stream does not transition again within 10/8 (12/10 in 10X mode) bit times.

3) Manchester violation
If the data violates Manchester coding rules, then collision is signaled.

A Manchester violation is a missing mid-bit transition.

4) Watchdog timer
If the watchdog timer expires, then collision will be signaled.

5) Echo timer
If the echo timer expires without receive carrier going active, then collision will be signaled.

6) External collision
If the external collision pin ($\overline{\text{ECLSN}}$) goes low for at least 20ns, then collision will be signaled.

7) Receive carrier lost during transmission
If the MK50351 is transmitting and the receive carrier goes active and then inactive before it is through transmitting, then collision is signaled.

8) Heartbeat
Collision, as a result of heartbeat, will be signaled 8 TCLKs after TENA goes away, and collision will remain active for at least 8 TCLKs.

Once CLSN is activated it remains active until both TENA and RENA go inactive. The exception to this is heartbeat. If heartbeat signals collision, then collision is guaranteed to remain for 8 TCLKs.

WATCHDOG TIMER

The watchdog timer ensures that the MK50351 will not transmit for more than 101K bit times. The timer is started when TENA goes active. The timer resets when TENA goes inactive. If TENA remains active for more than 101K bit times, then the timer will time-out causing collision to be asserted and $\overline{\text{XEN}}$ to go inactive. If loopback is enabled, watchdog timeout will occur after 325 bit times. This particular timer value allow StarLAN HUBs to activate their own jabber functions, thereby alerting net management.

ECHO TIMER

The MK50351 expects the data that it is transmitting to be received on $\overline{\text{RC}}$/RD within 510 bit times. The echo timer is activated when TENA goes active. If 510 bit times elapse before RENA goes active, then the timer will time out causing collision to be activated.

Oscillator

The MK50351 will accept two forms of clock input: a CMOS input or a crystal. If pin X2 is left unconnected, a 8.0/10.0 MHz $\pm$ 0.01% CMOS clock may be applied to pin X1. Alternately, a crystal circuit may be connected between X1 and X2 to form the basis of an oscillator. Typically, a 8.0/10.0 $\pm$ 0.005% parallel resonant crystal is needed to insure the $\pm$ 0.01% frequency accuracy required for StarLAN. Refer to Figure 4. A fundamental mode, parallel resonance type crystal should be used with the manufacturer's suggested load capacitance.

Reset Input

The reset pin is an active low Schmidt trigger input. A simple RC network may be used to insure correct operation upon power-up. Refer to Fig. 5.

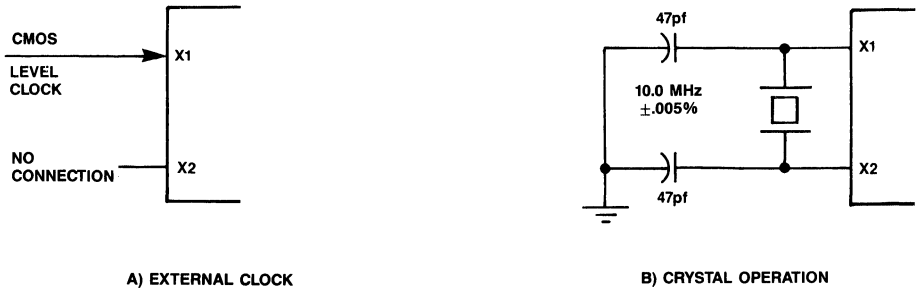


Figure 4. Oscillator Operation

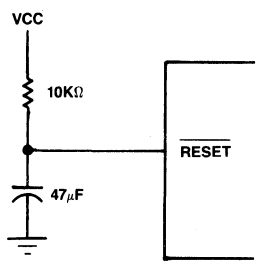


Figure 5. Typical RC Connection For Power-On Reset

ELECTRICAL SPECIFICATIONS

This chapter provides tabular presentations for Absolute Maximum Ratings, DC Characteristics, Capacitance and AC Timing Specifications. In addition, illustrations are provided for an Output Load Diagram (Figure 9) and Station Timing Diagrams.

ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias ..... −25°C to +100°C
Storage Temperature ..... −65°C to +150°C
Voltage on Any Pin with Respect to Ground ..... −0.5 V to V_{CC} +0.5 V
Power Dissipation (no load) 50mW

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = +5 V ±5% unless otherwise specified.

SYMBOL	CONDITIONS	MIN	MAX	UNITS
V_{IL}		−0.5	+0.8	V
V_{IH}	Except X1	+2.0	V_{CC} +0.5	V
V_{IH}	X1	+3.5	V_{CC} +0.5	V
V_{OL}	@ I_{OL} = 3.2 mA, except X2		+0.5	V
V_{OH}	@ I_{OH} = −0.4 mA, except X2	+2.4		V
V_{OH}	@ I_{OH} = −40 μA, except X2	+3.2		V
I_{IL}	@ V_{IN} = 0.4 to V_{CC}		±10	μA
I_{CC}			8	mA

CAPACITANCE

F = 1 MHz

SYMBOL	CONDITIONS	MIN	MAX	UNITS
C_{IN}			10	pf
C_{OUT}			10	pf
C_{IO}			20	pf

AC TIMING SPECIFICATIONS

T_A = 0°C to 70°C, V_{CC} = +5 V ±5% unless otherwise specified, V_{TH} = 2.0 V, V_{TL} = 0.8 V.

#	SIGNAL	SYMBOL	PARAMETER	MIN ns	TYP ns	MAX ns
1	X1	T_{X1T}	X1 period	62		
2	X1	T_{X1L}	X1 low time	24		
3	X1	T_{X1H}	X1 high time	24		
4	X1	T_{X1R}	Rise time of X1	0		8
5	X1	T_{X1F}	Fall time of X1	0		8

AC TIMING SPECIFICATIONS (cont.)

T_A = 0°C to 70°C, V_{CC} = +5 V ±5% unless otherwise specified, V_{TH} = 2.0 V, V_{TL} = 0.8 V.

#	SIGNAL	SYMBOL	PARAMETER	MIN ns	TYP ns	MAX ns
6	$\overline{XEN}$	$T_{\overline{XEN}}$	$\overline{XEN}$ delay from X1		40	65
7	XD	T_{XD}	XD delay from X1		40	65
8	XD	J_{XD}	Transmit jitter $\lvert T_{XD}\uparrow - T_{XD}\downarrow \rvert \div 2$		4	6
9	TCLK	T_{CLK}	TCLK delay from X1			70
10	TX	T_{TXST1}	TX setup to falling edge of TCLK, CMODE = 1	90		
11	TX	T_{TXHT1}	TX hold from falling edge of TCLK, CMODE = 1	15		
12	TX	T_{TXS}	TX setup to X1	15		
13	TX	T_{TXH}	TX hold from X1	15		
14	TENA	T_{TNAST1}	TENA setup to falling edge of TCLK, CMODE = 1	90		
15	TENA	T_{TNAST1}	TENA hold from falling edge of TCLK, CMODE = 1	15		
16	TENA	T_{TENAS}	TENA setup to X1	15		
17	TENA	T_{TENAH}	TENA hold from X1	15		
18	TX	T_{TXST0}	TX setup to rising edge of TCLK, CMODE = 0	90		
19	TX	T_{TXHT0}	TX hold from rising edge of TCLK, CMODE = 0	15		
20	TX	T_{TXS}	TX setup to X1, CMODE = 0	15		
21	TX	T_{TXH}	TX hold from X1, CMODE = 0	15		
22	TENA	T_{TNAST0}	TENA setup to positive edge of TCLK, CMODE = 0	90		
23	TENA	T_{TNAHT0}	TENA hold from positive edge of TCLK, CMODE = 0	15		
24	TENA	T_{TNAS}	TENA setup to X1, CMODE = 0	15		
25	TENA	T_{TNAH}	TENA hold from X1, CMODE = 0	15		
26	CLSN	T_{CLSN}	CLSN delay from X1			70
27	$\overline{ECLSN}$	$T_{\overline{ECLSN}}$	Minimum detected pulse width		5	20
28	$\overline{RC}$	$T_{\overline{RCS}}$	$\overline{RC}$ setup to X1	15		
29	$\overline{RC}$	$T_{\overline{RCH}}$	$\overline{RC}$ hold from X1	15		
30	RD	T_{RDS}	RD setup to X1	15		
31	RD	T_{RDH}	RD hold from X1	15		
32	RD	J_{RD6}	RD Incoming Jitter Tolerance, 8X mode, X1 = 8 MHz, $T_{X1T} - \lvert T_{RDS}\uparrow - T_{RDS}\downarrow \rvert$		123	119
33	RD	J_{RD8}	RD Incoming Jitter Tolerance, 10X mode, X1 = 10 MHz, $T_{X1T} - \lvert T_{RDS}\uparrow - T_{RDS}\downarrow \rvert$		198	194
34	RCLK	T_{RCLK}	RCLK delay from X1, CMODE = 1		40	65
35	TX	T_{RXRCK1}	RX delay from falling RCLK, CMODE = 1	−30		30
36	RX	T_{RX}	RX delay from X1, CMODE = 1		40	65
37	RENA	$T_{RNARCK1}$	RENA delay from falling RCLK, CMODE = 1	−30		30
38	RENA	T_{RENA}	RENA delay from X1, CMODE = 1		45	65
39	CLSN	$T_{CSNRCK1}$	CLSN delay from falling edge RCLK, CMODE = 1	−30		30
40	CLSN	T_{CLSN}	CLSN delay from X1, CMODE = 1			70

AC TIMING SPECIFICATIONS (cont.)

T_A = 0°C to 70°C, V_{CC} = +5 V ±5% unless otherwise specified, V_{TH} = 2.0 V, V_{TL} = 0.8 V.

#	SIGNAL	SYMBOL	PARAMETER	MIN ns	TYP ns	MAX ns
41	RCLK	T_{RCLK0}	RCLK delay from X1, CMODE = 0		40	65
42	RCLK	P_{RCLK}	RCLK pulse width, CMODE = 0	T_{X1T} −20		T_{X1T}+20
43	RCLK	T_{RXCLK}	RCLK delay from RX stable, CMODE = 0	T_{X1T} −20		
44	RX	T_{CLKRX}	RX hold from falling edge of RCLK, CMODE = 0	2*T_{X1T}−20		
45	RCLK	T_{RNACLK}	RCLK delay from RENA stable, CMODE = 0	T_{X1T} −20		
46	RENA	T_{CLKRNA}	RENA hold from falling edge of RCLK, CMODE = 0	2*T_{X1T}−20		
47	RCLK	T_{CSNCLK}	Rising RCLK delay from CLSN stable, CMODE = 0	2*T_{X1T}−20		
48	CLSN	T_{CLKCSN}	CLSN delay from rising edge of RCLK, CMODE = 0	T_{X1T} −20		

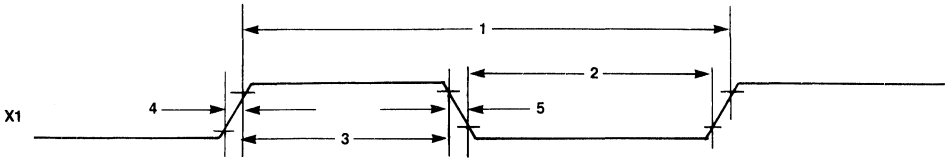


Figure 6. External X1 Timing Diagram

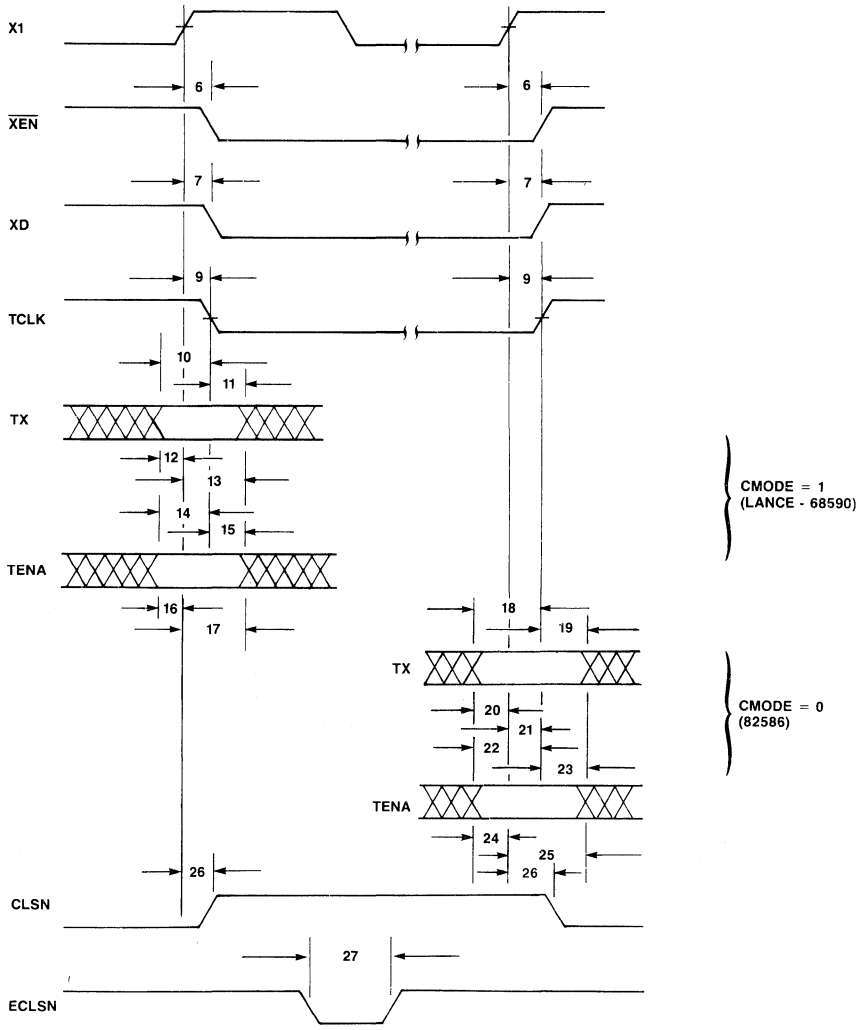


Figure 7. Transmit Timing Diagram

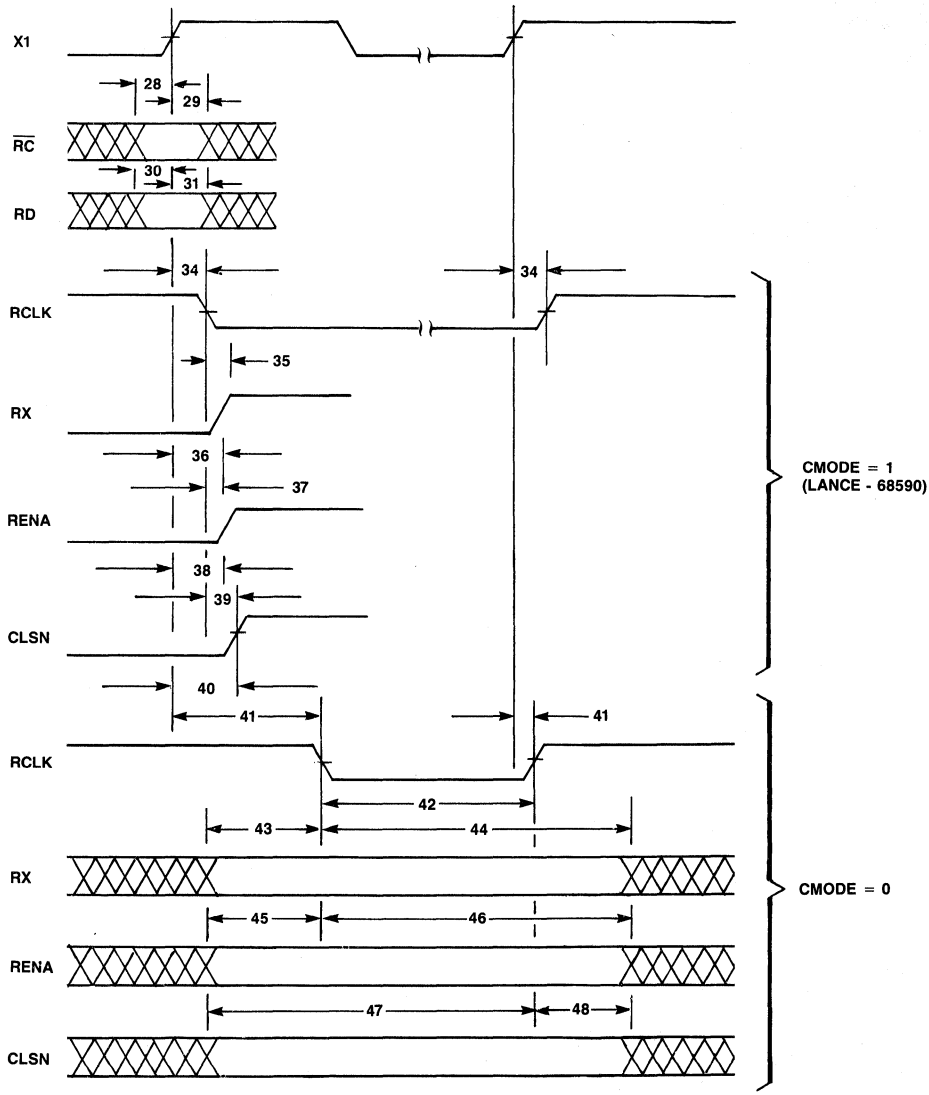


Figure 8. Receiver Timing Diagram

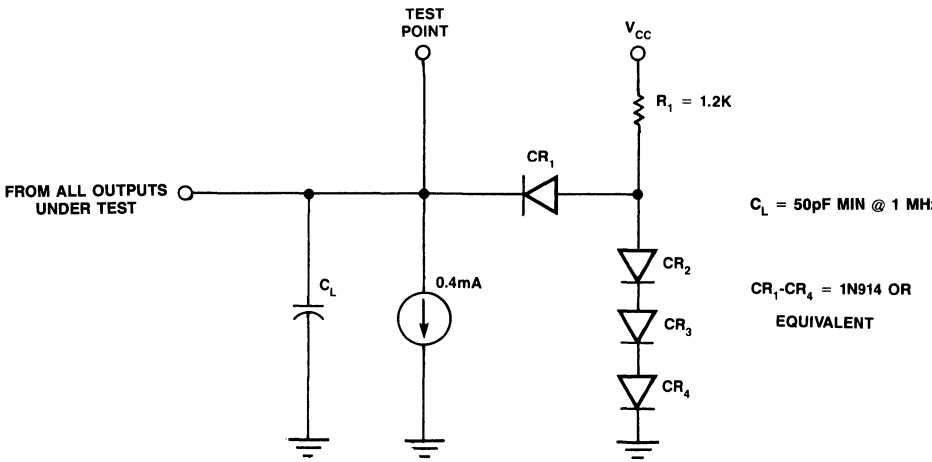
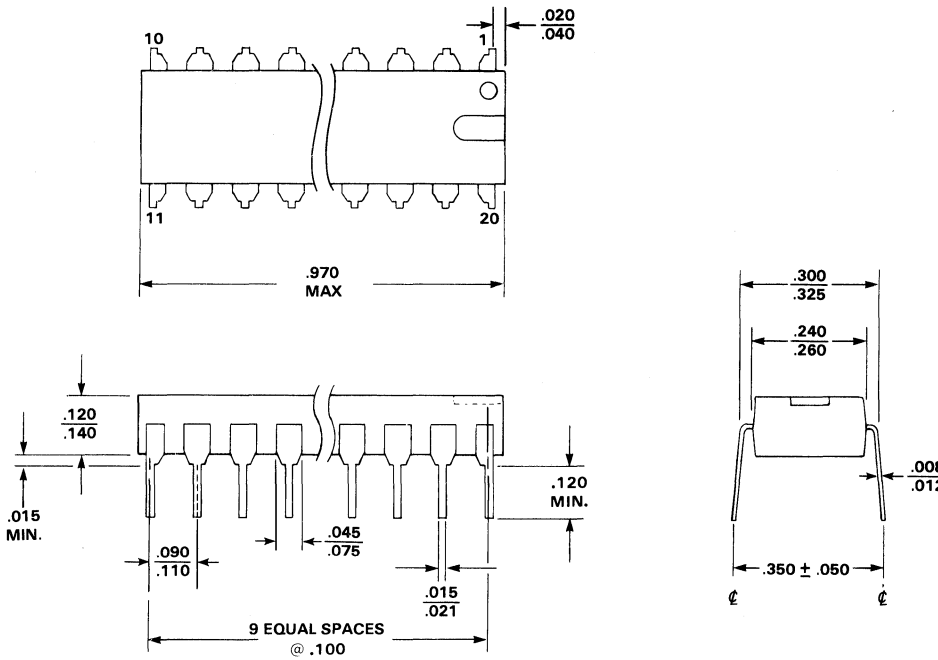


Figure 9. Output Load Diagram

PACKAGE DESCRIPTION
20 Pin Plastic
MK50351N



NOTE: Overall length includes .010 flash on either end of package

CHAPTER 2 - MODEM ICs

THOMSON COMPONENTS MOSTEK

TSG7515

SINGLE CHIP DPSK AND FSK MODEM

SINGLE CHIP DPSK AND FSK MODEM (BELL 212A - BELL 103 - V22 A/B)

The TSG7515 is a single chip DPSK and FSK voiceband modem, compatible with the applicable BELL and CCITT recommended standards for 212A sets including BELL 103 and V22 A-B type modems.

- Monolithic device includes both transmit and receive filters.
- Mixing analog and digital technics.
- Standard low cost crystal (4.9152 MHz).
- Available clock for microprocessor at 4.9152 MHz.
- Low power consumption - CMOS technology.
- Sharp adjacent channel rejection.
- Fixed equalization in transmitter and receiver.
- Test loops.
- Carrier detect output.
- CCITT and BELL signaling tone.
- 1200 bps and 600 bps bit synchronous format in DPSK.
- 1200 bps and 600 bps +1%, −2.5% or +2.3%, −2.5% character asynchronous format (8, 9, 10 or 11 bits) in DPSK.
- 0 to 300 bps in FSK.
- Break signal supervision.
- External voice band tone filtering available (i.e. 550 Hz or DTMF).
- CMOS and TTL compatible.
- Direct interface to THOMSON SEMICONDUCTEURS microprocessor family.
- Special line monitoring facility.

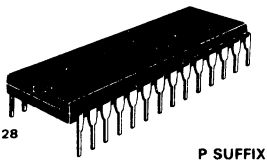
MAIN OPERATING MODES

- Standard selection (BELL 212A/BELL 103/V22).
- Answer tone selection.
- Low speed mode selection.
- Channel selection (Answer/Originate).
- Synchronous/Asynchronous mode selection.
- 8 bits to 11 bits word length selection in character asynchronous format mode.
- Overspeed selection in character asynchronous format mode.
- Scrambler selection.
- 1800 Hz guard tone selection in V22.
- Test loop selection (Digital/Analog).

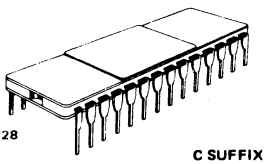
CMOS

SINGLE CHIP DPSK AND FSK MODEM

CASE CB-132

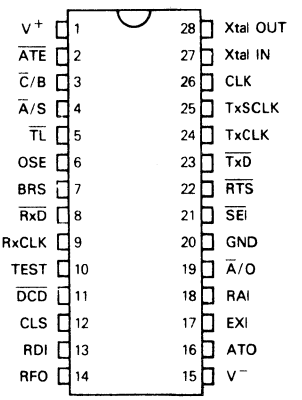


P SUFFIX
PLASTIC PACKAGE

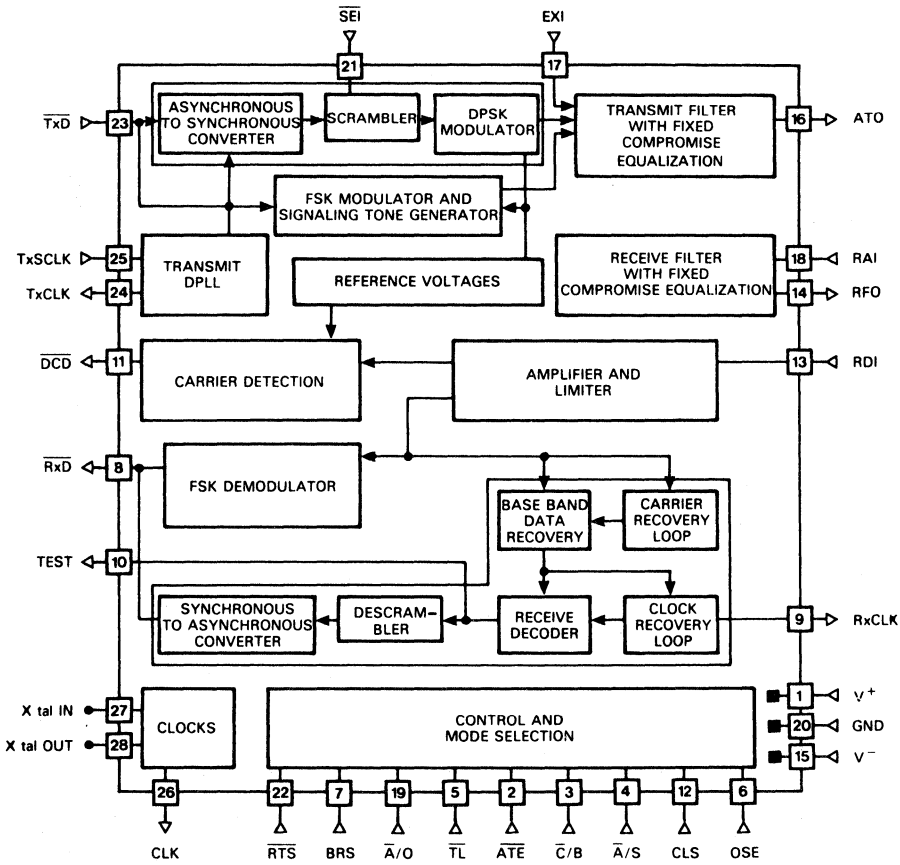


C SUFFIX
CERAMIC PACKAGE

PIN ASSIGNMENT



BLOCK DIAGRAM



PIN DESCRIPTION

Common section (supply, clock, handshaking and mode selection)

Name	Pin Type	No	Function	Description
V^+	I	1	Positive power supply	+5 V
V^-	I	15	Negative power supply	−5 V
GND	I	20	Ground	0 V
XIN	I	27	Oscillator input	This pin corresponds to the input of the oscillator. It is normally connected to an external crystal but may also be connected to a pulse generator. The nominal frequency of the oscillator is 4.9152 MHz.
XOUT	O	28	Oscillator output	This pin corresponds to the output of an inverter with sufficient loop gain to start and maintain the crystal oscillating.
CLK	O	26	Clock	This pin delivers a clock signal, the frequency of which is the crystal frequency. It may be used as a buffered clock for a microcontroller.
$\overline{C}$/B	I	3	CCITT/BELL selection	This three-state input selects the features corresponding to CCITT or BELL recommandation.
$\overline{A}$/S	I	4	Synchronous/ asynchronous selection	This three-state input selects the synchronous bit format or the asynchronous character format mode in DPSK transmission. This input allows also character length selection (refer to table 8).
CLS	I	12	Character length	This input selects the character length in conjunction with $\overline{A}$/S input (refer to table 8).
OSE	I	6	Over-speed selection	This input selects the over-speed in asynchronous character format mode required by CCITT recommandation (refer to table 8).
BRS	I	7	Binary rate selection	A logic "0" on this input turns the chip on 1200 bps rate. A logic "1" turns the chip on 600 bps or 0-300 bps according to $\overline{C}$/B selection.
$\overline{A}$/O	I	19	Answ./Orig. selection	A logic "0" on this input turns the chip on answer mode. A logic "1" turns the chip on originate mode.
$\overline{TL}$	I	5	Test loop selection	This three-state input, selects the test loops mode (refer to table 5).

Transmit section

Name	Pin Type	No	Function	Description
$\overline{TxD}$	I	23	Transmit data	Data bits to be transmitted are serially presented on this input. A mark corresponds to a logic "1" and a space to a logic "0". This data determines which phase or frequency appears at any instant at the ATO pin in DPSK or FSK modes.
ATO	O	16	Analog transmit output	The analog output is the modulated carrier or the answer tone to be conditionned and sent over the phone line mixed with the filtered signal from EXI.
EXI	I	17	External tone input	This analog input allows external tone to be filtered by an internal low-pass filter. Filtered signal appears at ATO whatever RTS.
$\overline{ATE}$	I	2	Answer tone enable	A logic "0" on this input instructs the chip to enter answer signaling tone mode according C/B selection. A logic "1" turns the chip on transmit data mode (refer to table 9).
$\overline{SEI}$	I	21	Scrambler enable input	A logic "0" on this input enables the internal scrambler. A logic "1" instructs the chip to bypass the scrambler.
TxCLK	O	24	Transmit clock from modem	This output delivers a transmit bit clock generated by the chip in synchronous mode. When TxSCLK is used, TxCLK is locked on TxSCLK. This output generates a logic "1" in asynchronous mode.
TxSCLK	I	25	Transmit clock from terminal	This input receives a bit clock supplied by the DTE. This clock synchronizes the internal transmit clock of the chip. In line monitoring mode this input receives the filters clock.
$\overline{RTS}$	I	22	Request to send terminal	When a logic "0" is present on this input, the chip delivers on ATO a modulated signal or a signaling tone and the filtered signal from EXI. When a logic "1" is present on this input, ATO delivers only the filtered signal from EXI. When a logic "-1" is present on this input, the receive section may be used for line monitoring and ATO delivers only the filtered signal from EXI.

Receive section

Name	Pin Type	No	Function	Description
RAI	I	18	Receive analog input	This input receives the analog signal from the hybrid. It corresponds to the input of the receive filters.
RFO	O	14	Receive filter output	This analog output is the signal received on RAI once filtered. The receive filter also equalizes the signal for adaptation to most existing lines. This output must be connected to RDI through a capacitor to meet the level detection conditions.
RDI	I	13	Receive demodulator input	This pin is the input of the carrier detection logic and of the demodulator.
$\overline{DCD}$	O	11	Data carrier detect	A logic "0" on this output indicates that a valid carrier signal is present on RAI. A logic "1" means that no valid signal is being received. The hysteresis meet standards recommendation.
$\overline{RxD}$	O	8	Receive data	Data bits demodulated are available serially at this output.
RxCLK	O	9	Receive clock	This output delivers a receive bit clock generated by the chip. In asynchronous mode this clock is 16 times the modulation rate. In synchronous mode the clock is equal to the bit rate.
TEST	O	10	Test	This output is an intermediate demodulator output intented for handshake and test purposes.

GENERAL DESCRIPTION

The TSG7515 is a general purpose monolithic DPSK and FSK modem implemented with double poly CMOS process. It is capable of generating and receiving phase modulated signals at data rates of 1200 bps or 600 bps as well as frequency modulated signals at data rates up to 300 bps on voice-grade telephone lines. It is offered in a 28 pin package capable of operating full-duplex according to three pin selectable standards :

- CCITT V22 A-B.
- Bell 212A with its low speed mode;
- Bell 103.

All filtering functions required for frequency generation, out-of-band noise rejection and demodulation are performed by on-chip switched capacitor filters. In phase modulation the modem provides all data buffering and scrambling functions necessary for bit synchronous format and asynchronous character format modes of operation. Internal frequencies are generated from a 4.9152 MHz crystal reference.

FUNCTIONAL DESCRIPTION

TRANSMITTER

The transmitter consists of two analog signal generators followed by switched capacitor and continuous filters. In phase modulation operation mode the DPSK signal generator is preceded by a selectable scrambler and an asynchronous to synchronous converter is included in character asynchronous format mode.

Tone allocation: the modem on the end of the line which initiates the call is called the originate modem. In normal transmission operation it transmits in low channel and receives in high channel. The other modem is the answer modem which transmits in high channel and receives in low channel.

Modulators

DPSK modulator: the phase modulation type is differential quadrature four phase shift keying (see table 1). The 1200 bps data stream to be transmitted is converted into two 300 dibits per second streams which modulate alternatively two independant carriers. Consequently the base band shaping is included is a 5 bit address ROM which generates samples for a 8 bit switched capacitor DAC at a frequency equals to 8 times the carrier frequency.

BRS	$\overline{TxD}$		Phase shift
	n-1	n	
0	0	0	+90°
		1	0°
	1	0	+270°
		1	+180°
1		0	+90°
		1	+270°

Table 1: DPSK modulation

FSK modulator and tone generator: a frequency synthesizer provides accurate clocks to a switched capacitor sine wave generator (see table 2). Phase continuity is maintained when a frequency shift occurs.

$\overline{A}$/O	$\overline{TxD}$	Standard frequency
0	0	2025 Hz
	1	2225 Hz
1	0	1070 Hz
	1	1270 Hz

Table 2: FSK modulation (BELL 103)

Transmit filters

To avoid unwanted frequency components to be echoed by the hybrid in the reception path, to maintain the level of spurious out-of-band signals transmitted to the telephone line below the limits specified by administrations (see figure below) and to complete statistical amplitude and phase equalization, the analog signals are processed by ten poles sharp pass-band switched capacitor filters. The response of these filters depends on the selected channel (Answer/Originate) and the selected standard (BELL 212-V22/BELL 103). A continuous filter eliminates parasitic sampling effects. An additional low-pass filter input is provided. This allows to mix and filter such tones as DTMF signals or special guard tones (550 Hz) to the transmitted signal.

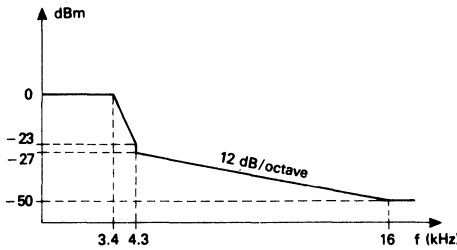


Figure 1 : Transmitted signal template

Scrambler

The scrambler used during phase modulation ensures the transmission of a continuously changing pattern. This avoids the receiving modem to drop out of lock on certain continuous repetitious data patterns. This scrambler may be disabled during handshaking procedures. In V22 a special unlocking sequence is performed on 64 spaces pattern at scrambler output.

Asynchronous to synchronous converter

The DPSK signal is synchronous in nature but the modem has both an asynchronous as well as a synchronous mode of operation in DPSK. So a data buffer is necessary to convert variable rate asynchronous character data to an equivalent bit oriented synchronous data stream. This is done by inserting or deleting stop bits. In addition this converter is able to recognize and format the break signal.

Standard frequency	Frequency using 4.91 MHz	% deviation from standard	Mode
1070 Hz	1066.7 Hz	-0.3%	BELL 103 Originate
1200 Hz	1200 Hz		BELL 212A or V22, Originate
1270 Hz	1269.4 Hz	-0.05%	BELL 103 Originate
1800 Hz	1807.1 Hz	+0.4%	Guard tone V22
2025 Hz	2021 Hz	-0.2%	BELL 103 Answer
2100 Hz	2104.1 Hz	+0.2%	Answer tone CCITT
2225 Hz	2226.1 Hz	+0.05%	BELL 103 Answer or Answer tone BELL
2400 Hz	2400 Hz		BELL 212A or V22, Answer

Table 3: Output frequency deviation

RECEIVER

The receiver includes two band-pass filters followed by an amplifier and a hard limiter. Depending on selected standard, the detector output is passed through a DPSK demodulator or a FSK demodulator. The DPSK demodulator is followed by a descrambler and a selectable synchronous to asynchronous converter. In addition a carrier detector monitors the level of the received signal.

Tone allocation: in normal transmission operation the originate modem receives in high channel and transmits in low channel. The answer modem receives in low channel and transmits in high channel.

Receive filters

The signal delivered by the hybrid to the receive analog input is a mixture of transmitted signal, received signal and noise with a level in the range from —48 dBm to —0 dBm. Depending on the operating mode and the selected standard the 20 poles receive switched capacitor band-pass filter selects the frequency band of the low channel or the high channel. A ratio of 14/15 is applied on the sampling clock frequency between FSK and DPSK in the same operating mode (Answer/Originate). These filters reject out-of-band transmission noise components and undesirable adjacent channel echo signals which can be fed from the transmit section into the receive section. Fixed equalization is included in order to assure low error rate.

Amplifier and hard limiter

Once filtered the received signal is amplified and fed to the carrier detector. In order to limit analog parts in the design all the demodulator techniques used in the TSG7515 are based on zero crossing detection. So the received signal is just limited before entering demodulator.

Demodulators

DPSK demodulator: a DPLL is used to recover the carrier signal. This DPLL has a lock range of ±2 Hz but as the incoming carrier may present an offset of ±7 Hz a second loop allows the first DPLL to lock on the exact frequency of the carrier with an accuracy of ±1 Hz and to follow its slow variations. Then the limited received signal is mixed through exclusive-Or with the recovered carrier and with the 90 degrees phase shifted recovered carrier. The results are processed through four poles Bessel filters which provide a good amplitude propagation time compromise. The received sampling clock is recovered from these base band data with a simple DPLL. The received data are sampled by this clock and then converted into a serial synchronous bit stream.

FSK demodulator: the zero crossing detector output is passed through a shift register whose length depends on the operating mode (Answer/Originate). The output of the shift register and the detector are mixed into an exclusive-Or. Then they are processed through a four poles Bessel filter and a slicer.

Test output

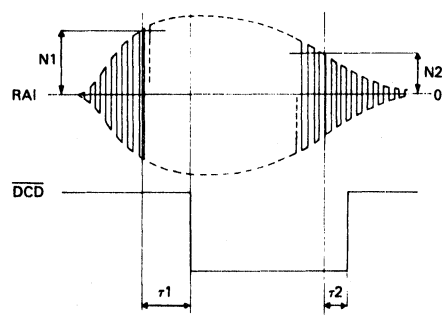
Once demodulated DPSK data are generally processed (cf next paragraph) but during call set-up procedures or data set testing it is of importance to monitor the demodulator output. So in DPSK mode demodulated data are available on TEST pin.

Descrambler and synchronous to asynchronous converter

Data coming from the DPSK demodulator are unscrambled. In V22 the unlocking sequence is detected at descrambler input and the original data are decoded before descrambling. In asynchronous character format mode of operation a data buffer is able to detect missing stop bits and reinsert them. The converter is able to recognize the break signal and transmits it without modification.

Carrier detector

Whenever valid signals are being received at the input of the demodulator and are acceptable for demodulation, carrier detect output is pulled down. A delay is timed out before the carrier received or carrier lost signal changes carrier detect output to provide immunity against noise bursts. The modem also provides at least 2 dB of hysteresis between the carrier ON and the carrier OFF thresholds (see diagram below).



In DPSK mode 105 ms < t1 < 205 ms 10 ms < t2 < 24 ms
In FSK mode 105 ms < t1 < 205 ms 25 ms < t2 < 75 ms

LOOP TESTS

LOOP 3

This loop is called the analog loop. When it is selected the receive filters and the demodulators are configured to process the same channel as the transmit section. The transmit carrier has to be looped back externally to the receive analog input. This loop allows the user or the DTE to check the satisfactory working of the local DCE.

LOOP 2

This loop is called the digital loop. When it is selected received data, receive clock and data carrier detect signals are respectively and internally looped back on transmit data, transmit clock from terminal and request to send. This loop allows the user or the DTE to check the satisfactory working of the line and the remote DCE.

CLOCKS

In synchronous mode of operation TxCLK, TxSCLK and RxCLK are respectively working as the V24 circuits C114, C113 and C115. In asynchronous mode of operation RxCLK can be used as baud rate clock to synchronize the transmit and the receive sections of a UART (see table 4).

OSCILLATOR OUTPUT

The buffered master clock (4.9152 MHz) is made available at output CLK. It can be used as a clock for a microcontroller.

VOLTAGE REFERENCE

A temperature compensated voltage reference build with a zener is included in the chip. This voltage is used to calibrate transmit levels and to generate the carrier detection thresholds.

$\overline{A}$/S	$\overline{C}$/B	BRS	TxCLK	RxCLK	Mode
– 1 ou 0	– 1 ou 0	0	1	19.2 kHz	V22 asynchronous
		1	1	9.6 kHz	
	1	0	1	19.2 kHz	BELL 212A asynchronous and BELL 103
		1	1	4.8 kHz	
1	– 1 ou 0	0	1200 Hz	1200 Hz	V22 synchronous
		1	600 Hz	600 Hz	
	1	0	1200 Hz	1200 Hz	BELL 212A synchronous and BELL 103
		1	1	4.8 kHz	

Table 4: Clocks operation

LINE MONITORING

A special mode has been included in the TSG7515 to monitor the line during an automatic call. When this mode is selected receive filters clock is directly derived from TxSCLK which allows the user to precisely observe broad frequency bands. Furthermore the DCD performs a fast carrier detection equivalent to an envelope detection. As the center frequency of the receive filters is proportional to TxSCLK frequency in this mode it is possible to tune the passband according to the frequencies to be detected (see table 5).

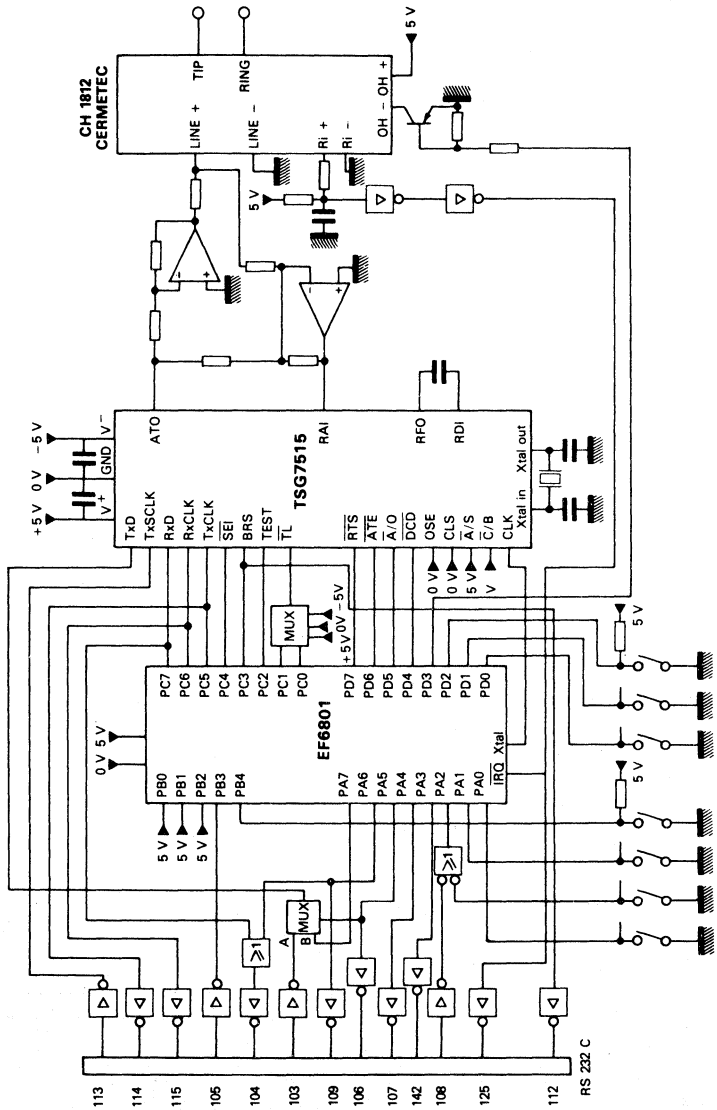
TxSCLK	Originate		Answer		Application
	Center frequency	Passband at 3 dB	Center frequency	Passband at 3 dB	
210 kHz	2400 Hz	±400 Hz	1200 Hz	±400 Hz	Voice detection
45 kHz	510 Hz	±85 Hz			440 Hz detection
			260 Hz	±85 Hz	330 Hz detection
76.8 kHz			440 Hz	±150 Hz	Dial tone and Busy tone detection

Table 5:

APPLICATIONS INFORMATION

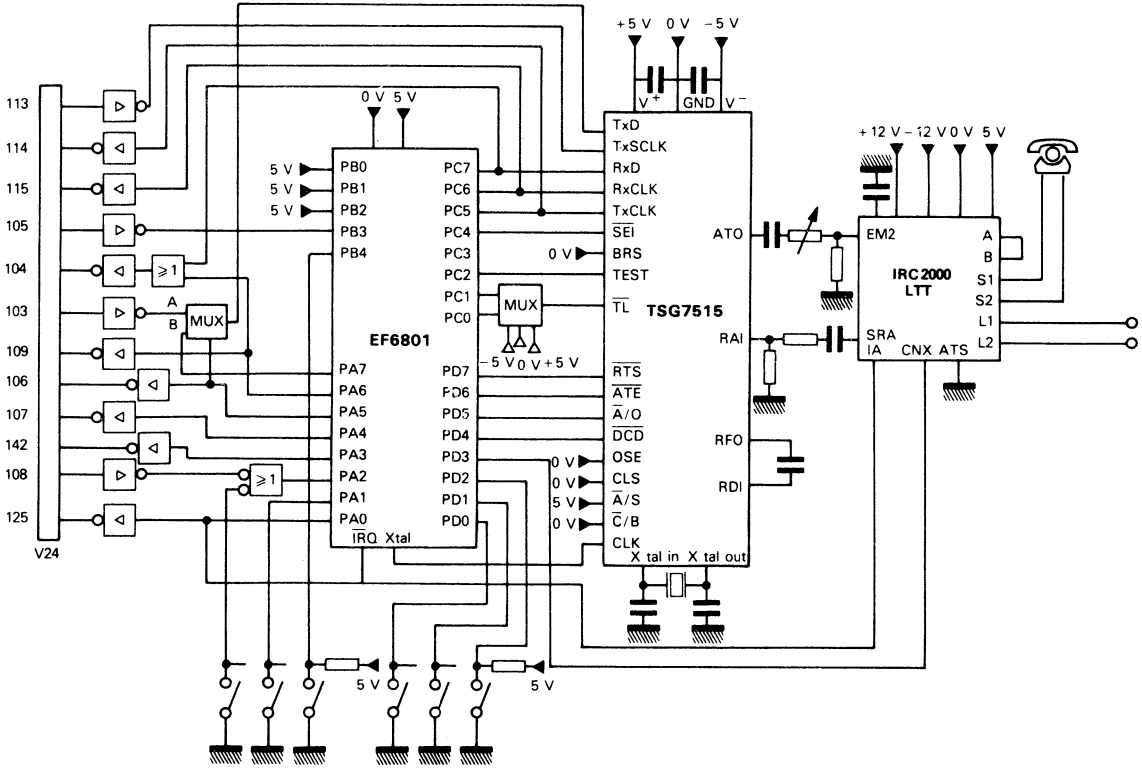
In a typical application a microcontroller provides control and interface to the Data Terminal Equipment (DTE), and a Direct Access Arrangement provides connection to the telephone line. Then the TSG7515 can communicate with the most popular modems (BELL 103 and BELL 212A) in countries under BELL standards and popular modems (V22) in countries under CCITT recommendations.

BELL 212A application :



On this typical application bit synchronous format is selected in high speed mode.

V22 application :



V22A with 1800 Hz and 1200 bps only

POWER SUPPLIES DECOUPLING AND LAYOUT CONSIDERATIONS

Power supplies to digital systems may contain high amplitude spikes and other noise. To optimize performances of the TSG7515 operating in close proximity to digital systems, supply and ground noise should be minimized. This involves attention to power supply design and circuit board layout.

The power supplies should be bypassed with tantalum or electrolytic type capacitors to obtain noise free operation. These capacitors should be located close to the TSG7515. The electrolytic type capacitors should be bypassed with ceramic capacitors for improved high frequency performance.

Power supplies connections should be short and direct. Ground loops should be avoided.

Coupling between analog inputs and digital lines should be minimized by careful layout. The RDI input (pin 13) is extremely sensitive to noise. The connection between this point and RFO (pin 14) through a ceramic type capacitor should be as short as possible and coupling between this connection and digital signals should be minimized by careful layout.

CARRIER RECOVERY LOOP

The carrier recovery loop utilizes a digital phase lock loop. Performances of the TSG7515 depend directly on this DPLL which needs to be resetted before receiving a DPSK carrier.

Three ways of resetting the DPLL exist on the TSG7515:

- A trailing edge on DCD.
- Changing FSK mode to DPSK mode or reversely.
- Changing receive channel.

These three ways of resetting the DPLL should be used in the software included in the microcontroller to perform the various set-up procedures and handshakes.

TYPICAL PERFORMANCES (PRELIMINARY)

The typical performances listed below are achieved with the environment described in the previous paragraph.

- Dynamic range: 0 dBm to -45 dBm.
- BER performances:

  Conditions: Xmit level = -10 dBm,
  Rec level = - 25 dBm,
  Message 511 bits
  on CCETT lines 1, 2, 3, 4
  and CNET lines QN and 3VHF
  and US lines C4, C2 and C0.

  1200 bps operation

  BER $< 10^{-3}$ for a 7 dB SNR
  BER $< 10^{-6}$ for a 11 dB SNR

  300 bps operation

  BER $< 10^{-3}$ for a 3 dB SNR
  BER $< 10^{-6}$ for a 8 dB SNR

- Specific DPSK performances

  Phase hits sensitivity : 25 degree
  Phase Jitter : 35 degree } BER $< 10^{-6}$
  Amplitude hits sensitivity : ±10 dB
  Offset carrier sensitivity : SNR increase $< +1$ dB
  1800 Hz guard tone sensitivity : SNR increase $< +2$ dB

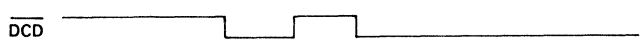
- Specific FSK performances

  Bias Distortion : less than 5%
  Jitter : less than 12%

EXAMPLES

- V22-V25 received signals in Originate mode.

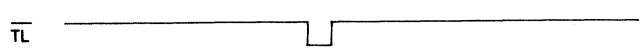
Line ———()()()———[2100 Hz]———[unscrambled marks 2400 Hz][data...



The DPLL is automatically resetted

- Bell 212A received signals in Originate mode.

Line ———( ) ( ) ( )———[2225 Hz] [scrambled marks 2400 Hz][data...



This transition to "-1" is needed to reset the DPLL

SELECTION MODE TABLES

SYNTHESIS OF DIFFERENT MODES FOR RECEIVE SECTION

$\overline{C}$/B	BRS	$\overline{TL}$	$\overline{A}$/0	Receive	Mode
–1 ou 0	X	–1	0	DPSK Originate loop 3	V22
			1	DPSK Answer loop 3	
		0	0	DPSK Answer loop 2	
			1	DPSK Originate loop 2	
		1	0	DPSK Answer	
			1	DPSK Originate	
1	0	–1	0	DPSK Originate loop 3	BELL 212 A including BELL 103
			1	DPSK Answer loop 3	
		0	0	DPSK Answer loop 2	
			1	DPSK Originate loop 2	
		1	0	DPSK Answer	
			1	DPSK Originate	
	1	–1	0	FSK Originate loop 3	
			1	FSK Answer loop 3	
		0	0	FSK Answer loop 2	
			1	FSK Originate loop 2	
		1	0	FSK Answer	
			1	FSK Originate	

Table 6

Answer : Receive in low channel
Originate : Receive in high channel
Loop 3 : Analog loop
Loop 2 : Digital loop

SYNTHESIS OF DIFFERENT MODES FOR TRANSMIT SECTION

$\overline{ATE}$	$\overline{C}$/B	BRS	$\overline{A}$/0	Transmit	Mode
0	–1 ou 0	X	X	2100 Hz	Answer tone
	1			2225 Hz	
1	–1	0	0	DPSK 1200 bps Answer	V22 without guard tone
			1	DPSK 1200 bps Originate	
		1	0	DPSK 600 bps Answer	
			1	DPSK 600 bps Originate	
	0	0	0	DPSK 1200 bps Answer	V22 with 1800 Hz guard tone
			1	DPSK 1200 bps Originate	
		1	0	DPSK 600 bps Answer	
			1	DPSK 600 bps Originate	
	1	0	0	DPSK 1200 bps Answer	BELL 212A
			1	DPSK 1200 bps Originate	
		1	0	FSK 0-300 bps Answer	
			1	FSK 0-300 bps Originate	

Table 7

Answer : Transmit in high channel
Originate : Transmit in low channel

MODE SELECTION IN PHASE MODULATION TRANSMISSION

$\overline{A}$/S	CLS	OSE
-1	0	0
		1
	1	0
		1
0	0	0
		1
	1	0
		1
1	0	0

Transmission mode	length	Over-speed
Asynchronous	8	+1%, -2.5%
		+2.3%, -2,5%
	11	+1%, -2.5%
		+2.3%, -2.5%
	9	+1%, -2.5%
		+2.3%, -2.5%
	10	+1%, -2.5%
		+2.3%, -2.5%
Synchronous		

Table 8

TEST PIN

$\overline{ATE}$	$\overline{C}$/B	BRS	Transmit	Receive	Test
0	-1 ou 0	0	2100 Hz	V22 DPSK 600 bps	DDO
		1		V22 DPSK 1200 bps	DDO
	1	0	2225 Hz	BELL 212A DPSK 1200 bps	DDO
		1		BELL 103 FSK 0-300 bps	HLO
1	-1	0	V22 without guard tone DPSK 1200 bps		DDO
		1	V22 without guard tone DPSK 600 bps		DDO
	0	0	V22 with guard tone DPSK 1200 bps		DDO
		1	V22 with guard tone DPSK 600 bps		DDO
	1	0	BELL 212A DPSK 1200 bps		DDO
		1	BELL 103 FSK 0-300 bps		HLO

Table 9

DDO : DPSK demodulator output
HLO : Hard limiter output

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply voltage	V^+	+7	V
Supply voltage	V^-	-7	V
Analog input range	V_{in}	$V^- < V_{in} < V^+$	V
Digital input range (except three-state inputs)	V_i	$GND < V_i < V^+$	V
Three-state input range	V_{i3}	$V^- < V_{i3} < V^+$	V
Operating temperature range	T_A	0 to 70	°C
Storage temperature range	T_{stg}	-55 to 125	°C
Pin temperature (soldering, 10 s)	T_S	260	°C

Stresses above those listed under "Absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions for extended periods may affect device reliability. Standard CMOS handling procedures should be employed to avoid possible damage to device.

ELECTRIC OPERATING CHARACTERISTICS

Characteristic	Symbol	Min	Nom	Max	Unit
Positive supply voltage	V^+	4.75	5	5.25	V
Negative supply voltage	V^-	-5.25	-5	-4.75	V
V^+ operating current	I^+	–	10	30	mA
V^- operating current	I^-	-20	-7	–	mA

D.C. AND OPERATING CHARACTERISTICS

$T_A = 0°C$ to $+70°C$, $V^+ = +5\ V \pm 5\%$, $V^- = -5\ V \pm 5\%$, GND = 0 V
(Unless otherwise noted)

DIGITAL INTERFACE

Characteristic	Symbol	Min	Typ*	Max	Unit
Input current (V_{IL}min < V_I < V_{IH}max)	I_L	−50	—	50	μA
Output low level current (V_{OL} = 0.4 V)	I_{OL}	800	—	—	μA
Output high level current (V_{OH} = 2.4 V)	I_{OH}	—	—	−40	μA
Input low voltage	V_{IL}	GND	—	0.8	V
Input high voltage	V_{IH}	2	—	V^+	V
Input negative voltage	V_{in}	V^-	—	−4	V

* Typical values are for $T_A = 25°C$ and nominal power supply values

ANALOG INTERFACE, FILTERS INPUTS AND OUTPUTS (RAI-RFO, EXI-ATO)

Characteristic	Symbol	Min	Typ*	Max	Unit
Input leakage current (−3 V < V_{IN} < +3 V)	I_L	−10	—	10	μA
Input resistance	R_I		3	—	MΩ
Input voltage swing	V_{IN}	−3	—	+3	V
Output offset voltage	V_{OF}	−500	—	+500	mV
Output voltage swing (R_L > 10 kΩ)	V_{OS}	−2	—	+2	V
Load capacitance	O_L	—	—	20	pF
Load resistance	R_L	10	—		kΩ
Signal distortion	D		−40		dB

ANALOG INTERFACE, TRANSMIT OUTPUT (ATO)

EXI connected to GND

Characteristic	Symbol	Min	Typ*	Max	Unit
Output offset voltage	V_{OF}	−500	—	+500	mV
Output voltage swing (R_L/ 10 kΩ, C_L = 20 pF) Carriers	V_O	—	2.2	—	V_{pp}
Answer/Originate amplitude ratio	A_R	−1		+1	dB
Guard tone 1800 Hz	V_O	—	1.1	—	V_{pp}
2400 Hz with 1800 Hz	V_O	—	1.9	—	V_{pp}
$\overline{RTS}$ attenuation	A_T	55	—	—	dB

ANALOG INTERFACE, RECEIVE DEMODULATOR INPUT (RDI)

Characteristic	Symbol	Min	Typ*	Max	Unit
Serial capacitor from RFO	Clink**	-1	10	—	μF
Maximum detection level to valid $\overline{DCD}$ output	NI	—	9.8	—	mVp
Minimum detection level to valid $\overline{DCD}$ output	N2	—	13.8	—	mVp
Hysteresis effect	N1/N2	2	—	5	dB

** This capacitor must be unpolarized type capacitor

DYNAMIC CHARACTERISTICS

RECEIVE FILTER TRANSFER CHARACTERISTICS IN DPSK

LOW CHANNEL

Characteristic		Symbol	Min	Typ*	Max	Unit
Absolute passband gain at	1200 Hz	GA	–	+6	–	dB
Relative gain to GA at	600 Hz	GR	–	−45	–	dB
	900 Hz		–	−0.5	–	dB
	1500 Hz		–	+0.8	–	dB
	1800 Hz		–	−50	–	dB
	2400 Hz		–	−65	–	dB

HIGH CHANNEL

Characteristic		Symbol	Min	Typ*	Max	Unit
Absolute passband gain at	2400 Hz	GA	–	+6	–	dB
Relative gain to GA at	2100 Hz	GR	–	−0.2	–	dB
	2700 Hz		–	+0.7	–	dB
	1800 Hz		–	−25	–	dB
	1200 Hz		–	−68	–	dB

RECEIVE FILTER TRANSFER CHARACTERISTICS IN FSK

In FSK the receive filter is the same as in DPSK but the sampling frequency is multiplied by a 14/15 ratio (i.e. 2400 Hz in DPSK becomes 2240 Hz in FSK).

LOW CHANNEL

Characteristic		Symbol	Min	Typ*	Max	Unit
Absolute passband gain at	1120 Hz	GA	–	+6	–	dB

HIGH CHANNEL

Characteristic		Symbol	Min	Typ*	Max	Unit
Absolute passband gain at	2240 Hz	GA	–	+6	–	dB

SUMMARY OF THE DIFFERENCES BETWEEN BELL 212A AND V22 A-B

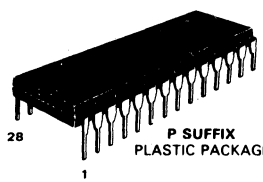
Feature	BELL 212A	V22
Low speed mode	0-300 bps FSK	600 bps DPSK
Guard tone	No	1800 Hz optional*
Answer tone	2225 Hz	2100 Hz
Character length in asynchronous mode in DPSK	9, 10 bits	8, 9, 10, 11 bits**
Over speed mode in asynchronous mode in DPSK	No	Yes**
64 spaces detection	No	Yes

Table 10

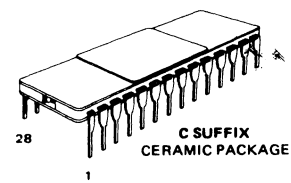
* 550 Hz may be externally generated and added to the transmit signal through EXI.
** Features of V22 are available in BELL 212A on the chip.

All these differences are taken into consideration inside the TSG7515

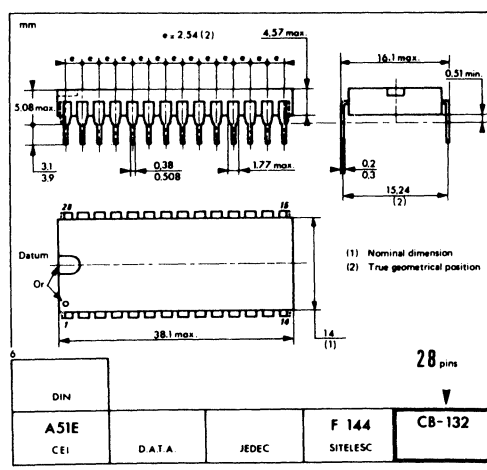
CASE CB-132



P SUFFIX
PLASTIC PACKAGE



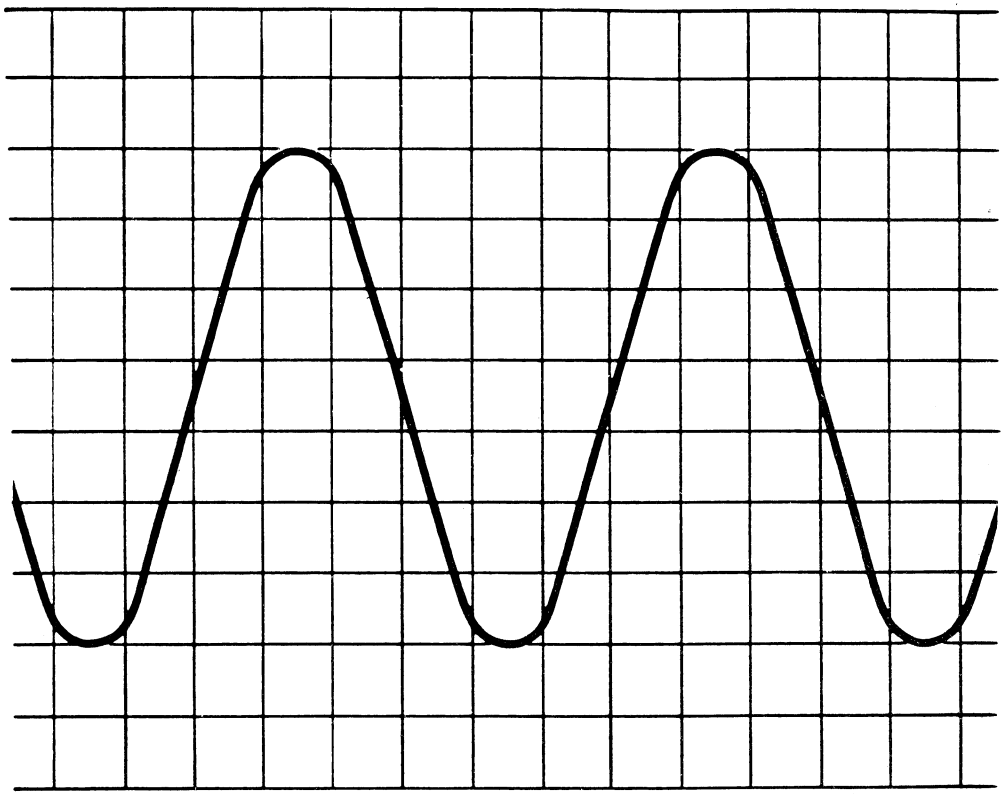
C SUFFIX
CERAMIC PACKAGE



TSG7515

SINGLE-CHIP MULTI-STANDARD DPSK & FSK MODEM

APPLICATION NOTE



APPLICATION NOTE AN-

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MOSTEK

214/466-6000
Telex 730643

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CHAPTER 1 - MAIN CHARACTERISTICS OF TSG 7515

1.1 - General Features

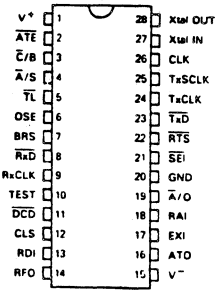
TSG 7515 is a mono chip voice-band modem compatible with BELL 212A, CCITT V.22 A and B standard requirements.

- Includes both Receive and Transmit Filters.
- Designed using analog and digital techniques.
- Requires standard 4.9152 MHz crystal oscillator.
- Buffered clock output for microprocessor-based applications.
- Low power consumption - CMOS technology.
- High adjacent channel signal rejection.
- Fixed equalization in transmission and reception.
- Maintenance loop : type 2 and 3.
- Carrier detect output.
- CCITT and BELL answer tones.
- 1200 and 600 bps synchronous operation in DPSK mode.
- 1200 and 600 bps +1%, -2.5% or +2.3%, -2.5% asynchronous operation in DPSK mode.
- 8-, 9-, 10-, 11-bit character format in asynchronous mode of operation.
- 0 to 300 bps data rate in FSK operation.
- Break signal supervision.
- Special line monitoring facilities.

Main Operating Modes

- BELL212A/BELL103/V.22 Standard Selection.
- Answer tone selection.
- Fallback Mode selection.
- Originate/Answer Channel Selection.
- Synchronous/Asynchronous Mode Selection.
- Character length selection in asynchronous mode.
- Overspeed Selection.
- Scrambler Selection.
- Guard tone selection in V.22 mode.
- Analog/Digital test loop Selection.

1.2 - Pin Configuration



1.3 - Description of Pins

Pin 1 : V^+

Positive power supply : 5V ±5%

Pin 2 : $\overline{ATE}$ (Answer Tone Enable)

This pin allows to configure the device in either modem mode or as a transmitter of pure frequency (answer tone).

- *A logic low (0) signal applied to this pin causes the device to output through ATO (Analog Transmit Output) pin a pure sinewave whose frequency depends on the programming of C/B ($\overline{CCITT}$/BELL) pin.*
- *Inversely, a logic high (1) on $\overline{ATE}$ pin will configure the device in modem mode.*

Pin 3 : C/B ($\overline{CCITT}$/BELL)

This three-state input selects one of CCITT V.22 and BELL 212A standards.

Pin 4 : A/S ($\overline{Asynchronous}$/Synchronous)

In DPSK mode, this three-state input selects Asynchronous or Synchronous mode of operation. In asynchronous operation, it also provides the character length selection.

Pin 5 : $\overline{TL}$ ($\overline{Test\ Loop}$)

Three-state input pin for the selection of **Test loop 2** or **Test loop 3**.

Pin 6 : OSE (Over Speed Enable)

In asynchronous mode, this input selects one of two possible over speed configurations available in CCITT standard recommendations.

Pin 7 : BRS (Binary Rate Selection)

This pin is used for the selection of binary rate as follows :

- **A logic low** (0) signal on this input configures the device to receive and transmit data at **1200 bps**.
- **A logic high** (1) signal applied to this input enables the circuit to receive and transmit data at **600 bps** in **CCITT mode** or **300 bps** in **BELL 212A mode**.

Pin 8 : $\overline{RxD}$ ($\overline{Receive\ Data}$)

This output provides binary data provided by the demodulator.

Pin 9 : RxCLK (Receive Clock)

This output corresponds to Modem's receive bit clock.

- In synchronous mode, the clock is synchronized with data output through $\overline{RxD}$ pin.
- In asynchronous mode, this pin delivers a clock rate 16 times faster than modem's modulation rate.

Pin 10 : TEST

The output signal is available on this pin before passing through the descrambler. This pin is intended for "**handshake**" and "**remote loop request**" purposes.

Pin 11 : $\overline{DCD}$ ($\overline{Data\ Carrier\ Detect}$)

This pin will go **low** when device receives a signal level **higher than - 43 dBm** on RAI (Receive Analog Input) **pin** and goes **high** if the signal level is **lower than - 48 dBm**. The - 43 dBm to - 48 dBm range provides a **5 dB** hysteresis for the initiation of $\overline{DCD}$ function.

Pin 12 : CLS (Character Length Selection)

In conjunction with $\overline{A}$/S pin, this input selects the character length.

Pin 13 : RDI (Receive Demodulator Input)

This input receives analog signals and directs them to comparators associated with demodulator and signal detector. The signal is also applied to various demodulation circuitry.

Pin 14 : RFO (Receive Filter Output)

The analog signal first goes through various band-pass and equalization filters and is then available at this output pin.
Access to this pin simplifies in particular the device test proceaures. While designing an application, and as far as possible, the P.C.Board layout must be so arranged that RFO output could be reaaily couplea to RDI input terminal through a single capacitor.

Pin 15 : V^-

Negative power supply : -5V $\pm$5%

Pin 16 : ATO (Analog Transmit Output)

In conjunction with signal applied to $\overline{ATE}$ ($\overline{Answer\ Tone\ Enable}$) terminal, this output delivers either a modulated carrier or an answer tone.

Pin 17 : EXI (External Tone Input)

With $\overline{RTS}$ ($\overline{Request\ To\ Send}$) terminal at logic "1", this analog input accepts an external tone which will be first filtered and then routed to ATO (Analog Transmit Output) terminal.

Pin 18 : RAI (Receive Analog Input)

This is input terminal to the receive filter. Signals received via line are applied to this pin.

Pin 19 : $\overline{A}$/O ($\overline{Answer}$/Originate)

Signal level applied to this pin selects modem's operating mode (Answer or Originate) as follows :

A "0" applied to this pin ***selects Answer mode.***

A "1" applied to this pin ***selects Originate mode.***

Note : In answer mode, upper channel (2400 Hz) and guard tone (1800 Hz) may be transmitted simultaneously, provided that the guard tone power level is 6dB less than that of modulated 2400 Hz signal. Transmission of this guard tone is enabled through C/B terminal.

Pin 20 : GND

This is the ground terminal common to all digital and analog sections of TSG 7515.

Pin 21 : SEI ($\overline{Scrambler\ Enable\ Input}$)

This input enables the scrambler operation.

A "0" applied to this input ***enables the scrambler.***

A "1" applied to this input ***disables the scrambler.***

Pin 22 : $\overline{RTS}$ ($\overline{Request\ To\ Send}$)

With a logic level "1" applied to this pin, the aevice outputs through ATO pin the signal delivered by EXI terminal.

With a logic level "0" on this pin, the circuit aelivers through ATO terminal a signal whose characteristics are determined by the state of $\overline{ATE}$ terminal.

With this pin at logic level "-1", the TSG 7515 is configured as a programmable filter. That is, TxSCLK input becomes a clock input running at a frequency equal to twice the sampling frequency of the receive filter, that may be assigned to upper or lower channel, in accordance with signal level applied to $\overline{A}$/O terminal. In this configuration of $\overline{RTS}$, the signal originated through $\overline{DCD}$ terminal is the exact representation of the tone envelope detected via line.

Pin 23 : $\overline{TxD}$ ($\overline{Transmit\ Data}$)

This input receives the data transmitted by terminal.
In DPSK and FSK operating modes, these data bits (1 and 0) determine the phase (for DPSK) or the frequency (for FSK) of the signal output through ATO pin.

Pin 24 : TxCLK (Transmit Clock [Generated by Modem])

In the absence of TxSCLK, this output delivers the bit clock transmitted by the modem for the synchronization of data output through TxD terminal.

BRS selects the frequency as follows :

BRS = 0 ==> TxCLK = 1200 Hz

BRS = 1 ==> TxCLK = 600 Hz

Pin 25 : TxSCLK (Transmit Clock [Generated by Terminal])

This input corresponds to bit clock generated by the terminal whose frequency is 1200 Hz if BRS=0 and 600 Hz if BRS=1. This clock allows to lock the modem's internal clock on the clock generated by terminal, thus providing synchronization between these two clocks.

Pin 26 : CLK (Clock)

This is buffered output of the clock running at 4.9152 MHz.

Pin 27 : Xtal in (Oscillator Input)

This pin corresponds to the oscillator's input inverter. It is normally connected to an external crystal but may also be fed by a pulse generator. The crystal frequency must correspond to standard frequency of 4.9152 MHz.

Pin 28 : Xtal out (Oscillator Output)

This pin corresponds to the output of an inverter with sufficient loop gain to trigger and maintain the crystal oscillation.

1.4 - General Description & Block Diagram

TSG 7515 is an integrated circuit fabricated resorting to silicon gate CMOS technology.
Device includes major modem functions required for simultaneous bidirectional transmission of asynchronous or synchronous data in accordance with the following standard requirements :

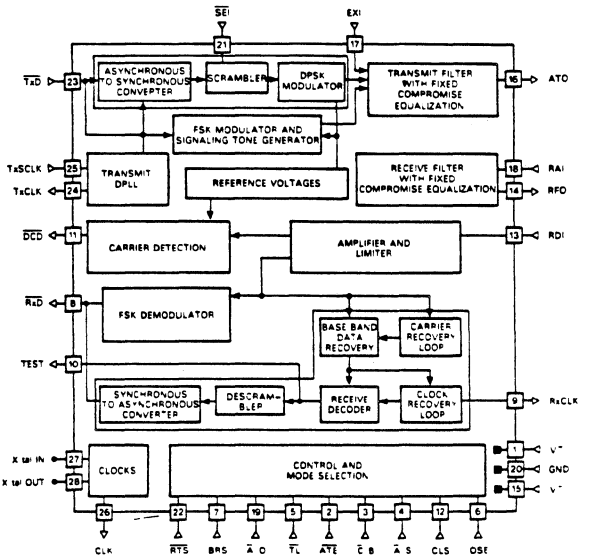
- *CCITT V.22 variants A & B*
- *BELL 212A DPSK operation*
- *BELL 103 FSK*

This modem operates using channel multiplexing techniques by frequency allocation of 600 Bauds for modulations rate and 1200 bits/s (600 bits/s in fallback mode) for transmission rate.

Transmission mode for each channel is Differential Phase Shift Keying (DPSK) modulation combined with on-line synchronous transmission. This feature is entirely reversible, i.e. operation is possible in either of Originate or Answer modes.

When used in combination with appropriate line and controller circuits, this device can operate on both 2-wire switched telephone network and all point-to-point leased lines.

Figure 1 - TSG 7515 Block Diagram



1.5 - Functional Description

The device is organized in 3 distinct sections :

- **Transmit section**
- **Receive section**
- **Common units**

1.5.1 - Transmit Section

This section comprises :

- An **asynchronous to synchronous converter** whose duty is to accept chain of asynchronous characters and to convert it to a form suitable for 1200 bits/s or 600 bits/s +0.01% synchronous transmission.

  This converter meets in all respects CCITT standard requirements defined in Chapter "4.2.1" of V.22 recommendations.

  In synchronous mode of operation, the converter is disabled.

- A **variable ratio divider** used for the generation of eight different frequencies :

1200Hz ±0.5 Hz	DPSK lower channel (Originate Mode)
1800 Hz ±20 Hz	Guard tone transmitted optionally with upper channel
2100 Hz ± 16 Hz	Answer tone (CCITT Standards)
2400 Hz ± 1 Hz	DPSK upper channel (Answer Mode)
2225 Hz ± 16 Hz	Answer tone (BELL Standards) or FSK upper channel
2025 Hz ± 10 Hz	FSK upper channel
1270 Hz ± 5 Hz	FSK lower channel
1070 Hz ± 5 Hz	FSK lower channel

- A **transmit clock generator** using a phase-locked loop circuit in order to lock the transmission clock onto either the clock generated by data terminal or the receive clock.

- A **data scrambler** in accordance with CCITT standard requirements as defined in "Chapter 5.1" of V.22 recommendations.

- A **buffer circuit** that stores the last phase of the carrier and generates appropriate phase shift thus providing the new phase shift to be applied to the carrier.

- A **carrier generator** that uses two sub-carriers over modulated in amplitude, to synthesize the DPSK signal.

- A **transmit filter** whose frequency response is determined by selected mode of operation (Originate or Answer).

- A **non switched smoothing filter** that removes clock transients and rejects out-of-band frequencies.

1.5.2 - Receive Section

This section includes :

- An **anti-aliasing filter**

- A **band-pass receive filter** whose frequency response depends on the selected mode of operation.

- A **compromise equalizer filter** that provides appropriate functional performance on a variety of lines.

- A **phase-locked loop** for the recovery of carrier signal frequency so as to perform a coherent differential phase demodulation on received signal.

- A **demodulator.**

- Two **low-pass digital filters** for the extraction of **Eyes Pattern**

- A **decision making module** that converts the **eyes pattern** into logic signals, stores them, detects the phase shift and performs identification of the received data.

- A **synchronization unit** that recovers the modulation time base and delivers RxCLK (Receive signal Clock) to the data terminal.

- A **delayed hysteresis level detector** that meets CCITT standard requirements of connector pin 109 as defined in Chapter 3.3 of V.22 recommendations.

- A **data descrambler** in accordance with CCITT V.22 recommendations.

- A **synchronous to asynchronous converter** whose duty is as follows :

  - Accept chain of characters originated from a V.22-type asynchronous modem operating in transmit mode, demodulated by a V.22-type synchronous demodulator

  - Recover the initial character chain applied to the asynchronous to synchronous converter of the transmitting modem.

This synchronous to asynchronous converter meets in all respects the CCITT standard requirements as defined in Chapter 4.2.2 of V.22 recommendations.

The converter is disabled in synchronous mode of operation.

1.5.3 - Common Units

This section includes :

- A **time base generator** that uses a standard 4.9152 MHz crystal oscillator to derive all internal clock frequencies required for modulator and demodulator operation.

- A **reference voltage generator** delivering an internal reference voltage for :

  - Amplitude clamping of the transmitted signal.

  - Definition of demodulator's two threshold detection levels.

1.6 - Functional Characteristics

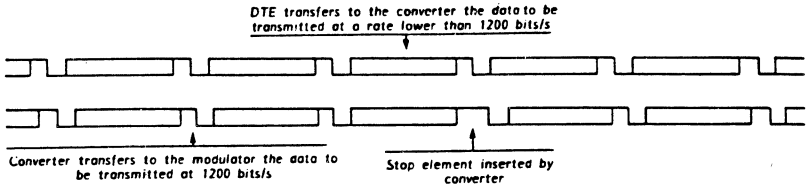
Asynchronous/Synchronous & Synchronous/Asynchronous Converters

Operating principles of these converters are covered in Sections 4.2.1 and 4.2.2 of CCITT V.22 recommendations.

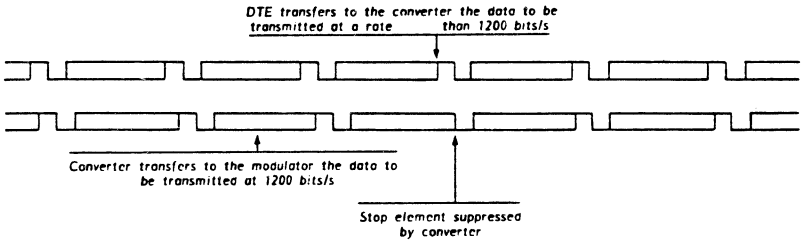
These converters are employed only in the case of variant B configuration.

1.6.1 - Asynchronous/Synchronous Converter

a) - If data to be transmitted is generated at a rate lower than 1200 bits/s (but within the over speed selection limits imposed by OSE), the converter will insert the necessary stop elements as illustrated by timing diagram below.

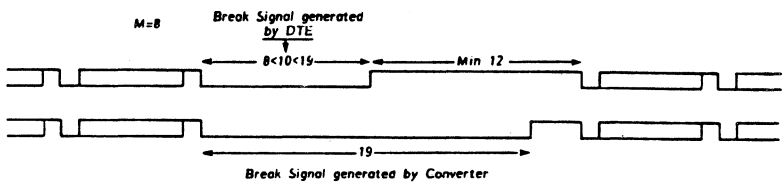


b) - If data to be transmitted is generated at a rate higher than 1200 bits/s (but within over speed selection limits imposed by OSE), the converter will suppress the stop elements as shown in timing diagram below.



c) - Break Signal

Break signal contains M to 2M+3 bits, all of which maintain their initial state. M represents number of bits per character corresponding to selected format. Upon detection of such signal, the converter automatically generates 2M+3 bits all having their initial polarity. Timing diagram below illustrates this procedure.



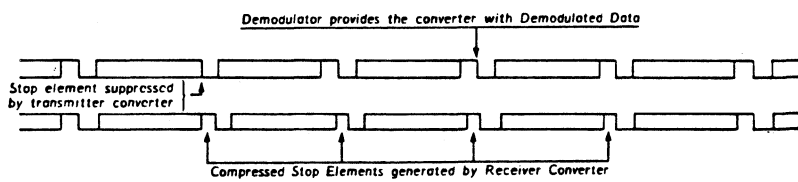
1.6.2 - Synchronous to Asynchronous Converter

In receive mode, this converter must be capable of recovering the data transmitted by distant DTE while respecting the break signal generated by aysnchronous to synchronous converter of the distant modem.

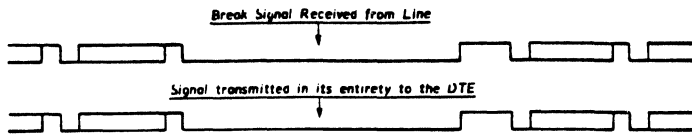
a) - If the converter detects a missing stop element within the demodulated signal :

- It will regenerate this missing element, and
- In order to resynchronize the demodulated signal, it will reduce the duration of stop elements by as much as necessary but within over speed selection limits of OSE.

This procedure is illustrated in timing diagram given below.



b) - The converter detects the missing stop elements at the end of a break signal character, and transfers this signal in its entirety to the DTE as shown in timing diagram below.



1.6.3 - Scrambler & Descrambler

Operating principles of the scrambler and the descrambler are discussed in Chapters 5.1 and 5.2 of CCITT V.22 recommendations.

The scrambler allows to recover, at receiver, the clock rate associated with the received data so as to perform a coherent demodulation and also to provide the DTE with a clock whose phase is synchronized with the received data.

Figure 2 illustrates the "scrambling fundamentals".

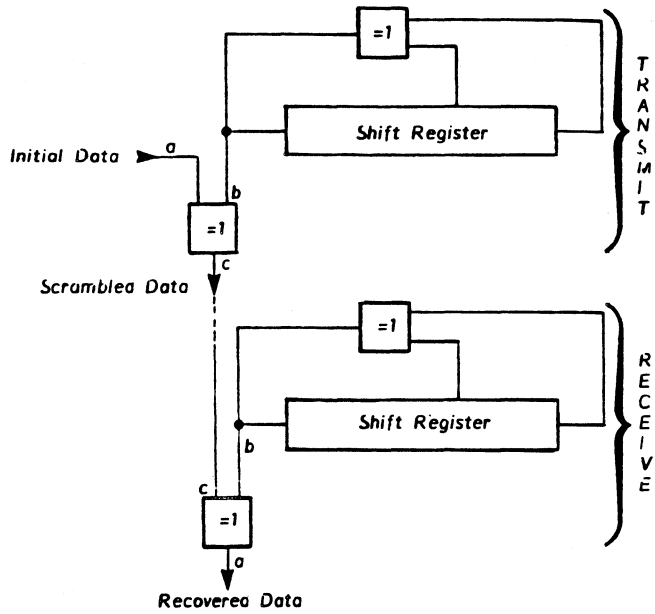
As shown, the scrambler includes a pseudo-random sequence generator composed of :

- *A single-input, single-output shift-register.*
- *In general, a single interconnection point.*
- *An Exclusive OR gate.*

If the interconnection point is appropriately located and if N represents the number of shift-register stages, then the generated bit sequence representing a pseudo-random character will have a period of $2^N - 1$.
Note that the number of identical bits of this sequence will not exceed N.

The shift-register is driven by the transmit clock. The pseudo-random sequence so generated is applied to one of the inputs of the "Exclusive OR"-whose other input is loaded with the data to be scrambled. Thus, data bits are inverted whenever they coincide with a high level (1) of the sequence.

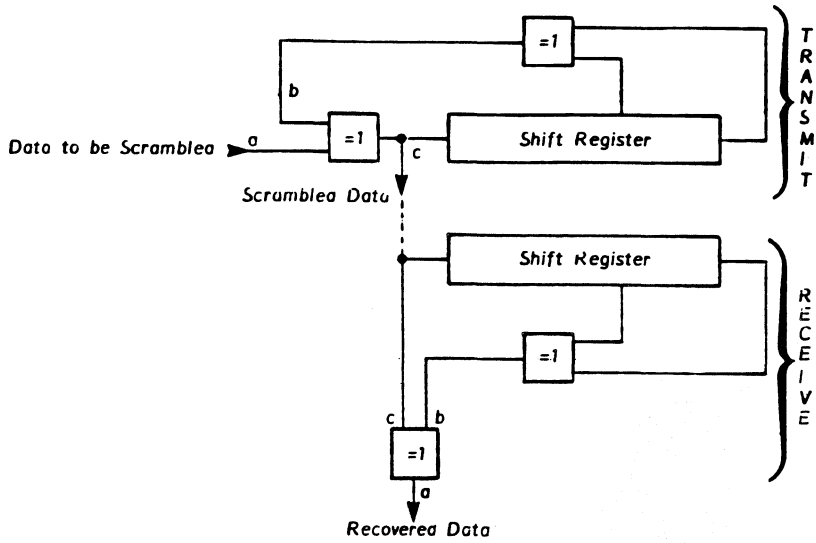
Figure 2 - Scrambler Block Diagram



Inverse procedure is performed in receive mode and requires the pseudo-random generator to operate in synchronization with the pseudo-random sequence generator used at transmission end. In order to avoid this constraint, it is generally preferable to emply a self-synchronizing scrambler similar to the one depicted in Figure 3.

Operation is identical to that given in Figure 2. However, in this case the scrambled data is applied to the transmit register and similarly, after transmission, the scrambled data is applied to the input of the receive register. It is clear that at the end of first N-bit transmission, the receive register will be in the same state as the transmit register - taking into consideration the propagation delay time inherent to the transmission line.

Figure 3 - Self-synchronizing Scrambler



In both types of the scrambler, data recovery procedure is accomplished thanks to reversible property of the **Exclusive Or** *gate.*

If $a \oplus b = c$ *[where* $\oplus$ *represents modulo-2 sum]*

then $a = b \oplus c$

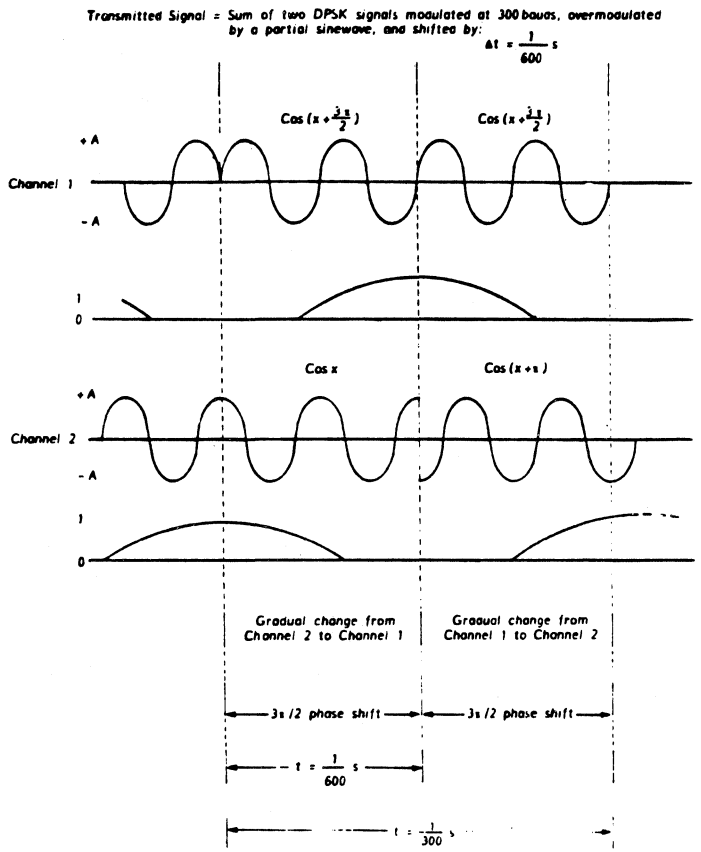
The self-synchronizing scrambler has the disadvantage of **multiplying the number of errors by a factor of 3.** *In fact, when an isolated error appears at the input of the receive register, it causes a* **first error** *in the recovered bit sequence - then a* **second error** *occurs as it reaches the level of interconnection point - and finally a* **third error** *is generated at the last stage of the register.*

1.6.4 - *Carrier & Tone Generators*

The DPSK signal generation is achieved using a ROM containing 32 x 8-bit states and an 8-bit C-2C converter circuit.

1.6.5 - *Transmitted Spectrum*

In order to respect the limits of amplitude and distortion due to propagation delay time recommended by CCITT, the modulated signal comprises sum of two carriers alternately modulated at a master rate of 600 bauds and overmodulated by a partial sinewave, as shown in timing diagram below.



1.6.6 - Filters

1.6.6.1 - Transmit Filter

In combination with the modulation effects, the transmit filter allows to meet performance characteristics recommended by CCITT. A compromise equalizer compensates partially for line irregularities.

This is a 12th order switched-capacitor filter.

1.6.6.2 - Receive Filter

The receive filter allows to recover a maximum amount of energy in receive channel while it offers an efficient rejection of the transmission channel and the guard tones. A fixed compromise equalizer compensates partially for irregularities due to line characteristics.

a) - Lower Channel

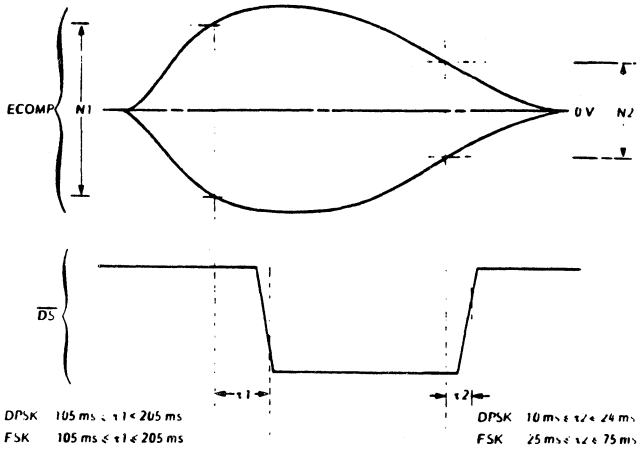
This is a 20th order filter implemented by cascading a 14th order amplitude clamping module and a 6th order all-pass module providing propagation delay time correction.

b) - Upper Channel

This is a 14th order filter implemented by cascading a 10th order amplitude clamping unit and a 4th order all-pass unit providing propagation delay time correction.

1.6.7 - Level Detector

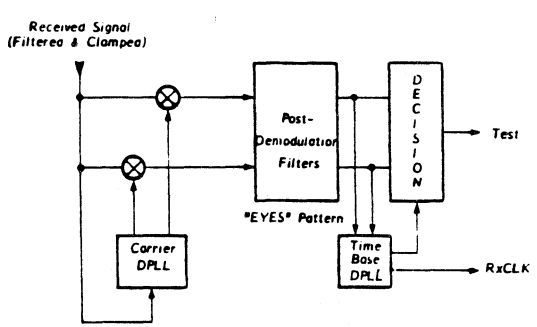
RDI input is connected to a signal detection circuit that discriminates beween two positive levels N1 and N2. Output of the detector is delayed so as to provide hysteresis effects between N1 and N2.
See timing diagram given next.



1.6.8 - Synchronous Demodulator

The signal received on line is first filtered and clamped at appropriate level and then applied to this synchronous modulator which will deliver demodulated data synchronized on receive clock.

1.6.8.1 - Demodulator Block Diagram



1.6.9 - Summary Tables of Operating Modes

1.6.9.1 - Synthesis of different Modes for Receive Section

$\overline{C}$/B	BRS	$\overline{TL}$	$\overline{A}$/O	Receive	Mode
- 1 or 0	X	- 1	0	DPSK Originate Loop 3	V.22
			1	DPSK Answer Loop 3	
		0	0	DPSK Answer Loop 2	
			1	DPSK Originate Loop 2	
		1	0	DPSK Answer	
			1	DPSK Originate	
1	0	- 1	0	DPSK Originate Loop 3	BELL 212A Including BELL 103
			1	DPSK Answer Loop 3	
		0	0	DPSK Answer Loop 2	
			1	DPSK Originate Loop 2	
		1	0	DPSK Answer	
			1	DPSK Originate	
	1	- 1	0	FSK Originate Loop 3	
			1	FSK Answer Loop 3	
		0	0	FSK Answer Loop 2	
			1	FSK Originate Loop 2	
		1	0	FSK Answer	
			1	FSK Originate	

Answer : Receive in Lower Channel
Originate : Receive in Upper Channel
Loop 3 : Analog Loop
Loop 2 : Digital Loop

1.6.9.2 - Synthesis of different Modes for Transmit Section

$\overline{ATE}$	$\overline{C/B}$	BRS	$\overline{A/O}$	Transmit	Mode
0	-1 or 0			2100 Hz	Answer Tone
	1			2225 Hz	
1	-1	0	0	DPSK 1200 bps Answer	V.22 without Guard Tone
			1	DPSK 1200 bps Originate	
		1	0	DPSK 600 bps Answer	
			1	DPSK 600 bps Originate	
	0	0	0	DPSK 1200 bps Answer	V.22 with 1800 Hz Guard Tone
			1	DPSK 1200 bps Originate	
		1	0	DPSK 600 bps Answer	
			1	DPSK 600 bps Originate	
	1	0	0	DPSK 1200 bps Answer	BELL 212 A
			1	DPSK 1200 bps Originate	
		1	0	FSK 0 - 300 bps Answer	
			1	FSK 0 - 300 bps Originate	

Answer : Transmit in Upper Channel

Originate : Transmit in Lower Channel

1.6.9.3 - Mode Selection in Phase Modulation Transmission

$\overline{A}$ / S.	CLS	OSE	Transmission Mode	Character Length	Overspeed
- 1	0	0	Asynchronous	8	+ 1% , - 2.5%
		1			+ 2.3% , - 2.5%
	1	0		11	+ 1% , - 2.5%
		1			+ 2.3% , - 2.5%
0	0	0		9	+ 1% , - 2.5%
		1			+ 2.3% , - 2.5%
	1	0		10	+ 1% , - 2.5%
		1			+ 2.3% , - 2.5%
1	0	0	Synchronous		

1.6.9.4 - Test Pin

ATE	$\overline{C}$ / B	BRS	Transmit	Receive	Test
0	- 1 or 0	0	2100 Hz	V.22 DPSK 600 bps	DDO
		1		V.22 DPSK 1200 bps	DDO
	1	0	2225 Hz	BELL 212A DPSK 1200 bps	DDO
		1		BELL 103 FSK 0 - 300 bps	HLO
1	- 1	0	V.22 without Guard Tone DPSK 1200 bps		DDO
		1	V.22 without Guard Tone DPSK 600 bps		DDO
	0	0	V.22 with Guard Tone DPSK 1200 bps		DDO
		1	V.22 with Guard Tone DPSK 600 bps		DDO
	1	0	BELL 212A DPSK 1200 bps		DDO
		1	BELL 103 FSK 0 - 300 bps		HLO

DDO : DPSK Demodulator Output

HLO : Hard Limiter Output

1.7 *Call Progress Detection*

The TSG7515 is a single chip 1200 bps (DPSK) and 300 bps (FSK) voiceband modem, compatible with Bell 212A, Bell 103, and CCITT V.22 A-B standards. The device includes transmit and receive filters implemented using switched capacitor techniques. A special mode has therefore been included in the TSG7515 to allow for the variation of the recieve filter characteristics. This mode also features a fast carrier detect to facilitate call progress detection. By changing the passband and bandwidth of the receive filter it is then possible to monitor the line for call progress tones such as busy and dial tone.

To select the line monitoring mode, a logic "-1" must be applied to the RTS input (pin 22). In this mode the receive filter clock is directly derived from the TxSCLK input (pin 25). Since in this mode the center frequency of the receive filters is proportional to the TxSCLK frequency, it is possible to tune the passband according to the frequencies to be detected. Table 1 shows some suggested clock frequencies that may be used to adjust the receive filter passband for detection of certain call progress signals. Furthermore, the DCD output performs a fast carrier detection of 3 - 5 mS that is equivalent to an envelope detection of the call progress signal.

TABLE 1

TxSCLK	Originate		Answer		Application
	Center frequency	Passband at 3 dB	Center frequency	Passband at 3 dB	
210 kHz	2400 Hz	±400 Hz	1200 Hz	±400 Hz	Voice detection
45 kHz	510 Hz	±85 Hz			440 Hz detection
			260 Hz	±85 Hz	330 Hz detection
76.8 kHz			440 Hz	±150 Hz	Dial tone and Busy tone detection

It should also be noted that when in the line monitoring mode the ATO output (pin 16) will only output to the line the filtered signal from the EXI input (pin 17). In a typical application, DTMF signals would be input to EXI for tone dialing purposes, and the TSG7515 would be switched out of line monitoring mode once the connection had been established. With these and other features the TSG 7515 provides the majority of all the functions necessary to implement an auto-dial/auto-answer modem.

CHAPTER 2 - DETAILED DESCRIPTION OF V.22 & BELL 212A STANDARDS

2.1 - Foreword

Due to the fact that the present application note is primarily intended for technicians not possessing an in-depth knowledge of this "advanced" field of telecommunications, it seemed appropriate to include an overview of the most recent publications covering specifications of the V.22 and BELL 212A standard requirements.

We shall also discuss line interface characteristics and requirements which together with modulator, demodulator, carrier detection, user interface (V.24, RS-232C) must be appropriately employed - or else, equipment of different manufacture will be unable to communicate with each other.

On the other hand, if standard requirements and rules are properly observed, then a system implemented in Japan and another in France, will be able to communicate without any difficulty.

2.2 - V.22 Standard

Modem operating at 1200 bits/s in full duplex.

Normalized for operation on general switched telephone lines and leased networks.

2.2.1 - General Description

This Modem is intended for operation on switched telephone networks and point-to-point leased lines.

Main characteristics are as follows :

- Duplex operation on switched 2-wire telephone and point-to-point leased lines.
- Frequency division channel assignment.
- Differential Phase Modulation for each channel with on-line synchronous transmission at 600 bauds.
- Scrambler availability.
- Measurement facilities.

Since the application coverage is wide, V.22 recommendations provide for 3 possible configuration variants. As far as we are concerned, we shall limit our discussion to two of these variants.

Characteristics of these variants are as follows :

2.2.1.1 - *Variant A*

1200 bits/s	*synchronous*
600 bits/s	*synchronous*

2.2.1.2 - *Variant B*

1200 bits/s	*synchronous*	} *Variant A*
600 bits/s	*synchronous*	
	+	
1200 bits/s	*Asynchronous*	
600 bits/s	*Asynchronous*	

2.2.2 - *On-line Signals*

Carrier frequency and Guard Tone

Frequencies of the operation are respectively **1200 Hz ± 0.5 Hz for lower channel** *and* **2400 Hz ± 1 Hz for upper channel.** *A* **1800 Hz ± 20 Hz Guard Tone** *is transmitted continuously whenever modem transmits in upper channel. This guard tone must be disabled when modem transmits in lower channel.*

An additional 550 Hz guard tone may be transmitted for national applications.

2.2.2.1 - *Levels of transmitted Data Signals & Guard Tone*

The 1800 Hz guard tone must be 6 ± 1 dB below power level of data signals transmitted in upper channel.

Total power of signal transmitted on-line must meet specifications defined by V.2 recommendations :

Total power drawn from line by subscriber equipment must not exceed 1 mW, whatever the operating frequency.

Note that this power must be identical in both directions (go & return).

Due to the presence of the guard tone, power level of upper channel signals is approximately 1 dB below that of the lower channel signals.

2.2.3 - *Fixed delay Compromise Equalizer*

This on-chip compromise equalizer is commonly shared by both transmit and receive sections.

Note : This equalizer is mainly intended to compensate for transmission line irregularities caused by signal amplitude attenuation and group propagation delay time $\frac{d\varphi}{d\omega}$.

2.2.4 - *Spectrum & Group Propagation Times*

Signal transmitted on the line must conform to characteristics depicted in the following Figure.

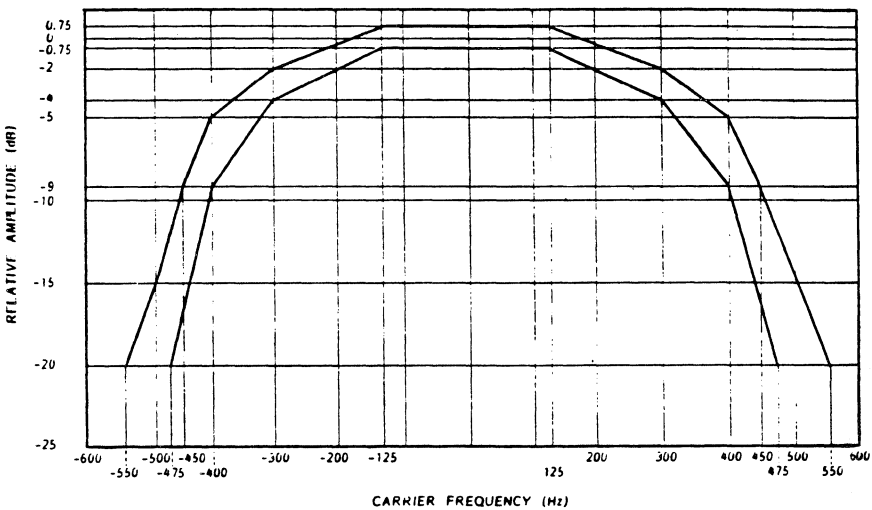


Figure 7 - Amplitude limits of signal transmitted on-line (without equalization)

The group propagation time of transmitter output signals must fall within ± 100 µs limits in frequency range of 800 Hz to 1600 Hz (lower channel) and 2000 Hz to 2800 Hz (upper channel).

2.2.5 - *Modulation*

2.2.5.1 - *Bit Rate*

As mentioned earlier, we shall only discuss variants A and B of V.22 .

The on-line transmission bit rate must be either **1200 bits/s or 600 bits/s ± 0.01%** with a modulation rate of **600 bauds ± 0.01%** .

2.2.5.2 - *Data bits coding*

Data stream to be transmitted is split into groups of consecutive 2 bits called **dibits**. Each dibit is encoded by considering the relative phase change with respect to previous phase element of the signal (see table below).

Dibit Value (at 1200 bits/s)	Bit Value (at 600 bits/s)	Phase Change
00	0	+ 90°
01		0°
11	1	+ 270°
10		+ 180°

Note : The phase change is the actual phase shift on-line within signal transition area situated between the middle of a signal element and the mid point of the following element.

Upon receipt, dibits are decoded and recovered bits arranged in correct order. The left number of the dibit appears first within the data streams as they enter modem's demodulater section located following the scrambler.

The foregoing applies to bit rate of 1200 bits/s. In the case of 600 bits/s, each bit is coded by a phase change with respect to the preceding phase of the signal element.

2.2.6 - *Frequency tolerance of the received signal*

The transmitter carrier frequency tolerance is at maximum ± 1 Hz and allowing a drift of ± 6 Hz due to transmission line characteristics, the receiver must therefore be capable of accepting errors at ± 7 Hz tolerance on received frequencies.

2.2.7 - Connector Pins

The following table gives a list of indispensable and optional connector pins used for DTE / DCE Interface.

2.2.7.1 - Summary of Connector Pins

Pin Number	Function	Note
102	Signal Ground or Common return Line	
102 a	DTE common return line	
102 b	DCE common return line	
103	Transmitted Data	
104	Received Data	
105	Request To Send	
106	Clear To Send	
107	Data Set Ready	
108 / 1	Connect Data Set to Line	
108 / 2	Data Terminal Ready	
109	Received line signal (carrier detector)	
111	Bit Rate Selection (DTE originated)	1
113	Transmit signal element timing (DTE source)	2
114	Transmit signal element timing (DCE source)	3
115	Receive signal element timing (DCE source)	3
125	Ring / Calling Indicator	4
140	Test / Diagnostic Loop	
141	Local Loop	
142	Test Indicator	

Note 1 : This pin is optional.

2 : Signals on this pin are ignored when modem not operating in synchronous mode.

3 : This pin is locked on OFF state when modem does not operate in synchronous mode.

4 : Used only when modem is connected to public switched telephone lines.

2.2.7.2 - *Thresholds of Pin 109*

Thresholds of pin 109 are specified at Modem input terminals, ignoring effects produced by compromise equalizer.

This pin must not react to 1800 Hz Guard Tone and 2100 Hz Answer Tone transmitted during call establishment sequence.

Upper Channel threshold

Higher than -43 dBm ==> Pin 109 ON
Lower than -48 dBm ==> Pin 109 OFF

Lower Channel threshold

Higher than -43 dBm ==> Pin 109 ON
Lower than -48 dBm ==> Pin 109 OFF

The intermediate state of pin 109 between ON and OFF levels is not specifed. However, the signal level detector must exibit a hysteresis higher than 2 dB.

2.2.7.3 - *Pin 111 & Bit Rate Control*

The bit rate is selected by :

- *Appropriate strap or switch settings on Modem Board*
- *Using connector pin 111*
- *Or, combination of both.*

If used, pin 111 will in ON state enable 1200 bits/s operation, and 600 bits/s in OFF condition.

2.2.7.4 - *Electrical Characteristics of Connector Pins*

It is advised to respect electrical characteristics specified in V.28 recommendations. Applicable connector and pin spacing requirements are defined in ISO 2110 publication.

2.2.7.5 - *Error Conditions of Connector Pins*

Some applications require detection of failure conditions on connector pins, a summary of which is given next.

1) - Lack of connection between DTE and DCE

2) - Open-circuited interconnecting cable

3) - Short-circuited interconnecting cable

Type 1 error : Data pins are all at logic level "1". Control and timing pins are in OFF state.

The DTE must consider an error on pin 107 as being in OFF state.

Similarly, failure conditions on pins 105 and 108, are considered as OFF states by DCE.

2.2.8 - DTE / DCE Interface Modes of Operation

2.2.8.1 - Variant A

The Modem may be configured for the following modes of operation :

- 1200 bits/s ± 0.01% synchronous
- 600 bits/s ± 0.01% synchronous

In these modes, the modem monitors pin 113 or pin 114 and accepts through pin 103 the synchronous data originated from DTE. These data are then scrambled and forwarded to the modulator for coding.

In addition to normal transmit timing element, the modem must provide the possibility of deriving the transmit signal element timing from receive signal element timing.

2.2.8.2 - Variant B

- 1200 bits/s ± 0.01% synchronous
- 1200 bits/s asynchronous, 8-, 9-, 10-, 11-bit characters
- 600 bits/s ± 0.01% synchronous
- 600 bits/s asynchronous, 8-, 9-, 10-, 11-bit characters

Synchronous modes are identical to those outlined for variant A.

2.2.9 - Transmitter

In asynchronous modes, modem accepts asynchronous data stream issued by DTE at a nominal rate of 1200 or 600 bps.

Asynchronous data are converted into suitable format for synchronous transmission at 1200 or 600 bps ± 0.01%, then scrambled and sent to the modulator for encoding.

The converter must be configured to accept the following character formats :

a) - One start bit, followed by seven data bits and one stop bit (9-bit character)

b) - One start bit, followed by eight data bits and one stop bit (10-bit character)

c) - One start bit, followed by nine data bits and one stop bit (11-bit character)

d) - One start bit, followed by six data bits and one stop bit (8-bit character)

2.2.10 Fundamental Bit Rate

The intercharacter binary bit rate (including start and information bits) generated by DTE or provided through pin 103, must be 1200 or 600 bits/s with tolerance falling within + 1% to - 2.5% limits.

When the character bit rate falls within the limits of theoretical values (1200 or 600 bits/s) and the maximum value (+ 1%), the asynchronous to synchronous converter implemented in the transmitter section must suppress, whenever necessary, the stop bits of the input characters.
Within 8 consecutive characters, at most one stop element may be eliminated.

On the other hand, if the character bit rate falls within the limits of theoretical values (1200 or 600 bits/s) and the minimum value (- 2.5%), then the asynchronous to synchronous converter will provide more bits per second than DTE is generating. As a consequence, the converter will insert additional stop elements within the transmitted characters.

2.2.10.1 - Higher bit rates

Some Data Terminal Equipment and Multiplexors exceed the + 1% bit rate tolerance. The modem must therefore be capable of accepting data provided by DTE at 1200 or 600 bits/s, tolerance between + 2.3% and - 2.5%, and consequently suppress at most one stop element per 4 consecutive characters.

2.2.11 - *Break Signal*

If the converter detects M to 2M + 3 bits all of which have the polarity of start bit, where M is the number of bits per character in selected format, it will transmit 2M + 3 bits all with start polarity. However, if more than 2M + 3 bits of start polarity are detected, the converter will transmit them all with start polarity.

2.2.12 - *Receiver*

Intercharacter bit rate delivered to DTE through pin 104 must have a value between 1200 and 1221 bits/s.

For all characters, start and data elements should be of identical nominal length. The wiath of the stop element should not be reduced by more than 12.5% for fundamental bit rates so as to allow detection of any excessive bit rate caused by transmission terminal equipment.

2.2.12.1 - *Break Signal*

Received 2M + 3 bits (or more) with start polarity sent by originating modem are supplied to pin 104. The modem detects the transition from stop polarity to start polarity in order to regenerate character synchronization.

2.2.13 - *Scrambler & Descrambler*

2.2.13.1 - *Scrambler*

The modem includes a self-synchronizing scrambler that implements $1 + x^{-14} + x^{-17}$ *polynomial generator. This scrambler is integrated inside the transmitter section of the modem.*

The data message sequence applied to the scrambler are divided by the polynomial generator. The resultant quotient coefficients, arranged in decreasing order, represent the data sequence to appear at scrambler output.

The scrambler output data sequence is given by the following expression.

$$D_s = D_i \odot D_s \cdot x^{-14} \odot D_s \cdot x^{-17}$$

Where :

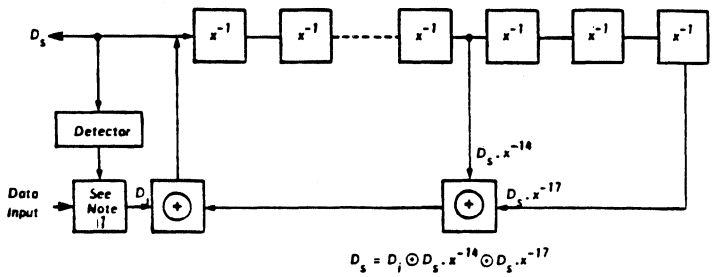
D_s : *Data sequence at Scrambler Output*

D_i : *Data sequence applied to Scrambler Input*

$\odot$: *Modulo-2 Sum*

"." : *Binary multiplication*

The following Figure illustrates Scrambler functional configuration.



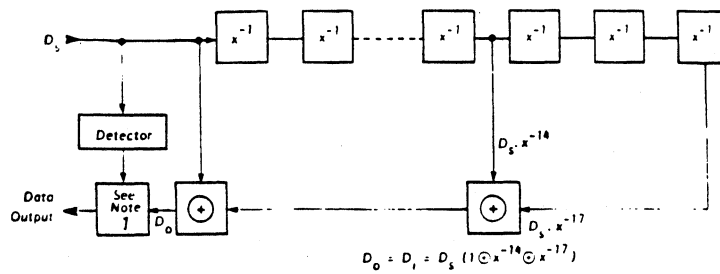
Note 1 : In order to avoid scrambler blocking to cause occasional and unpredicted occurrence of type-2 loopback, 64 consecutive binary "1"s must be first detected on scrambler output (D_S) and only then, the next signal applied to scrambler input (D_i) will be inverted. This function must be disabled during both call establishment and type-2 loopback sequences.

2.2.13.2 - Descrambler

Modem's receiver integrates a self-synchronizing descrambler implementing the $1+x^{-14}+x^{-17}$ polynomial. The data sequence obtained after demodulation must be multiplied by $1+x^{-14}+x^{-17}$ polynomial generator so as to obtain the descrambled message. Coefficients of the regenerated message, arranged in decreasing order, represent the data sequence on D_0 output. This sequence is defined by the following expression :

$$D_0 = D_S(1 \oplus x^{-14} \oplus x^{-17})$$

Figure below gives Descrambler functional diagram.



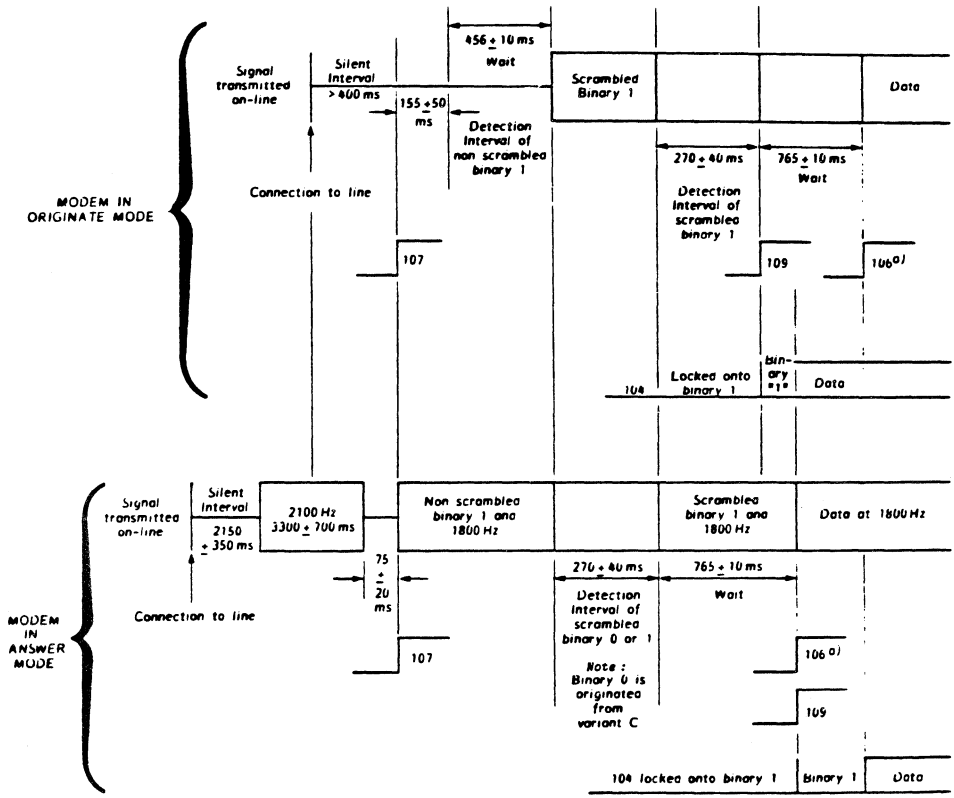
2.2.14 - Sequence of Operation (Permanent Carrier)

2.2.14.1 - Channel & Operating Mode Selection

In public switched telephone lines, the called modem receives data in lower channel and transmits in upper channel.

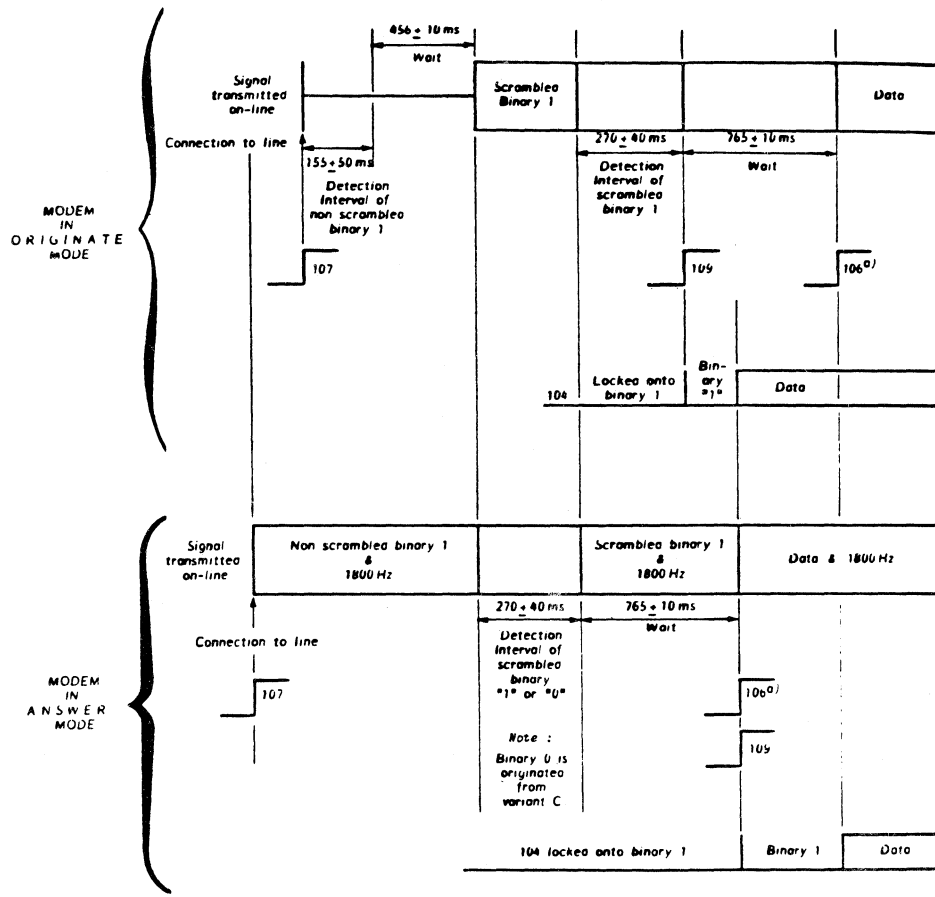
2.2.14.2 - Operation on switched telephone lines

Timing diagram below illustrates how initial synchronization is established between originating and answering modem communicating through international switched telephone networks.



a) Assumes that connector pin 105 has been switched to ON state.

The following timing diagram depicts the call establishment sequence without auto-answer capability, as defined in V.25 recommendations.



a) Assumes that connector pin 105 has been switched to ON state.

2.2.14.3 - Modem in Originate Mode

Once the originating Modem is connected to line, it must be conditioned to receive signals in upper channel by switching the connector pin 107 to **ON** state as required by V.25 recommendations. Then, the modem remains silent until it detects a sequence of non scrambled "1"s during an interval of 155 ± 50 ms, waits another 456 ± 10 ms and then begins sending a sequence of scrambled "1"s in the lower channel. When it detects a sequence of scrambled binary "1"s for a period of 270 ± 40 ms in the upper channel, the modem switches connector **pin 109** (**Received Line Signal**) to **ON** state and then goes silent for 765 ± 10 ms. Then **pin 106** (**Clear To Send**) will react in response to the state of **pin 105** (**Request To Send**).
When **pin 106** (**Clear To Send**) goes to **OFF** state, **pin 103** (**Transmitted Data**) will be locked on binary "1".

2.2.14.4 - Modem in Answer Mode

Once the answering modem is connected to line, and immediately after answer sequence defined by V.25 recommendations is terminated, the modem will be conditioned to receive signals in the lower channel. Connector **pin 107** (**Data Set Ready**) is switched to **ON** state and the modem begins transmitting a sequence of non scrambled binary "1"s. When it detects scrambled binary "1"s for an interval of 270 ± 40 ms in lower channel, the modem begins sending scrambled binary "1"s in the upper channel, waits 765 ± 10 ms and then switches **pin 109** (Data Carrier Detect) to **ON** state and as a consequence **pin 106** will react in response to **pin 105**. In the case where **pin 106** is **OFF** connector **pin 103** (**Transmitted Data**) will be locked on binary state "1"
The foregoing sequence must be applied whenever two modems are connected to the line manually and irrespective of which modem is connected first.
Once the contact has been established, any unpredicted loss and the reappearance of the signal on line, must not cause the generation of another call establishment sequence.

2.2.15 - Measurement Facilities (Maintenance)

The system must provide for both type-2 (local & remote) test loops and also type-3 loops, in accordance with V.54 recommendations.

2.2.15.1 - Type-2 Loopback Establishment

Important : Signals used to establish type-2 loopback may be transmitted only after the conclusion of synchronization handshake procedure.

As defined in V.54 recommendations, from now on, the modems will be called **Modem A & Modem B.**

When **Modem A** receives **"through a switch mounted on front panel"** an instruction to establish type-2 loopback, it begins the transmission of the initiation signal composed of non scrambled binary "1" elements.

Modem B detects this signal for an interval of 154 to 231 ms and returns to **Modem A** a sequence of scrambled alternate "1"s and "0"s at 1200 bits/s (or 600 bits/s).

Modem A detects alternate scrambled "1"s and "0"s during an interval of 231 to 308 ms, ends the initiation signal and transmits scrambled "1"s at 1200 bits/s (or 600 bits/s).

Modem B detects the loss of the initiation signal and consequently establishes a type-2 loopback locally.

After the reception of scrambled binary "1"s during 231 to 308 ms, **Modem A** informs the DTE that transmission of test messages may begin.

2.2.15.2 - Suppression of Type-2 Loopback

When **Modem A** receives instruction to remove the type-2 loopback, the on-line signal transmission must be halted for 77 ± 10 ms interval, then re-initiated.

Modem B detects, signal loss within 17 ± 7 ms, signal reappearance within $155 + 50$ ms, and then resumes its normal mode of operation.

2.3 - BELL 212A Standard Description

Previous discussion covered in detail V.22 standard requirements that approach closely those of BELL 212A standards. In order to avoid unnecessary repetition of common topics, we shall limit our discussion to differences between V.22 and BELL 212A standard requirements.

BELL 212A covers entirely the A and B variants of V.22 with minor differences indicated below :

- Variant B has no fallback mode at 600 bits/s.
- Character lengths in asynchronous mode are limited to 9 and 10 bits.
- Only one overspeed (+ 1% , - 2.5%) is available.

BELL 212A standard includes a fallback mode called **BELL 103.**

BELL 103 Characteristics

Modulation Speed : **300 bits/s**

Modulation Type : **Frequency Shift Keying (FSK)**

Data Transfer : **Asynchronous, through both the RS-232C interface connector and the telephone line.**

Frequency Spectrum : **Band Division**

Communication : **Full duplex**

It differs from its CCITT equivalent in that **logic "1"** is represented by the **high frequency** and **logic "0"** by the **low frequency** of the **frequency pair** used for the modulation.

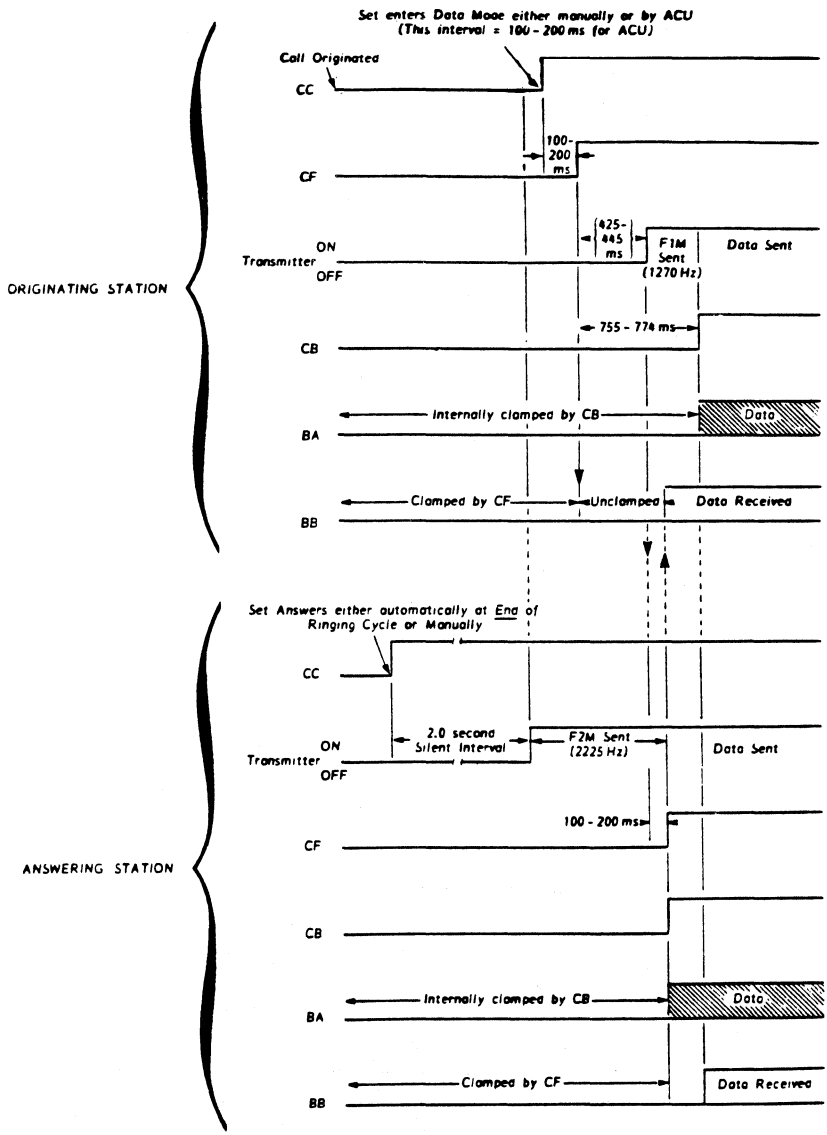
Differences between BELL 212A & V.22

- In answer mode, detection of originating modem's speed.
- During call initiation sequence, the answering modem first sends the answer tone and then transmits a sequence of scrambled "1"s without interruption of carrier signal.
- Modem disconnection upon the reception of a sequence called **Long Space.**
- Transmission of **Long Space** to disconnect the distant modem.
- Absence of **64 consecutive binary** "1" detection.

The following timing diagrams show different BELL 212A sequences.

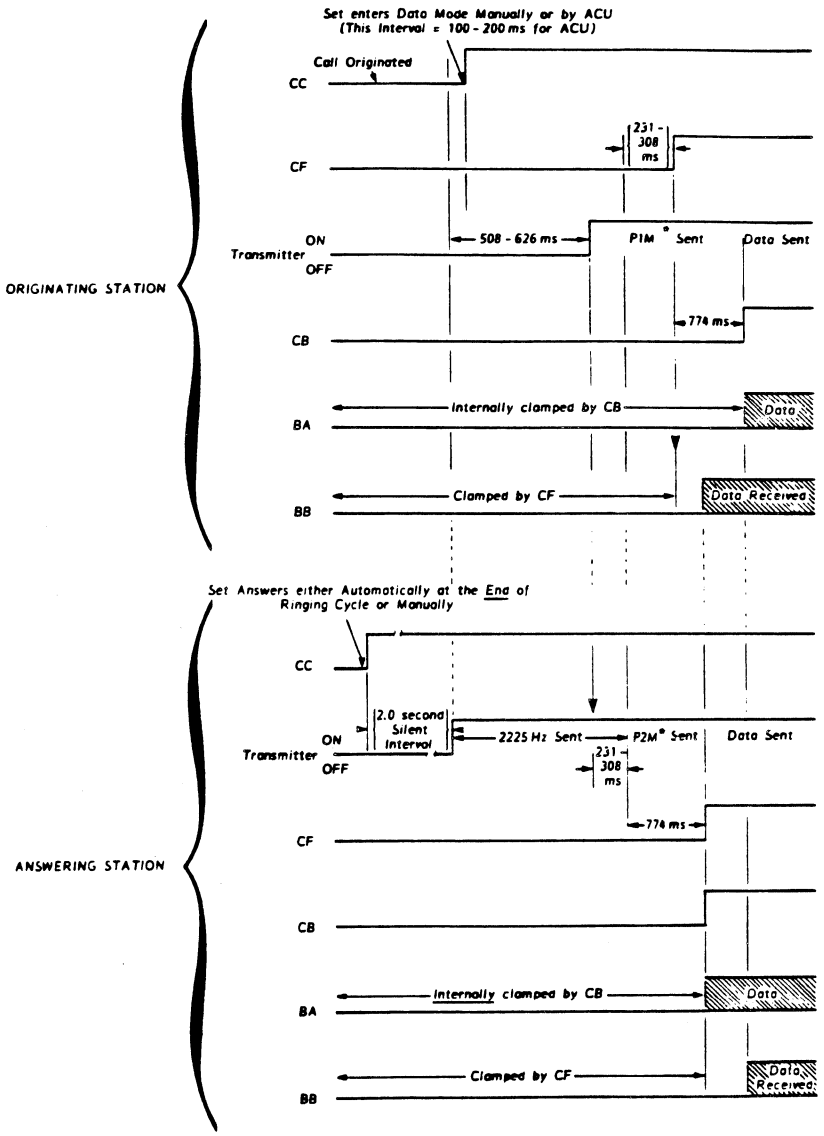
BELL 212A LOW SPEED CONNECT SEQUENCE

CD ON : Either Automatic or Manual Operation



BELL 212A HIGH SPEED CONNECT SEQUENCE

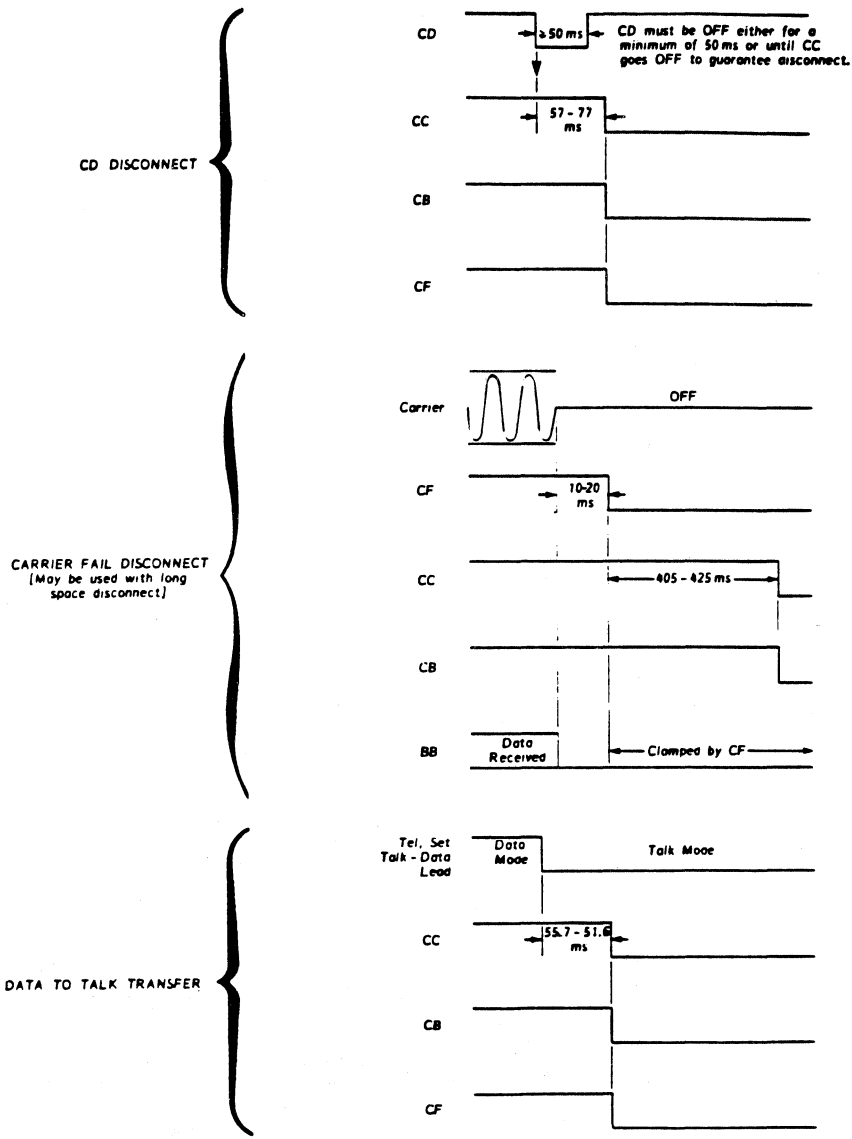
CD ON : Either Automatic or Manual Operation



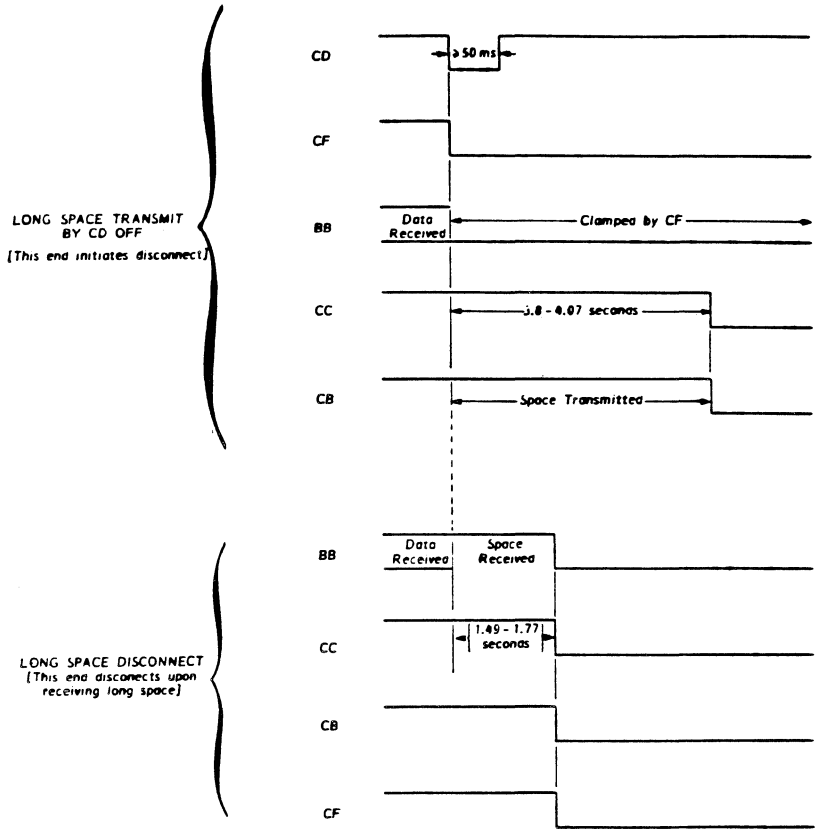
* P1M is the low band phase shift keyed signal representing a marking data sequence.

P2M is the similar signal in high band.

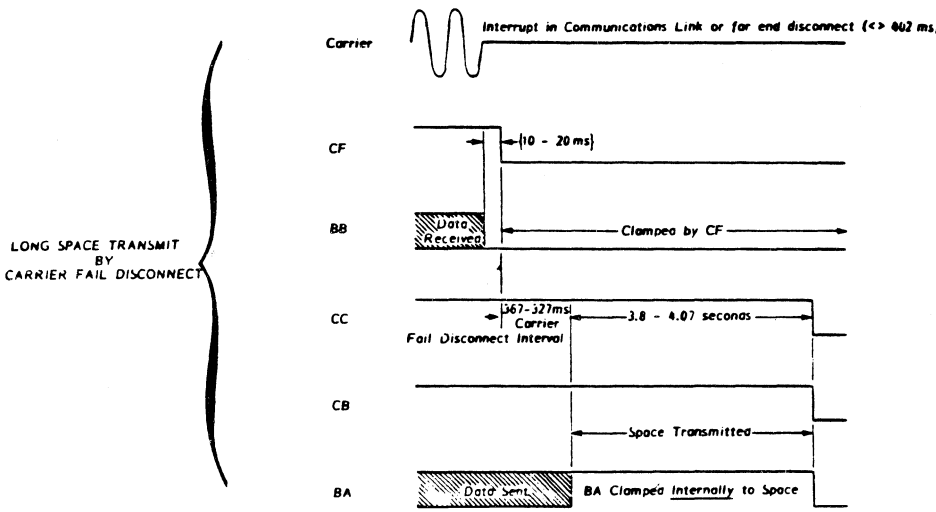
BELL 212A DISCONNECT SEQUENCES (High or Low Speed)



BELL 212A DISCONNECT SEQUENCES (continued)



BELL 212A DISCONNECT SEQUENCES (continued)



EIA CONNECTOR PIN ASSIGNMENTS

Pin Number	Name	Direction	Function
1	-	-	No connection (NC)*
2	BA	To Data Set	Transmitted Data
3	BB	From Data Set	Received Data
4	-	-	NC
5	CB	From Data Set	Clear To Send
6	CC	From Data Set	Data Set Ready
7	AB	-	Signal Ground
8	CF	From Data Set	Received Line Signal Detector
9	+P	From Data Set	Testing Voltage
10	-P	From Data Set	Testing Voltage
11	-	-	NC
12	CI**	From Data Set	Speed Mode Indication
13	-	-	NC
14	-	-	NC
15	DB**	From Data Set	Transmit Signal Element Timing (Data Communication Equipment Source)
16	-	-	NC
17	DD**	From Data Set	Received Signal Element Timing (Data Communication Equipment Source)
18	CN**	To Data Set	Make Busy / Analog Loop
19	-	-	NC
20	CD	To Data Set	Data Terminal Ready
21	RL**	To Data Set	Remote Digital Loop
22	CE	From Data Set	Ring Indicator
23	CH**	To Data Set	Speed Select - Originate
24	DA	To Data Set	Transmit Signal Element Timing-Data (Terminal Equipment Source)
25	CN** or TM**	To Data Set	Make Busy / Analog Loop
		From Data Set	Test Mode

* Protective Ground is provided on a screw terminal.

** May be disconnected from interface via options.

CHAPTER 3 - TSG 7515 APPLICATIONS

3.1 - Introduction

In this chapter, we shall discuss an TSG 7515 - based application implemented in Thomson Semiconducteurs' Application Laboratory - MOS division - EFCIS.

This is a stand-alone application providing for both **V.22** and **BELL 212A** standard requirements.

Following modes of operation are available :

- **Manual call mode**
- **Manual answer mode**
- **Automatic answer mode**

In order to develop a practical configuration in conjuction with the sub-section called line interface (will be explained in detail later), the interface used was deliberately selected among those currently approuved by telecommunications authorities.

3.2 - Application Diagram

The complete application diagram is given at the end of this chapter.

- Modulation - Demodulation, Transmission - Reception Filtering, Asynchronous - Synchronous Conversion, Scrambling - Descrambling Carrier Detection functions are accomplished by TSG 7515.
- A 6805 CT single-chip microcomputer, configured in type 2 open mode, executes the modem management functions.
- The program memory is a 2732 - type PROM containing the object code.
  Since the selected mode of 6805 CT operation uses the available C and D ports for Data and Address Bus, it was as a consequence necessary to add 5 bi-directional ports within the area reserved for this function. This explains the presence of 74 LS 244 and 74 LS 377 devices.
- Interface to the telephone line is implemented by "IRC 2000" of LTT whose characteristics will be detailed later.

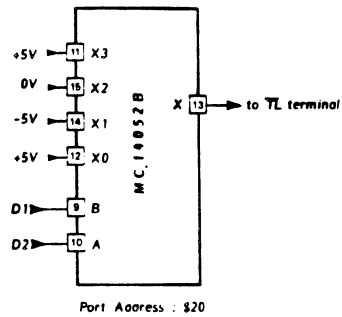
Additional details concerning the application diagram

- **MUX 1 multiplexor** : *allows transmission of messages issued by the microcomputer during connection establishment or loopback answer sequences.*
  (Description of software, chapter 4, explains the occurrence of these events)

- **OR Gate connected to Pin 104** : *Some particular sequences defined by V.22 and BELL 212A recommendations require the connector pin 104 to go to logic "1" in response to the state of V.24 connector pin 109.*

- **MUX 2 , MUX 3 , MUX 4 Multiplexors** : *Some of TSG 7515 terminals have been designed to accept three-state input signals to perform 3 different functions.*
  Suitable translation of these three-state signals is obtained by applying the two logic outputs to an analog multiplexor. Various solutions, two of which are outlined next, are possible.

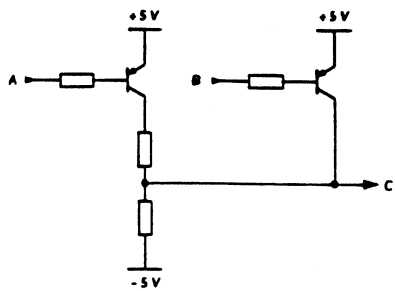
  1 - *Using a "4000" series CMOS multiplexor (e.g. MC 14052 B) as shown below (example of type 2 and type 3 loops).*



Port Address : $20

This solution has the disadvantage of requiring one MC 14052 B circuit or equivalent for each 3-state input.

2 - Using a transistor array as shown below.



A	B	C
+5V	+5V	-5V
0V	+5V	0V
+5V	0V	+5V
0V	0V	+5V

This alternative offers the advantage of using currently available resistor and transistor arrays thereby achieving component count reduction.

- Purpose of adjustable resistors for on-line signal transmission / reception

Telecommunications authorities have established maximum admissible on-line power level transmitted by any device. In order to comply with these strict limits, a combination of fixed and adjustable resistors is used to achieve signal level adjustment.

Resistor bridge on receive channel allows aajustment of complete loop gain so as to enable the carrier detection circuit (internal to TSG 7515) to meet the requirements of V.22 and BELL 212A standards :

High level : - 43 dBm on-line
Low level : - 48 dBm on-line

3.3 - Modem Configuration Switches

16 programming switches are available - some of them are used for the selection of modem's operational status (Data format, channel selection, ...) and the others for monitoring purposes such as maintenance loop, remote loop request, ...

A summary description of these switches is given next.

SW0 : BRS (Binary Rate Selection)

Selects Data Transfer Rate as follows :

SW0 Setting	Binary Rate
1	1200 bits/s
0	600 bits/s (CCITT) 300 bits/s - FSK BELL

SW1 : $\overline{L2}$ (Loop 2)

Configures the modem for type-2 maintenance loop operation.

Type-2 loop is intended to enable the station or the network to monitor the error-free operation of both the line (or a section of the line) and the distant modem.

SW1 Setting	Loop 2
1	Deselected
0	Selected

SW3 : $\overline{L3}$ (Loop 3)

Configures the modem for type-3 maintenance loop operation.

This is a local analog loop used to test modem's correct operation. It should be as close to the line as possible.

In the case of our application, this loop is implemented by disconnecting the modem from line which will cause an imbalance of 4-wire/2-wire converter. (Further details are given later in this chapter)

SW2 Setting	Loop 3
1	Deselected
0	Selected

SW3 : $\overline{C/B}$

Configures the modem for operation in accordance with CCITT V.22 or BELL 212A standards.

SW4 : $\overline{GT}$ (Guard Tone)

In CCITT V.22 mode of operation, enables or disables the transmission of 1800 Hz guard tone.

When SW3 is switched to "1" level, a 1800 $\pm$ 20 Hz guard tone is continuously transmitted while modem is sending in upper channel.

This guard tone is disabled when modem transmits in lower channel.

SW3 Setting	Transmit Channel	
	Lower	Upper
1	Without 1800 Hz	With 1800 Hz
0	Without 1800 Hz	Without 1800 Hz

SW5 : $\overline{SEI}$

Scrambler $\overline{Enable}$ / Disable. Employed for debug mode only.

SW6 : $\overline{A}$ / O ($\overline{Answer}$ / Originate)

Selection of Answer or Originate mode. This switch affects directly the selection of the transmission channel (lower / upper), other channel being automatically assigned to reception.

SW7 : $\overline{ATE}$ ($\overline{Answer\ Tone\ Enable}$)

This switch enables the transmission of the answer tone.
Employed for debug mode only.

SW8 : $\overline{T}$ / D ($\overline{Telephone}$ / Data)

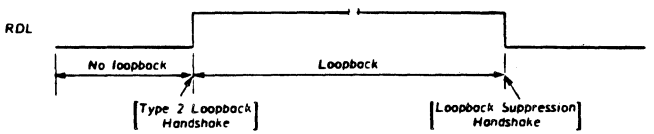
Allows to switch between telephone line (TPH) and Modem (DATA) connections.

SW9 : RDL (Remote Digital Loop)

Used to send loop 2 request to remote modem. This request initiates the loopback handshake sequence.

Signals used for type-2 loopback establishment may be transmitted only after the conclusion of contact initiation procedure for synchronization.

When a type-2 loopback sequence is terminated and when RDL switch returns to "0", the modem sends a loopback suppression instruction.



SW10 : AA (Auto Answer)

Enables or disables modem configuration for auto answer capability to incoming calls.

SW11 : $\overline{S1}$ / A
SW12 : $\overline{S2}$ / A

Synchronous / Asynchronous Mode Selection

SW13 : CLS
SW14 : OSE

In asynchronous mode, selects the character length and configures the modem for overspeed function.

Table next page gives all possible configurations.

$\overline{S1}$ / A	$\overline{S2}$ / A	CLS	OSE	Mode of Operation
0	X	0	0	Synchronous
1	1	0	0	Asyn 9bits (+1% , -2.5%)
1	1	0	1	Asyn 9bits (+2.3% , -2.5%)
1	1	1	0	Asyn 10bits (+1% , -2.5%)
1	1	1	1	Asyn 10bits (+2.3% , -2.5%)
1	0	0	0	Asyn 8bits (+1% , -2.5%)
1	0	0	1	Asyn 8bits (+2.3% , -2.5%)
1	0	1	0	Asyn 11bits (+1% , -2.5%)
1	0	1	1	Asyn 11bits (+2.3% , -2.5%)

X : Don't care

Remarks concerning the above table

1 - When the application board is configured for **synchronous operation**, it is **strictly forbidden** to set CLS and OSE switches to any state other than "0". Any other setting will configure the TSG 7515 for factory test configurations.

In chapter 4 (Description of Software) the inclusion of this illegal configuration is illustrated.

2 - Note that the following configurations are not available in either asynchronous or BELL 212A modes of operation :

- CLS = 8bits & CLS = 11bits
- OSE = +2.3% , -2.5%

The integrated firmware will alert the user of any illegal configuration.

SW15 : $\overline{RTS}$

Disables the data transmission. Employed for debug mode only.

3.4 - *Terminal Interface*

Terminal to Application board interconnection is implemented via a 25-pin connector (ISO 2110 standards) mounted on the Printed Circuit Board.

This interface meets both CCITT V.24 / V.28 and EIA RS-232C specifications.

CCITT : Comité Consultatif International Télégraphique et Téléphonique.

EIA : Electronic Industries Association.

The following table gives a list of interface connector pins.

Pin Number	CCITT Circuit Number	French Designation	American Designation	Signal Direction Terminal ← → Modem
2	103	ED	BA	→
3	104	RD	BB	←
4	105	DPE	-	→
5	106	PAE	CB	←
6	107	PDP	CC	←
7	102	TS	AB	0 volt
8	109	DS	CF	←
12	112	-	CI	←
15	114	HEM	DB	←
17	115	HRM	DD	←
20	108	CPD	CD	→
22	125	IA	CE	←
24	113	HET	DA	→
25	142	IE	TM	←

3.5 - Line Interface

This is a hybrid device inserted between TSG 7515 and the telephone line.

In general, it performs the following functions :

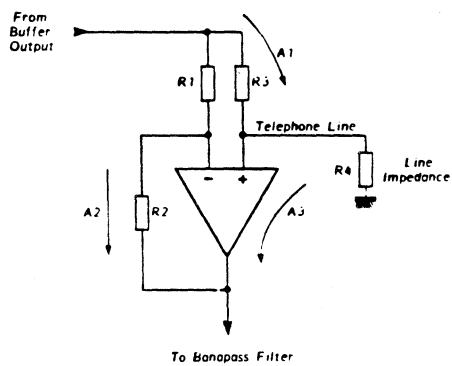
- **4-wire / 2-wire conversion**
- **Line current regulation**
- **Overvoltage protection**
- **Ring detection**
- **Pulse dialing**
- **Telephone / Data switching**
- **Galvanic Isolation**

3.5.1 - 4-wire /2-wire conversion

This configuration employs an operational amplifier - whose duty is to route signals issued by the modulator towards the telephone line - while preventing, by as much as possible, the signal reinjection into the demodulator.

Inversely, it routes the signal received via line towards the demodulator with minimal attenuation.

Figure below illustrates the arrangement of a popular 4-wire / 2-wire converter.



The gain between the on-line signal and modulator's output is :

$$A1 = \frac{R4}{R3 + R4}$$

Where R4 is the Line Impedance theoretically considered as 600Ω resistive.

If the line is properly matched, R3 must be equal to R4 :

$$i.e.\quad R3 = R4 = 600\Omega$$

$$therefore : A1 = 0.5$$

The gain between the modulator and the demodulator (banapass filter) is given by the following expression :

$$A2 = -\frac{R2}{R1} + \left(1 + \frac{R2}{R1}\right)\left(\frac{R4}{R3+R4}\right)$$

To obtain a null signal reinjection : $A2 = 0$

$$i.e.\quad 0 = -\frac{R2}{R1} + \left(1 + \frac{R2}{R1}\right)\frac{1}{2}$$

after simplification : $\underline{R2 = R1}$

The gain between the demodulator and the line :

$$A3 = 1 + \frac{R2}{R1}$$

$$therefore : \underline{A3 = 2}$$

It is obviously clear that these calculations are purely theoretical. In practice, the line impedance has a complex component whose value varies as a function of the frequency. However, the 4-wire / 2-wire converter is consiaered as acceptable if the Gain "A2" is approximately **- 10 dB.**

Further discussion on this topic is beyond the scope of the present application note. The interested reader is advisea to refer to specialized text books for a full coverage of this subject.

3.5.2 - *Galvanic Isolation*

This isolation is achieved by a transformer whose rating should be higher than **1 500 volts.**

3.5.3 - Line current Regulation

The on-chip regulation circuitry maintain the line current within two limits, which vary from country to country according to specifications in force.

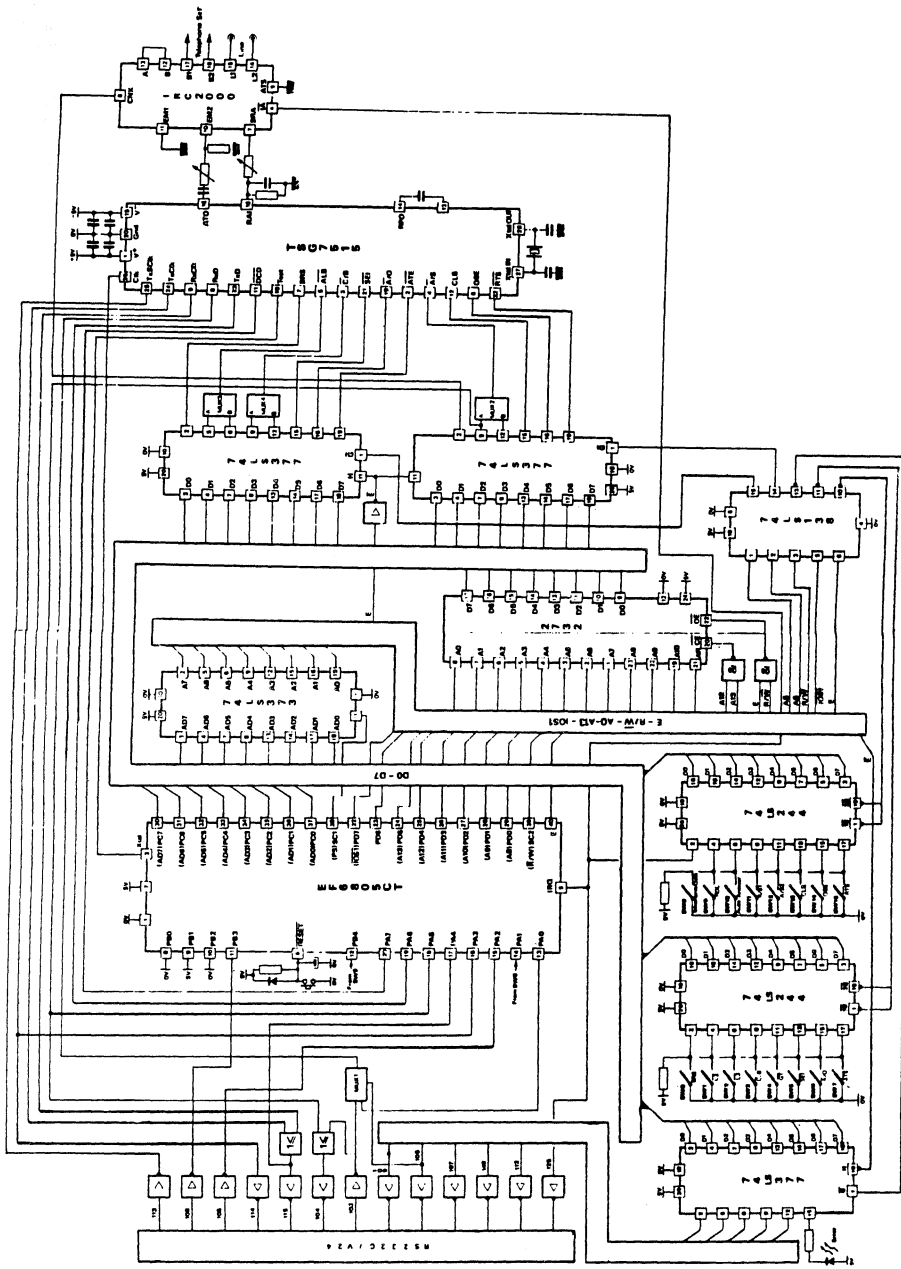
Line interface Device	Max. Current (mA)	Min. Current (mA)
IRC 2000	50	20

3.5.4 - Ring Detection

In general, this output delivers a logic signal corresponding to ring signal envelope.

3.5.5 - Pulse Dialing

In the case of IRC 2000, this pin delivers loop disconnect pulses for dialing and modem connection. In addition, it offers the possibility of telephone connection / disconnection.



CHAPTER 4 - DESCRIPTION OF SOFTWARE

4.1 - Definition of software modules

Each individual module given in this chapter is intended for a particular function. They cover the occurrence of events sequentially from the time of modem's initial power on until the completion of on-line information transfer.

4.1.1 - Idle State Management Module

- *Microcomputer configuration*
- *V.24 connector initialization*
- *Interface disconnection from line*
- *Read the settings of programming switches, monitor absence of error and configure the TSG7515 according to switch settings.*
- *Loop 3 management*
- *Wait for an event causing connection to line*

4.1.2 - CCITT Handshake Module

- *V.25 sequence*
- *Answer handshake*
- *Originate handshake*

4.1.3 - BELL Handshake Module

- *1200 Originate handshake*
- *300 Originate handshake*
- *Answer handshake*

4.1.4 - CCITT Transmission Module

- *Telephone line monitoring (appearance of special sequences)*
- *V.24 connector management*
- *Monitoring several switch settings*
- *Monitoring $\overline{DCD}$ terminal of TSG7515*

4.1.5 - BELL Transmission Module

Identical to preceding CCITT module. In addition, it provides for the identification of "Long Space" for line disconnection.

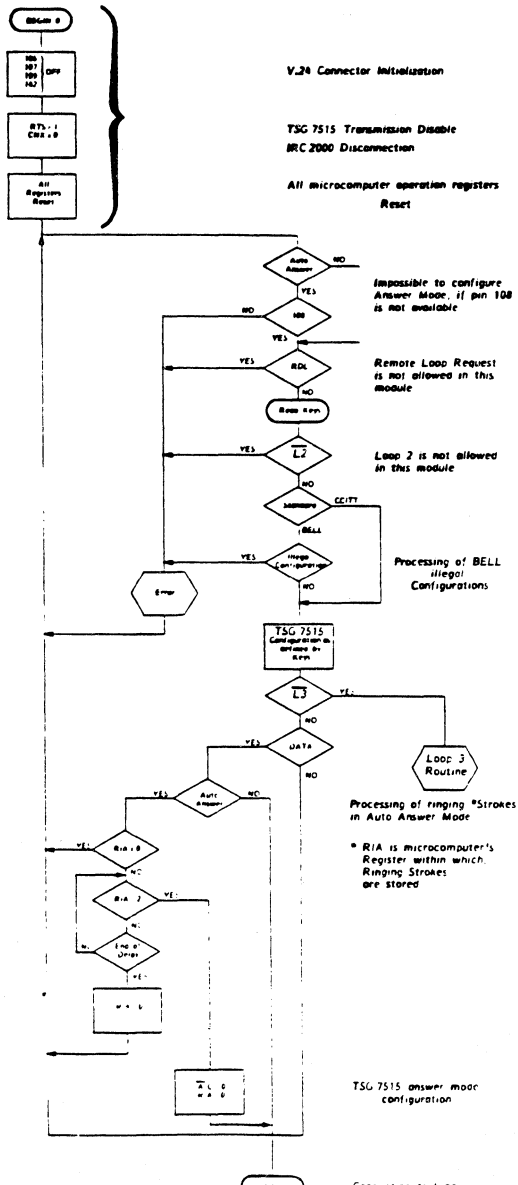
4.1.6 - RDL Handshake Module

Protocol used for the initiation of remote loop sequence.

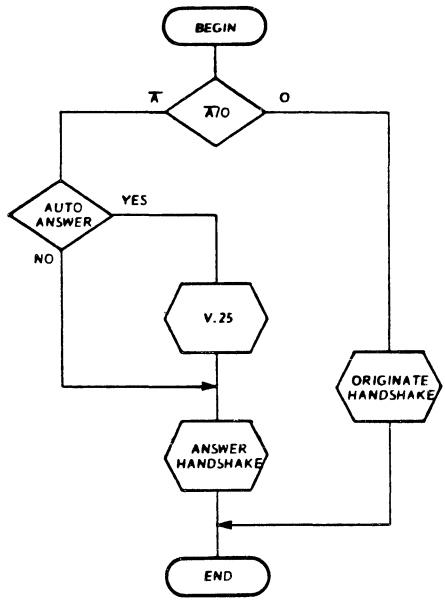
4.1.7 - Loop 2 Receive Handshake Module

Protocol for the reception of type-2 loopback request initiated by distant modem.

Idle State Management Module

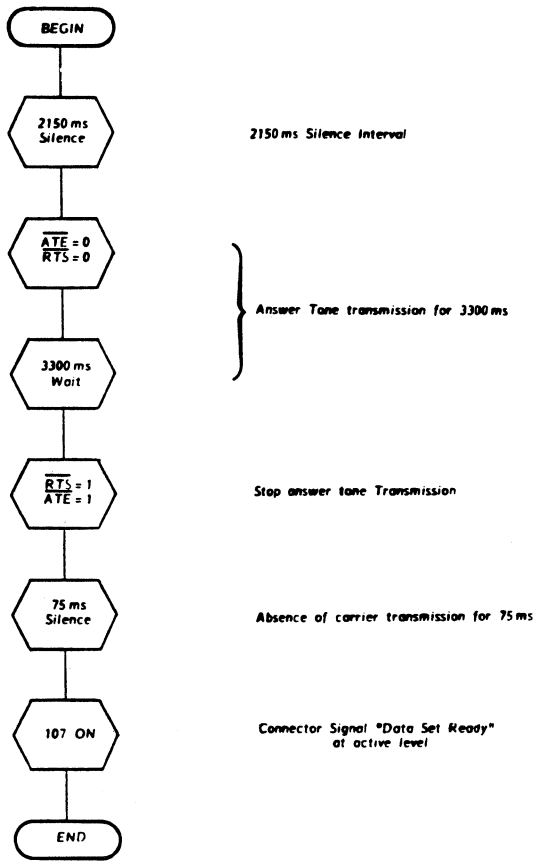


CCITT Handshake Module



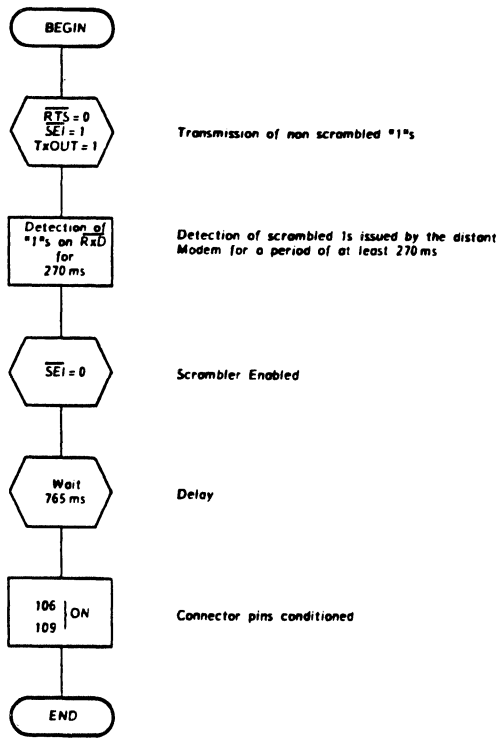
This flowchart illustrates clearly the sequence of events. In the case of manual answer, the software will ignore the V.25 module.

V.25 Sequence



Comment : Writing this sequence meets no difficulty.
Only, CCITT recommendations must be carefully observed.

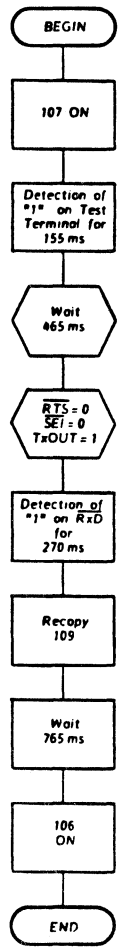
Answer Handshake Sequence



Comments : Detection of scrambled "1" on $\overline{RxD}$ terminal for an interval of 270 ms is performed as follows :

The sequence begins within a loop searching to detect a logic "1" on $\overline{RxD}$ terminal while simultaneously, a 15-second **"time out"** is initiated. If within the loop a logic "0" is detected on $\overline{RxD}$ pin, 270 ms count is reset but the **"time out"** continues. The software sequence will return to the starting point (i.e. idle state management), if at the end of 15-second interval a sequence of continuous "1"s for a 270 ms duration has not been found.

Originate Handshake



This interval corresponds to the period during which the distant Modem transmits non scrambled "1"s.

Delay

Transmission of scrambled "1"s

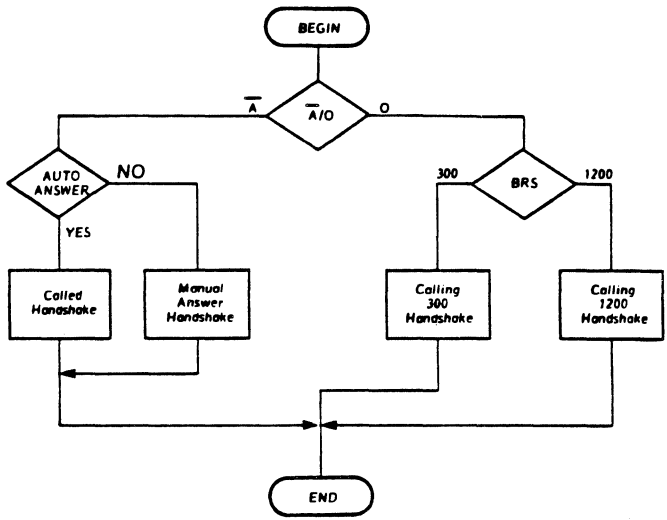
Detection of scrambled "1"s issued by distant Modem

Connector pin 109 conditioned

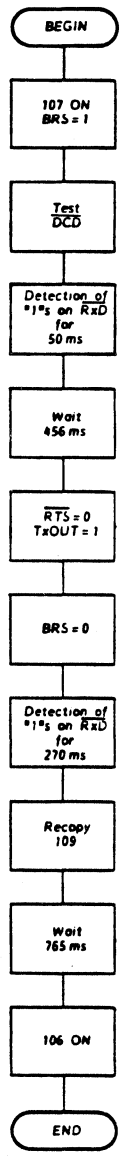
Delay

Connector pin 106 conditioned

BELL Handshake Module



1200 Originate Handshake



Change to FSK mode

Test to detect presence of 2225 Hz

Delay

Transmission of scrambled "1"s

Change to DPSK mode

Detection of scrambled "1"s sequence originated by distant modem

Connector configuration

Delay

Connector configuration

Important Note on this Module next page

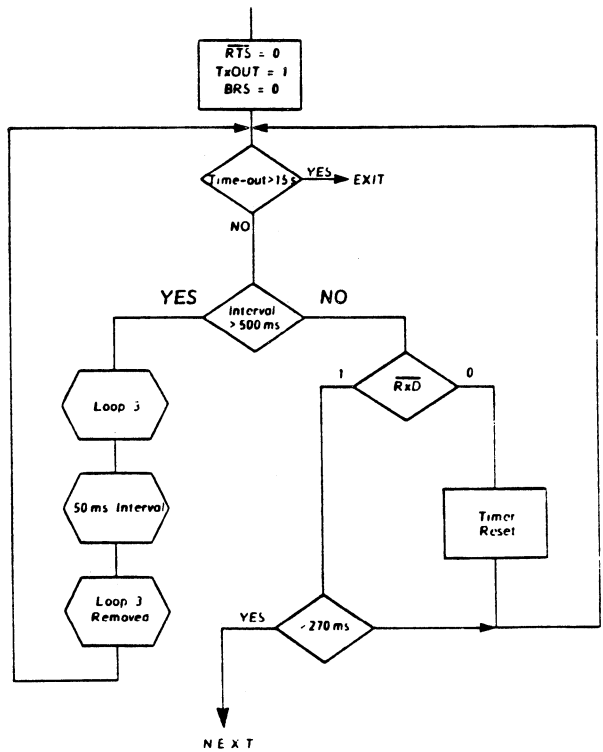
Important : *Sequence of events in Bell Answer Mode differs slightly from equivalent CCITT sequence as follows :*

There is no transistion between the transmission of Answer Tone and Scrambled "1"s Sequence.

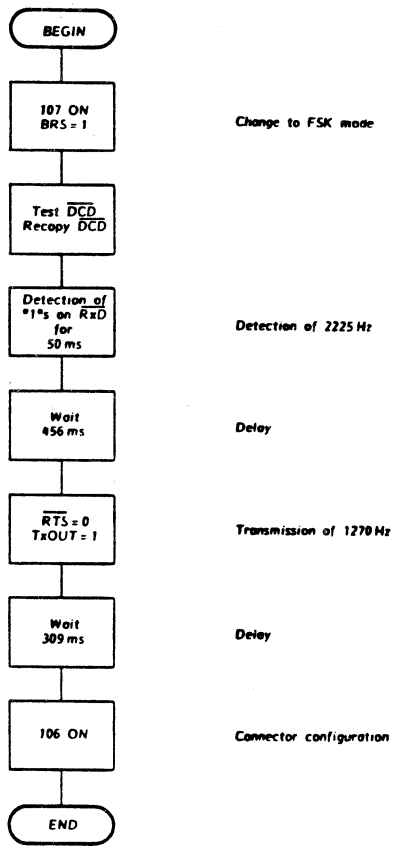
In the case of TSG 7515 and upon the appearance of scrambled "1"s sequence, this may result in "Carrier DPLL" locking on an incorrect frequency.

An efficient solution to overcome this problem would be to program the TSG 7515, for a short interval, in loop 3 configuration.

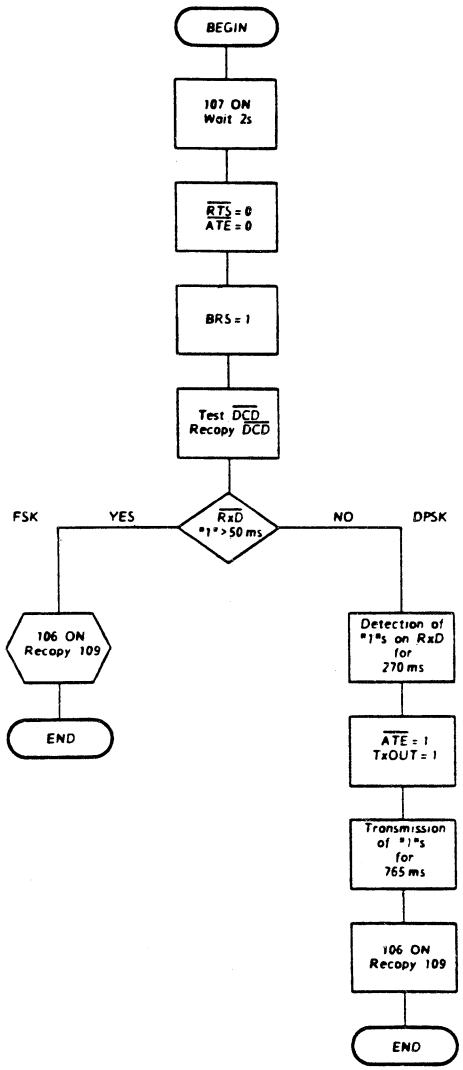
The following flowchart illustrates this recommended solution.



300 Originate Handshake



Answer Handshake



2 seconds Silent Interval

Answer Tone Transmission

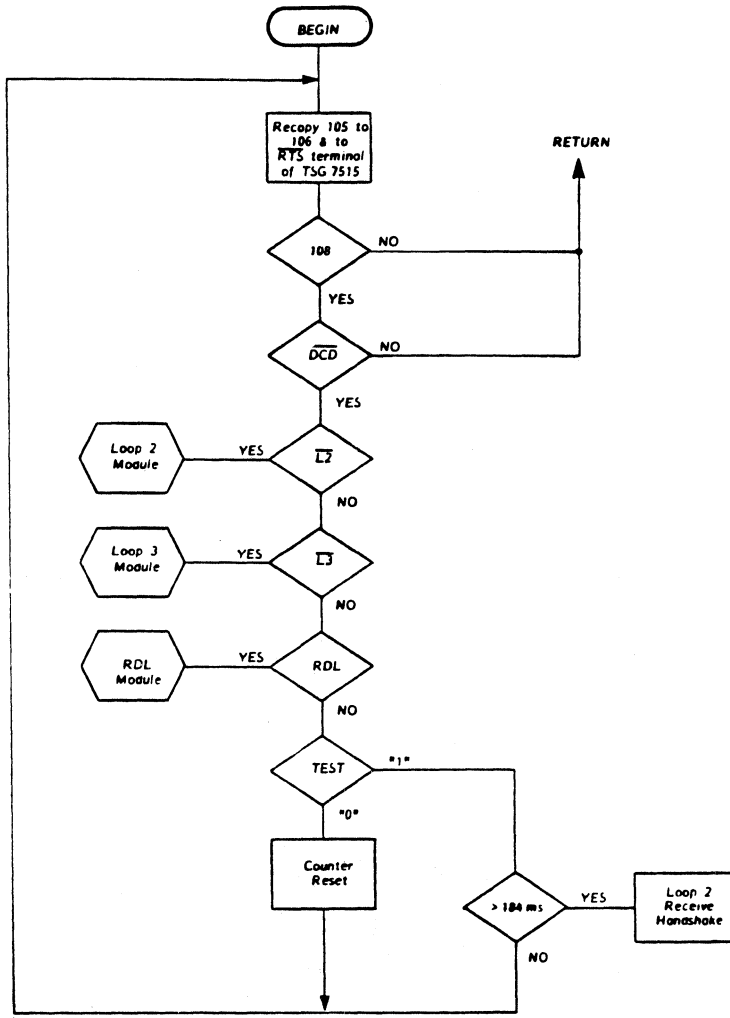
Change to FSK mode

Check for the presence of carrier

Test the speed of the calling station

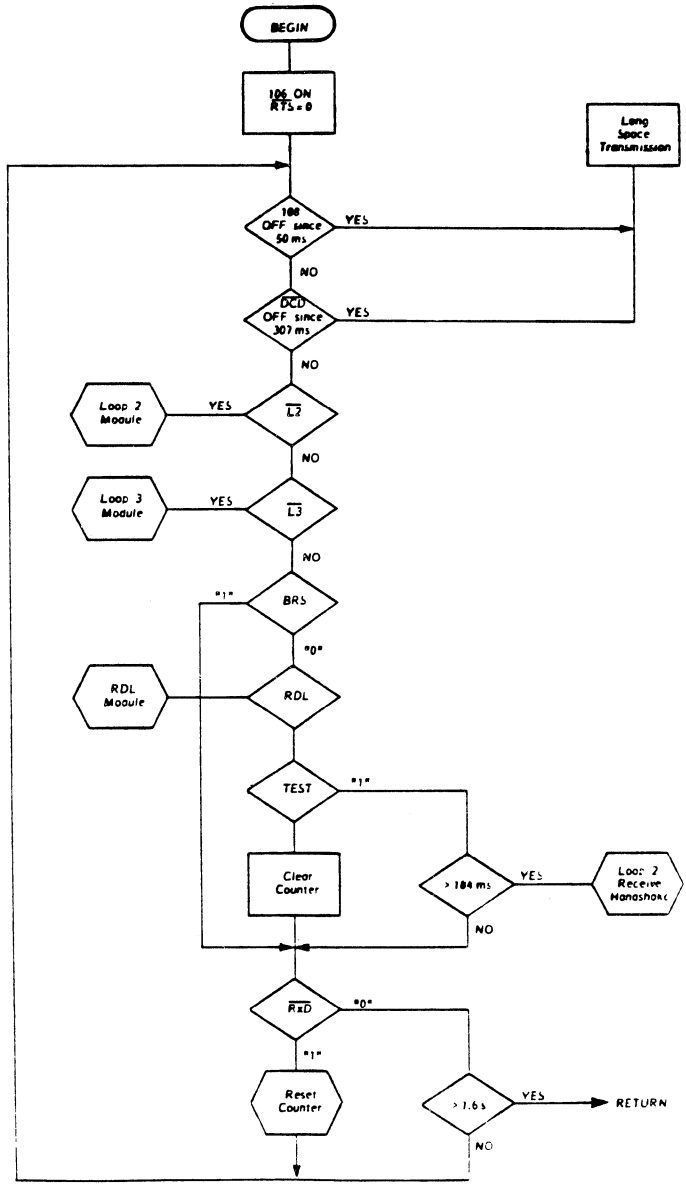
Connection to FSK or DPSK Answer Module

CCITT Transmission Module

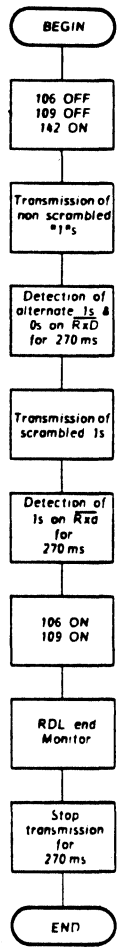


The duty of this module is to monitor either the user connector to detect a line disconnect sequence, or to monitor the telephone line since programming switch settings may cause occurrence of special on-line sequences.

BELL Transmission Module



RDL Handshake Module



Configuration of the user connector

Transmission of RDL Request Sequence

Detection of Answer to this Request

End of RDL Request Signal and transmission of scrambled "1"s

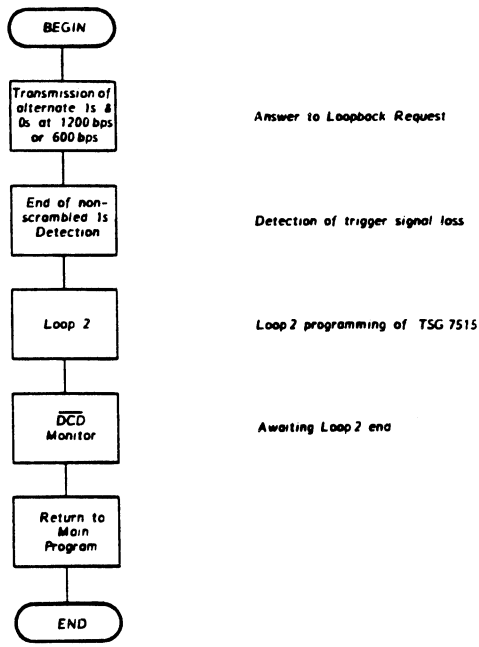
Detection of signal "echoed" by distant Modem on RxD terminal

Configuration of the user connector

Monitoring of RDL key

Transmission of loopback suppression sequence

Loop 2 Receive Handshake Module



APPENDIX A - TSG 7515 HANDLING PRECAUTIONS

A.1 - Power supplies decoupling and layout considerations

Power supplies to digital systems may contain high amplitude spikes and other noise. To optimize performances of the TSG 7515, operating in close proximity to digital systems, supply and ground noise should be minimized. This involves attention to power supply design and circuit board layout.

The power supplies should be bypassed with tantalum or electrolytic type capacitors to obtain noise-free operation. These capacitors should be located close to the TSG 7515. The electrolytic type capacitors should be bypassed with ceramic capacitors for improved high frequency performance.

Power supply connections should be short and direct. Ground loops should be avoided.

Coupling between analog inputs and digital lines should be minimized by careful layout. The RDI input (pin 13) is extremely sensitive to noise. The connection between this point and RFO (pin 14) through a ceramic type capacitor should be as short as possible and coupling between this connection and digital signals should be minimized by careful layout.

A.2 - Carrier Recovery Loop

The carrier recovery loop utilizes a digital phase-locked loop. Performances of the TSG 7515 depend directly on this DPLL which needs to be reset prior to the reception of a DPSK carrier.

TSG 7515 offers three possibilities of resetting this DPLL :

- A trailing edge on $\overline{DCD}$ terminal
- Switching from FSK mode to DPSK mode.
- Changing the receive channel

These three possibilities of resetting the DPLL should be integrated within the microcontroller so as to provide for various set-up and handshake procedures.

Timing diagrams given in chapter 2 illustrate examples of V.22 / V.25 and BELL 212A received signals in originate mode.

A.3 - Frequency Precision of Crystal Oscillator

In order to meet the frequency precision of the transmission baud rate required by V.22 and BELL 212A specifications, it is recommended to use a crystal oscillator whose series resonance frequency precision is better than 0.01% with respect to the theoretical frequency of 4.9152 MHz.

Such precision would be feasible by optimizing the capacitance values spread around the quartz oscillator.

APPENDIX B - GLOSSARY OF TERMS

Acoustic Coupler : A device that permits the use of a telephone handset as a connection to dial-up telephone lines (rather than a direct connection using DAA interface) for data transmission by means of sound transducers. Usually implemented for call origination, and is frequently used with portable terminals.

Analog Loopback : A diagnostic mode whereby the transmitted analog output is internally connected to the analog received signal input in a single band (determined by $\overline{A}/O$ pin) so that the device's entire signal path is under test.

Answer Tone : A tone returned by the answering modem to the originating modem and the network.

A S C I I : American Standard Code for Information Interchange. This is a seven-bit-plus-parity code established by the American National Standards Institute (Formerly American Standards Association) to achieve compatibility between data services. Also called USASCII.

Attenuation : The difference between transmitted and received power due to transmission loss through equipment, lines or other communications devices.

Asynchronous Transmission : A data transmission scheme that handles data on a character-by-character basis (without synchronization by a clocking signal). Time intervals between transmitted characters may be of unequal length. The character code includes a "**start**" bit to identify the beginning of a data character, a "**stop**" bit (or bits) to identify the end of the data character and a "**parity**" bit to check for errors in transmission. Also called "**Start-Stop**" transmission.

Auto-Answer : A circuit in a modem system that can automatically make a connection on the switched telephone system when its number is dialed.

Automatic Dialer : A device which will automatically dial telephone numbers on the switched telephone network. An automatic dialer can be easily incorporated into a TSG 7515-based modem system.

Bandpass Filter : A filter circuit that passes a single band of frequencies and filters out, or excludes, all others.

Bandwidth : The range of frequencies assigned to a channel or system; the difference expressed in Hertz (Hz) between the highest and lowest frequencies of a band.

Baud : A unit of signalling speed equal to the number of modulations or signal events per second. In FSK synchronous transmission, the unit of signalling speed corresponding to one unit interval per second ; that is, if the duration of the unit interval is 20 milliseconds, the signalling speed is 50 baud. Baud is the same as "**bits per second**" only if each signal event represents exactly one bit, as in the frequency-shift keyed TSG 7515 modem.

As used in the TSG 7515 four-phase PSK transmission, every two bits of digital data are encoded into dibits (1dibit = two bits) for translation or modulation into phase shift information. In PSK the baud rate is one-half the bit rate.

Bit Error Rate (BER) : A measurement of the average number of bits transmitted before an error occurs. Usually expressed as the reciprocal of the average.

GLOSSARY OF TERMS (continued)

Bit Rate : For modems using voicegrade telephone lines, the bit rate equals the data rate. The baud rate is the actual number of times per second that the transmited carrier is modulated or changes state. Each modulation may represent multiple bits.

Carrier : An analog signal fixed in amplitude and frequency that can be combined in a modulation process with a second information-bearing signal to produce a signal for transmission.

C C I T T (Comité Consultatif International de Télégraphie et Téléphonie) : An international committee established by the United Nations to recommend international telecommunications standards of transmission within the International Telecommunications Union (ITU).

Channel : A communications path providing signal transfer in a single direction at a time.

Circuit Grade : The grades of circuits are broadband, voice, sub-voice and telegraph. Circuits are graded on the basic line speed expressed in characters per second, bits per second, or words per second.

Coherent Detection : A method of phase-shift detection, used in the TSG 7515 PSK modem, in which the received modulated signal is compared with a purified and locally-generated reference frequency, instead of using the instantaneous value of the received carrier frequency (which is often distorted).

Common Carrier : A company which dedicates its facilities to a public offering universal communications services and which is subject to public utility regulations.

D A A (Data Access Arrangement) : Originally this term was used to define a device, provided by the telephone company, which was used to connect privately owned or customer provided equipment (data sets) to the switched telephone network.

dB (Decibel) : The decibel is defined by the ratio of output signal power to input signal power as **dB = 10 * Log 10 (Output Power)**.

Note that if the output power is less than the input power, the logarithmic result is negative. In this case the line is said to have a loss of that many dB.

dBm : Input and output signal powers may be related to a specific level called a dBm for reference purposes. Zero dBm (log 1 = 0) equals 1mW dissipated in 600 Ω impedance. The reference frequency used in most circuits is 1000 Hz. Measurements relative to reference frequency are expressed in decibels relative to 1 mW as follows :

dBm = 10 * log 10 (Signal Power in mW/1mW)

Thus, zero dBm means 1mW and absolute power levels may be expressed as so many dBm.

dBSPL : In acoustics, the unit commonly utilized to measure sound pressure level or dBSPL. The zero reference for this measurement is 0.0002 dynes per square centimeter.

GLOSSARY OF TERMS (continued)

dBv : Microphone sensitivities are commonly related to a specific level called a dBv for reference purposes. Zero dBv (log 1 = 0) represents one mW dissipated in 1000 Ω impedance . The unit dBv is expressed in terms of the peak voltage of a signal referenced to one volt.

$$dBv = 20 * \log 10 \text{ (Peak Voltage of Signal / 1 volt)}$$

D C E (Data Communications Equipment) : Consists of the modem and any other equipment related to the transmission or reception of analog signals over the telephone lines, such as the FCC-approved Registered Protective Circuit.

Data Set : - A modem,
- A collection of similar and related data records.

D T E (Data Terminal Equipment) : The digital equipment to which a data communications path begins or ends.

Demodulator : A component of a modem which recovers data from received analog signals and converts them to a form suitable for the DTE.

Descrambler : A device or circuit that transposes or decodes a demodulated signal to restore the original data prior to transmission by the remote transmitter and scrambler.

Digital Loopback : A means of routing data from the transmit path back to the received data path by switches, as a means of testing a modem.

Equalization : Compensation for the increases of attenuation with frequency. Its purpose is to produce a flat frequency response.

F S K (Frequency Shift Keying) : A method of frequency modulation which varies the carrier frequency at significant instants by smooth as well as abrupt transitions.

Full Duplex : Simultaneous two-way independent transmission in both directions on a communications channel. Also called **Duplex.**

Cross Distortion : Distortion is an undisred change in a signal or data transmission. The primary sources of distortion in modem communication are in speed differences between the Data Terminal Equipment (DTE) and the modem, and circuit variations and noise. The maximum gross (total) distortion in modem communication is 45%, as defined by EIA standard RS-404.

Half Duplex : A circuit designed for transmission in either direction, but not in both directions simultaneously. A modem in half-duplex mode will be either transmitting or receiving, but not both at the same time.

Handshaking : An exchange of predetermined signals when a connection is established between two modems.

Host Computer : A computer attached to a network providing primary services such as computation, data base access, special programs, or programming languages.

Information Bit : A bit generated by the data source which is not used for error control.

Impulse Noise or Surge : A type of high-amplitude short-duration interference on communications lines caused by events such as lightning, electrical sparking action, make/break action of switching devices, or electrostatic discharge. A registered protective network is required to protect the modem from such voltages which occur on communications lines.

GLOSSARY OF TERMS (continued)

Mark : A logic one, or the presence of current or carrier on a digital communications channel in the idle condition. Compare with space.

Parity Check : Addition of non-information bits to data, making the number of ones in each group either always even (for even parity) or odd (for odd parity). This permits single error detection in each group.

Phase Locked Loop : An electronic servo system controlling an oscillator so that it maintains a constant phase angle relative to a reference signal source.

P S K (Phase-Shift Keying) : A type of phase modulation in which the modulation function shifts the instantaneous phase of the modulated wave between predetermined discrete values.

Protocol : A procedure used to control the orderly communications between stations on a data link. Examples of protocols are HDLC, SDLC, and Synchronous Bit-Oriented protocols.

Q A M (Quadrature Amplitude Modulation) : One form of 4-level differential Phase-Shift Keying.

Reference Clock : A clock of high stability and accuracy used to govern the frequency of a network of mutually synchronized clocks of lesser stability.

R D L (Remote Digital Loopback) : A type of test in which a signal is transmitted from a local modem to a remote modem, or other device or switch, to loop the remote received data back to the sending modem to measure or test the modem, communications line, remote modem or device, or the entire circuit.

Scrambler : A device or circuit that encodes a data signal at the transmitting modem, to make it unitelligible for data security purposes (at a receiver not equipped with an appropriate descrambler), and to maintain carrier detect lock during idle or slow data rate input.

Serial Transmission : A method of transmission in which each bit of information is sent sequentially on a single channel, rather than simultaneously on several channels, as in parallel transmission.

S N R (Signal-to-Noise Ratio) : The ratio of the signal power to the noise power on a communications line, expressed in dB.

Space : A logic zero, or the absence of current or carrier on a digital communications channel. Compare with Mark.

Start Element : In character synchronous (start-stop) transmission, the first element in each character, which serves to prepare the receiving equipment for the reception and registration of the character.

Start-Stop Transmission : Asynchronous transmission in which a group of code elements are preceded by a start element (or bit) and ended with a stop element (or bit).

Statistical Equalizer : A modem compensation circuit which provides equalization of a communications line based on the average switched telephone line circuit distortion.

GLOSSARY OF TERMS (continued)

Stop Element : In character asynchronous (start-stop) transmission, the last element in each character, to which is assigned a minimum duration, during which the receiving equipment is returned to its rest (idle) condition in preparation for receiving the next character.

Switched Line : A communications link for which the physical path may vary each time it is used, as in the dial-up (switched) public telephone network.

Synchronous Transmission : A data transmission scheme in which the data characters and bits are transmitted at a fixed rate with the transmitter and receiver synchronized. This eliminates the need for start-stop elements, thus providing greater efficiency.

APPENDIX C - BIBLIOGRAPHY

- American Telephone and Telegraph Company
  Bell System Reference Data Set 212A Interface Specifications
  PUB 41214 - January 1978

- Comité Consultatif International Télégraphique et Téléphonique
  Communications de Données sur le Réseau Téléphonique
  Avis de la série V - Genève Novembre 1980

- Thomson Semiconducteurs
  EFG 7515 Advance Information Data Sheet

- Electronic Industries Association
  EIA Standard : RS-232C Interface between Data Terminal Equipment and Data Communication Equipment Employing Serial Binary Data Interchange
  August 1969

Designed to interface an equipment with the telephone line, this 8 pins IC provides:
- Line adaptation.
- Ring detection.

It is particularly convenient for modem applications and fulfills a wide range of international specifications.

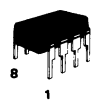
Line adaptation: (DC characteristic)
- Zener characteristic with adjustable slope.
- Adjustable dynamic impedance.
- Adjustable maximum amplitude of the signal.
- Use only a low cost dry transformer.
- Need no dialling relay.

Ring detection:
- Adjustable detection level.
- Adjustable AC impedance.
- Very low line distortion.
- Logic signal output.

Other:
- Low working voltage.
- Wide operating current range.

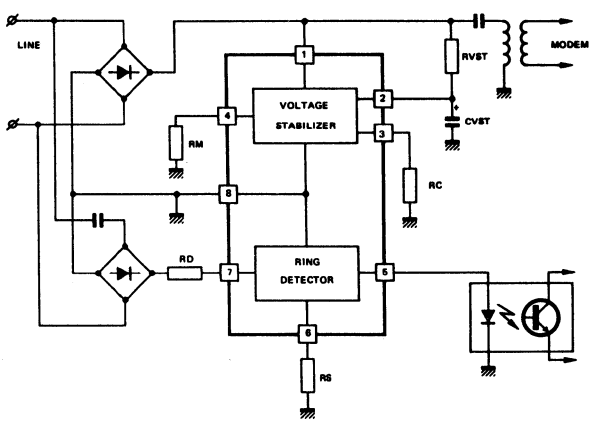
LINE INTERFACE

CASE CB-98

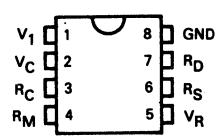


PLASTIC PACKAGE

BLOCK DIAGRAM



PIN ASSIGNMENT



PIN DESCRIPTION

VOLTAGE STABILIZER

Name	No.	Description
V_1	1	Voltage over the IC
V_C	2	C_{VST} decouples the voltage stabilizer and R_{VST} fixes the impedance
R_C	3	R_C fixes the voltage through R_{VST}
R_M	4	R_M fixes the slope of the DC characteristic
GND	8	Ground

RING DETECTOR

Name	No.	Description
V_R	5	Ring detection output connected to an optocoupling device
R_S	6	R_S fixes the ring detection level
R_D	7	Ring detection input. R_D fixes the impedance of the ring detector

Outlines

Specially designed for the modem applications, this 8 pins IC provides line adaptation, ring detection and easy pulse dialling. It is a Direct Connect Circuit (DCC) which has been designed to fulfill a wide range of AC and DC specifications for various countries.

Ring dectection

This circuit detects the incoming ringing signal and generates a logic signal to the microcomputer via an optocoupling device. The detection level can be fixed by an external resistor. The dynamic impedance of the ring detector is also fixed by an external resistor. The line distortion of the ringing signal is very low compared to the distortion introduced by a zener detector.

Line adaptation

The DC characteristic can fulfill a wide range of DC specifications:

— zener characteristic with adjustable slope fixed by an external resistor,
— line current limitation using an external CTP.

The dynamic impedance is fixed by an external resistor R_{VST} so as to match with different line impedances.
The maximum amplitude of the signal is fixed by two external resistors R_{VST} and R_C.
This circuit has been designed to be connected to a low cost dry transformer.
The application has been studied to avoid the use of dialling relay.
With its possibility of ring detection, off-hook and dialling this circuit is adapted to the application in smart modems. Is also satisfies the FCC Rules Part 68.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply voltage	V_1 V_7	16 16	V V
Power dissipation	P_{tot}	600	mW
Operating temperature	T_{oper}	− 25 to + 65	°C
Storage temperature	T_{stg}	− 55 to + 150	°C

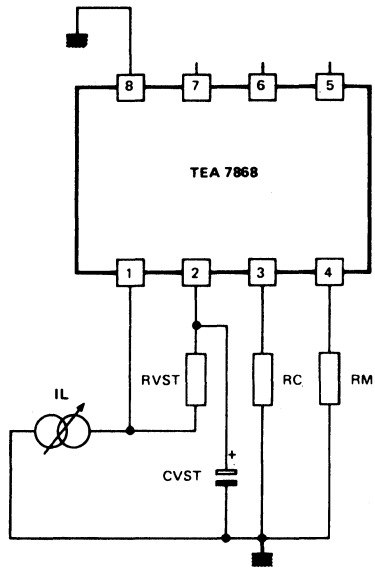
STATIC ELECTRICAL CHARACTERISTICS:
$T_{amb} = 25°C$

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Line current (Pin 1)	I_L	10	—	120	mA
Voltage over the IC (Pin 1) See note 1 I_L = 10 mA I_L = 100 mA	 V_1 V_1	 — —	 3 4.5	 — —	 V V
Voltage stabilizer (Pin 2) See note 1 I_L = 10 mA I_L = 100 mA	 V_C V_C	 — —	 2.1 3.5	 — —	 V V

DYNAMIC ELECTRICAL CHARACTERISTICS:
$T_{amb} = 25°C$

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Impedance of the transmission part. See note 2 Return loss compared to 600 Ω: 300 Hz < f < 5 kHz	 R.L.	 15	 —	 —	 dB
Ring detection level (See note 3) For a low level on pin 5 (< 0.3 V) : no detection For a high level on pin 5 (> 0.8 V) : ring detection	V_R	 18 —	 20 20	 — 22	Vpp
Impedance of the ring detection part: Typically $R_S + R_D/13$ (See note 3)	Z_R	9.5	10.5	11.5	kΩ
Distortion in ring mode: f_{Ring} = 50 Hz (See note 4)		—	—	—	—

Note 1: Static electrical characteristic test diagram:



External components:

$C_{VST} = 100\ \mu F$ $R_{VST} = 1.2\ k\Omega$

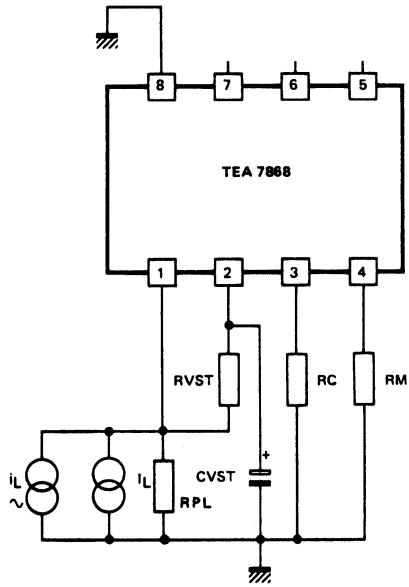
$R_C = 2.7\ k\Omega$ $R_M = 12\ \Omega$

Test conditions:

for: $I_L = 10$ mA $V_1 = 3.2$ V
and $V_C = 2.1$ V

for: $I_L = 100$ mA $V_1 = 4.5$ V
and $V_C = 3.4$ V

Note 2: Impedance measurement:



External components:

$C_{VST} = 100\ \mu F$ $R_{VST} = 1200\ \Omega$
$R_C = 2.7\ k\Omega$ $R_M = 12\ \Omega$
$RPL = 1200\ \Omega$

Test conditions:

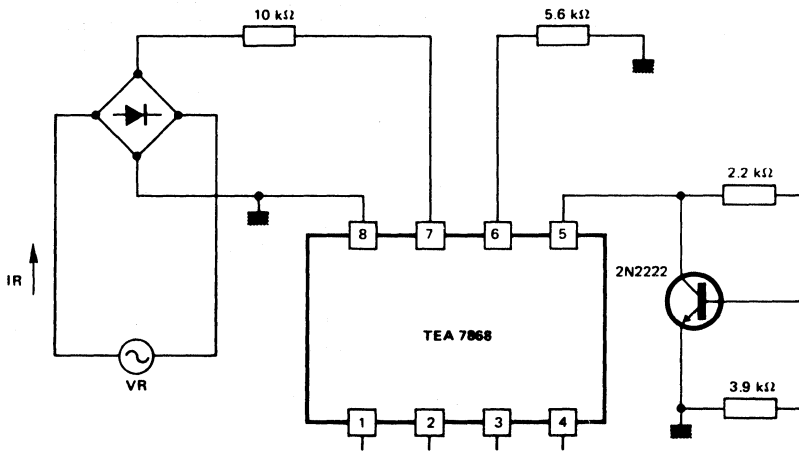
$I_L = 20\ mA$

$$Z_{out} = \frac{V_1}{i_L}$$

Return loss is defined by:

$$R.L. = 20 \log \left(\frac{|Z_{out} + 600|}{|Z_{out} - 600|} \right)$$

Note 3: Ring detection part:



Test conditions:

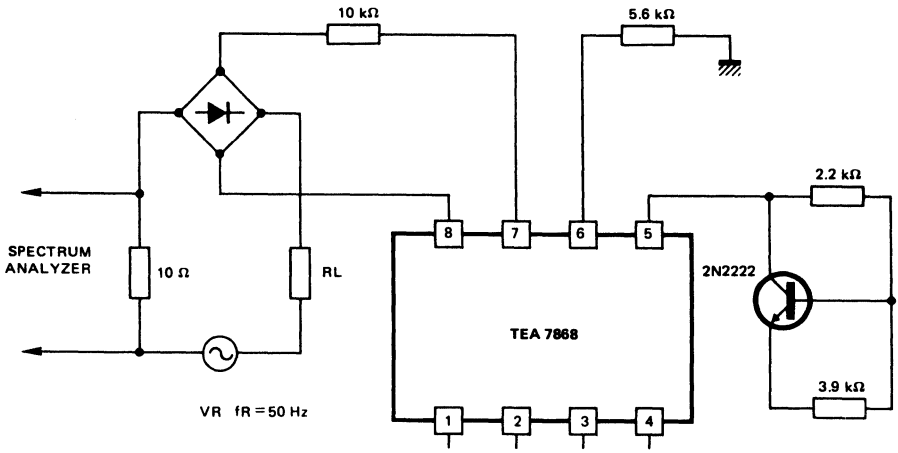
- Ring detection level

for: $V_R = 18$ Vpp $V(5) < 0.3$ V
for: $V_R = 22$ Vpp $V(5) > 0.8$ V

- Impedance of the ring detection part:

$$Z_R = \frac{V_R}{I_R}$$

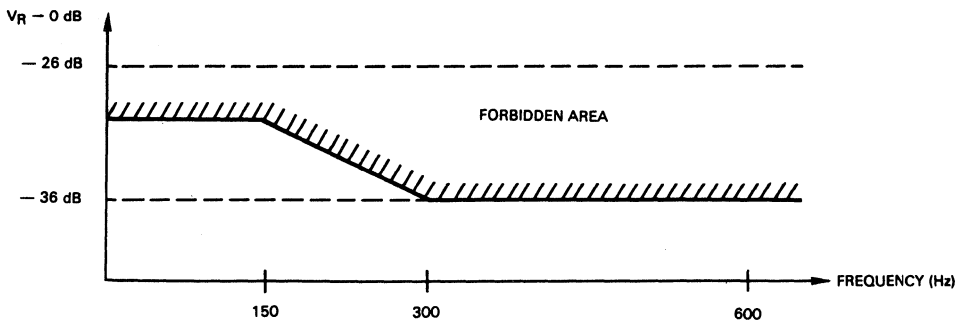
Note 4: Ring detection distortion:



Test conditions:

$V_R = 90\ V_{RMS}$ $\quad 300\ \Omega < R_L < 1400\ \Omega$

No distortion peaks appear in the forbidden area of the following shape:



APPLICATIONS INFORMATION

RING DETECTION:

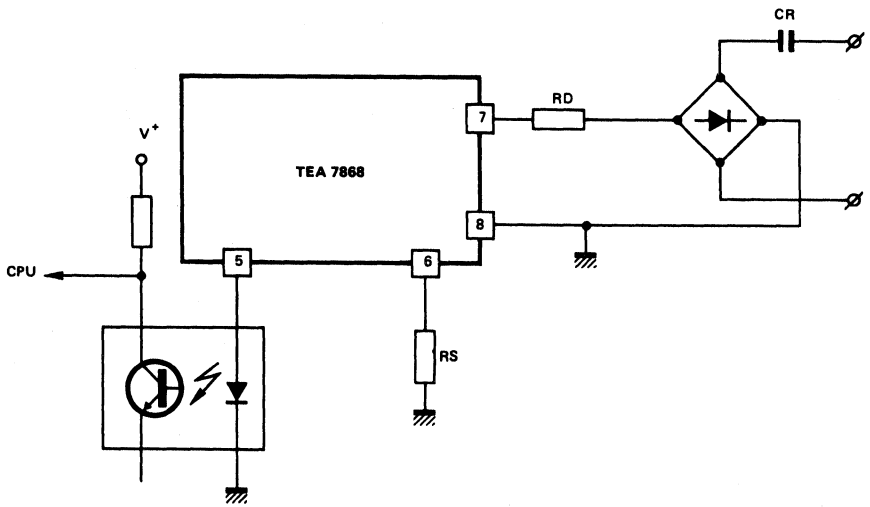


FIGURE 1

The ringing signal coming from the line is rectified by the diode bridge; the circuit compares the peak amplitude of the signal to a predeterminated detection level fixed by R_S. On the output transistor of the optocoupling device a logic signal is generated which frequency is twice the frequency of the ringing signal.

"0" = the amplitude of the ringing signal is greater than the detection level.

"1" = the amplitude of the ringing signal is lower than the detection level.

The ring detection circuit is fully linear; so the distortion on the line is very low compared to the distorsion introduced by a zener detector as usually used.

Three external components affect the characteristic of the ring detection circuit. The capacitor C_R provides the DC solation from the line.
The AC impedance of the circuit at the ringing frequency is given by the formula:

$$Z_{AC} = Z_{CR(f)} + R_D + R_S/13$$

Z_{CR} is the impedance of the capacitor C_R at the ringing frequency.

The ring detection level is fixed by the external resistor R_S with the following formula:

$$R_S = \frac{11 \text{ volts}}{V_R\text{-}V_D\text{-}3 \text{ volts}} R_D$$

V_R is the peak amplitude of the ringing signal at the detection level.
V_D is the voltage over the diode bridge and the capacitor C_R at the ringing frequency.

AC/DC LINE ADAPTATION:

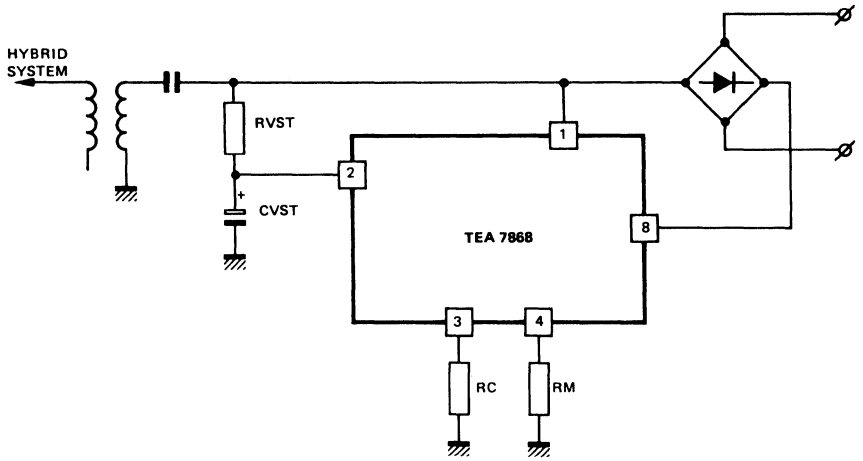


FIGURE 2

This part of the TEA7868 is used for line adaptation. An equivalent diagram of the circuit is given at fig. 3.

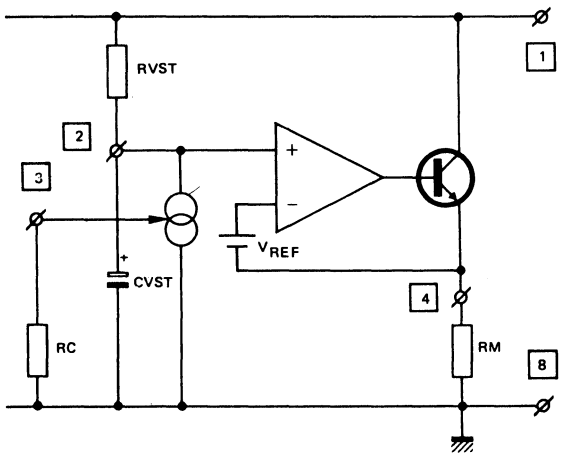


FIGURE 3

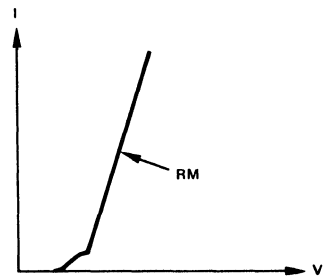


FIGURE 4

The DC characteristic is a zener characteristic which slope is fixed by R_M (see fig. 4). The voltage over the circuit (pin 1) is fixed via a current source driven through R_{VST}. The value of this current source is fixed by the external resistor R_C with the formula:

$$V(R_{VST}) = V(pin1) - V(pin2) = \frac{R_{VST}}{R_C} \times 2.45 \text{ volts}$$

Note that the voltage through R_{VST} also limits the amplitude of the emitted signal.

The external resistor R_{VST} also defines the AC impedance of the circuit:

Z_{AC} = R_{VST} // impedance seen from the transformer (see hybrid system)

* When a current limitation is required for the DC characteristic (as for the French specification), an external TPE is connected between the telephone line and the circuit (see application diagram).

PULSE DIALLING:

Pulse dialling is easily done using a high voltage optocoupling device and a high voltage PNP transistor as shown on the typical application diagram.

HYBRID SYSTEM:

This system uses an operational amplifier to prevent from injecting the emitted signal in the receiving path of the modem IC. A typical diagram is given at fig. 5.

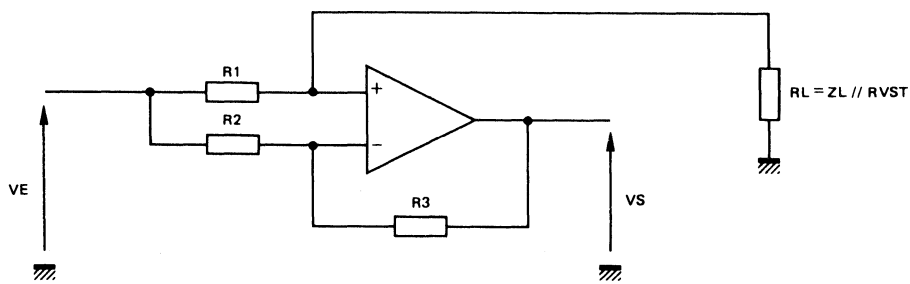


FIGURE 5

R_L represents the impedance of the telephone line Z_L in parallel with R_{VST}. Typically we take Z_L = 600 ohms.
The hybrid gain of the system is given by:

$$G_D = \frac{V_S}{V_E} = 1 - \frac{R_2+R_3}{R_2}\frac{R_1}{R_1+R_L}$$

For a maximum efficiency you must have $G_D = 0$ and this gives:

$$\frac{R_3}{R_2} = \frac{R_L}{R_1}$$

The impedance seen from the line must be 600 ohms, this impedance is given by:

$Z_{out} = R_1 // R_{VST}$

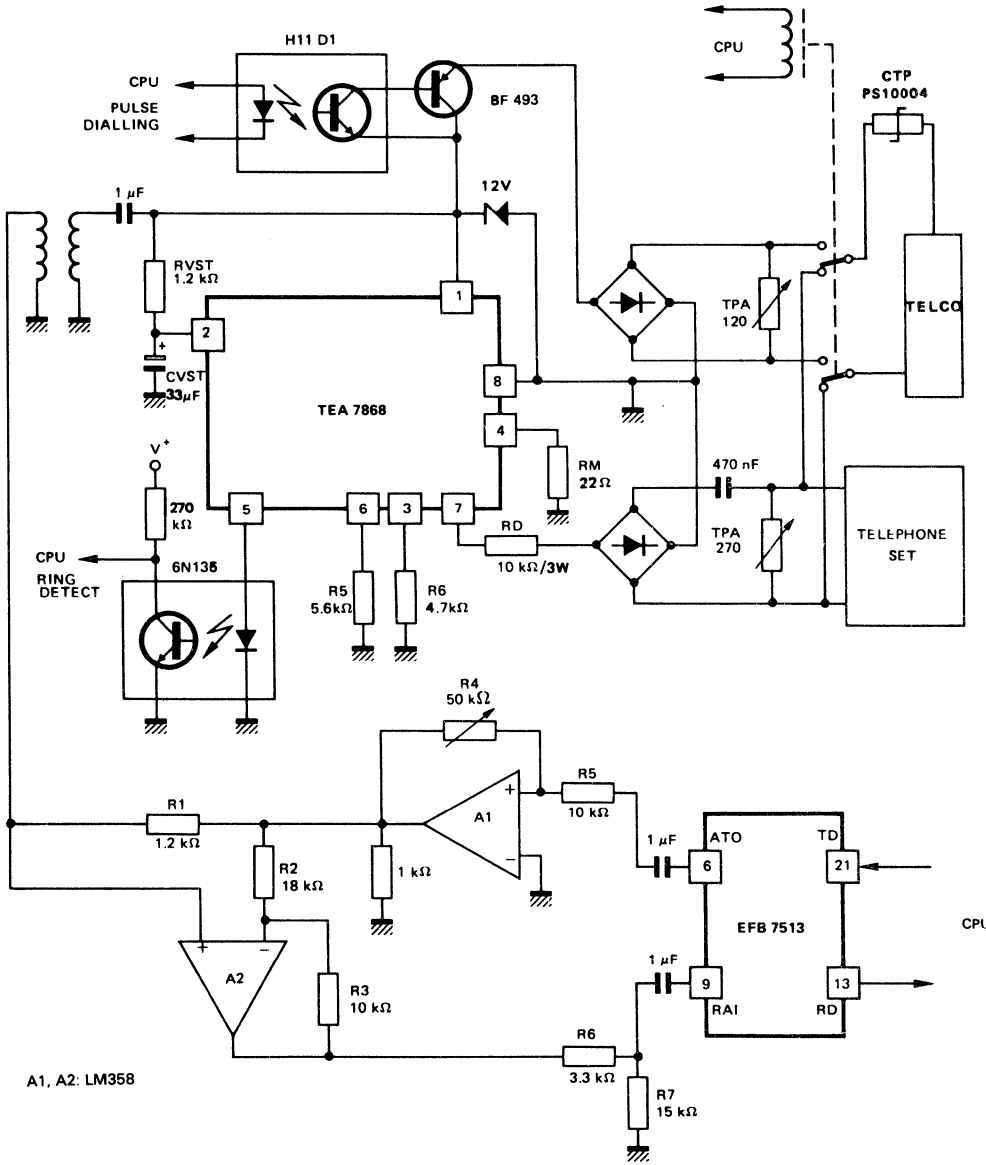
So, if R_{VST} is fixed, R_1 is also fixed by Z_{out} = 600 ohms.
The gain between the online signal and the modem input is:

$$G_E = \frac{R_L}{R_1+R_L}$$

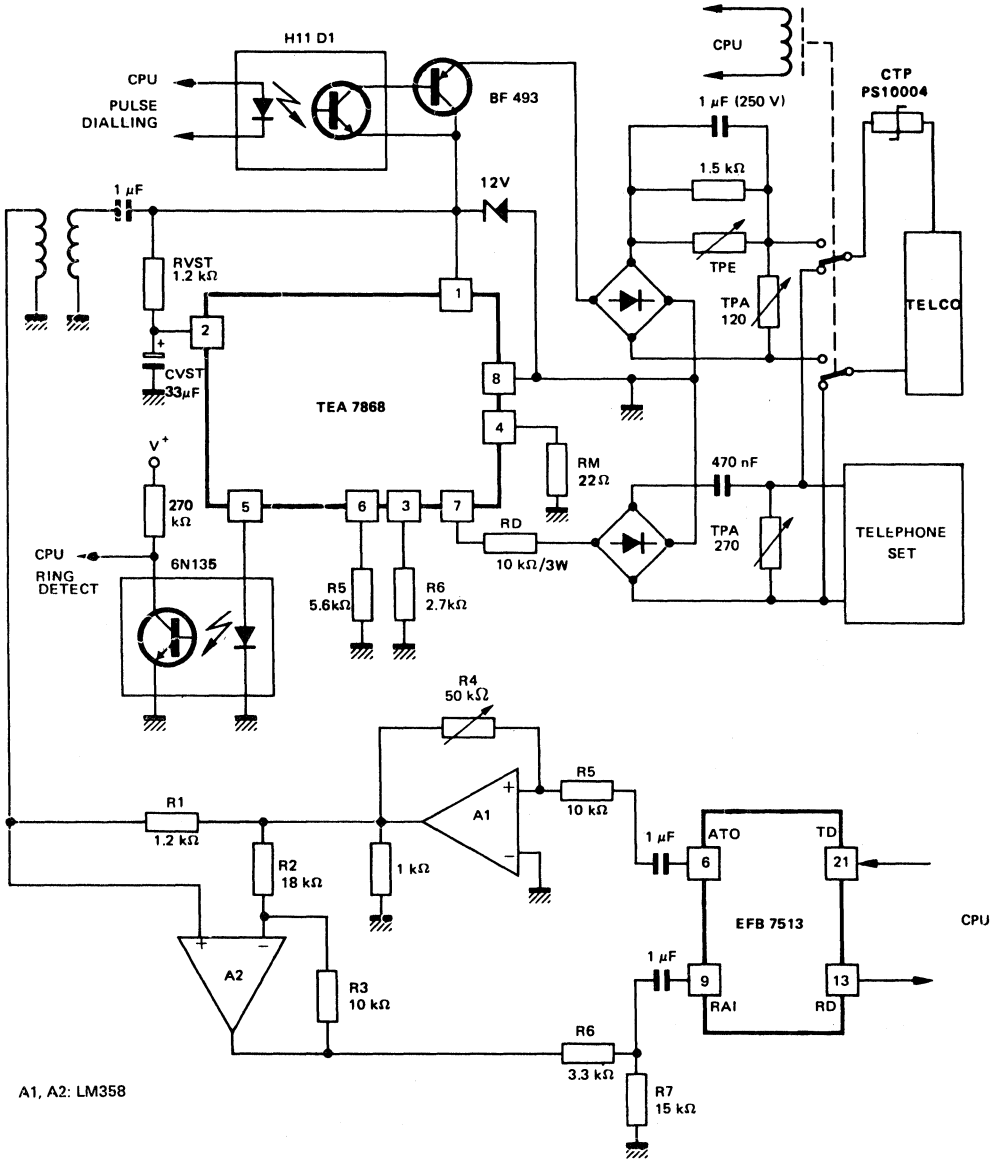
The gain between the line and the modem input is:

$$G_R = 1 + \frac{R_3}{R_2}$$

Those calculations are purely theoretical; really the line impedance has a complex component, so there will be little changes in the value of R_1, R_2, R_3 to adapt the hybrid system.



COMPLETE DAA INTERFACE CIRCUIT WITH TEA7868

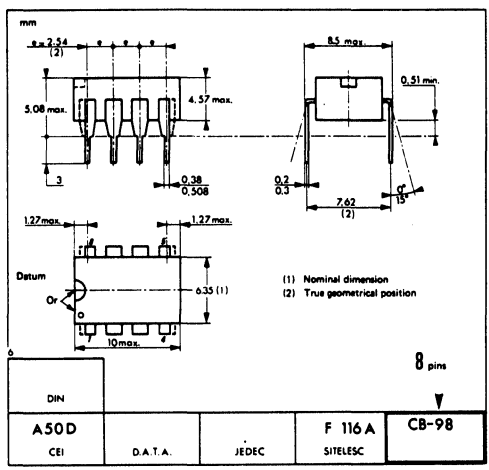


COMPLETE DAA INTERFACE CIRCUIT WITH TEA7868

PHYSICAL DIMENSIONS

CB-98

PLASTIC PACKAGE



MODEM APPLICATION COVERAGE

Standard	Digital signal Processor DSP	Analog front end AFE	Additional circuits
V22 bis	1 × TS 75240	1 x TS 7542	–
BELL 201 (V26) HD 2400 bps	1 x TS 68930	1 × TS 68950 Transmit 1 × TS 68951 Receive 1 × TS 68952 Logic	–
BELL 208 (V27) HD 4800 bps	1 x TS 68930	1 x TS 68951 Transmit 1 x TS 68951 Receive 1 x TS 68952 Logic	–
BELL 209 (V29) HD 9600 bps	1 x TS 68930	1 x TS 68950 Transmit 1 x TS 68951 Receive 1 x TS 68952 Logic	Fast RAM 256 x 16
V33 HD (14.4 bps)	1 x TS 68930	1 x TS 68950 Transmit 1 x TS 68951 Receive 1 x TS 68952 Logic	Fast RAM 2 k x 16
V26 ter FD/EC 2400 bps	1 x TS 68930	1 x TS 68950 Transmit 1 x TS 68951 Receive 1 x TS 68952 Logic	Fast RAM 1 k x 16
V32 FD/EC 4800 bps	1 x TS 68930	1 x TS 68950 Transmit 1 x TS 68951 Receive 1 x TS 68952 Logic	Fast RAM 2 k x 16
V32 FD/EC 9600 bps	3 × TS 68930	1 x TS 68950 Transmit 1 x TS 68951 Receive 1 x TS 68952 Logic	Fast RAM 2 k x 16

THOMSON COMPONENTS
MOSTEK

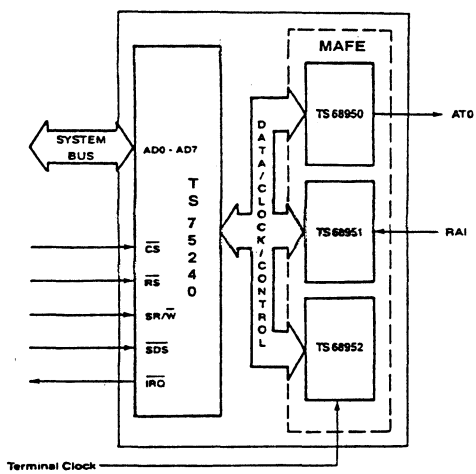
TS 7524

V.22 BIS, V.22, BELL 212 / V.23, V.21, BELL 103 CHIP SET

ADVANCE INFORMATION

COMMUNICATIONS PRODUCTS

- DSP (TS75240) and Modem Analog Front-End (MAFE™) implementation.
- QAM, DPSK and FSK Modulation and Demodulation.
- Auto-adaptative Equalization.
- Transmit and Receive Filtering.
- Sharp adjacent channel rejection.
- Versatile high performance Analog Front-end (MAFE™).
- Data transmission speed :
  - 2400 bps in QAM
  - 1200,600 bps in DPSK
  - 1200,300,75 bps in FSK
- Programmable transmit level.
- On-chip 4/2-wire hybrid function.
- Answer tone detection and generation for CCITT (2100 Hz) and Bell (2225HZ) Standards.
- 550 Hz and 1800 Hz guard tone generation.
- DTMF Tone Generation.
- Call progress tone detection.
- Scrambler and Descrambler selection.
- 64-space detection feature.
- Supply voltages : ± 5 V.



TS7524 BLOCK DIAGRAM

™ MAFE refers to TS 68950, TS 68951 and TS 68952 devices (see appropriate data sheets).
These specifications are subject to change without notice.

CHAPTER 3 - DIGITAL SIGNAL PROCESSORS & PERIPHERALS

THOMSON COMPONENTS
MOSTEK

TS68930 • TS68931

PROGRAMMABLE SIGNAL PROCESSOR

ADVANCE INFORMATION

The TS68930/1 (Programmable Signal Processor) is a high-speed general purpose signal and arithmetic processor with on-chip memory, multiplier, ALU, accumulators and I/Os. It is organized in a parallel/pipeline structure to execute simultaneously one ALU, function, multiplication, two reads and one write operation and associated address calculation every 160 ns.

- Parallel/pipeline Harvard architecture
- 3 data-bus structure
- 3 data types : 16-bit real, 32-bit real
  : 16 + 16-bit complex number
- 2 versions : TS68930 (internal ROMs) 48-pin
  : TS68931 (external ROMs) 84-pin
- Pipeline complex multiplier
- 2 x 128 x 16-bit RAM
- 512 x 16-bit coefficient ROM
- 32-bit instruction bus
- 64 k x 32-bit external program space
- 68000 family compatibility
- Dual external buses : local/system

HMOS2

PROGRAMMABLE SIGNAL PROCESSOR

CASE CB-229

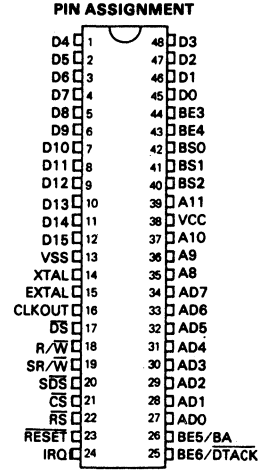
TS68930
P SUFFIX
PLASTIC PACKAGE

TS68931
E SUFFIX
LCCC 84

TYPICAL APPLICATIONS

- Adaptive processing
- Complex numbers
- Digital filtering
- Fast Fourier transform
- Voice grade communication systems
- High-speed modems
- Speech processing
- Audio Frequencies
- Sonar/radar
- Image processing
- Robotics
- Graphics processing

PIN ASSIGNMENT



TS68930

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(continued)

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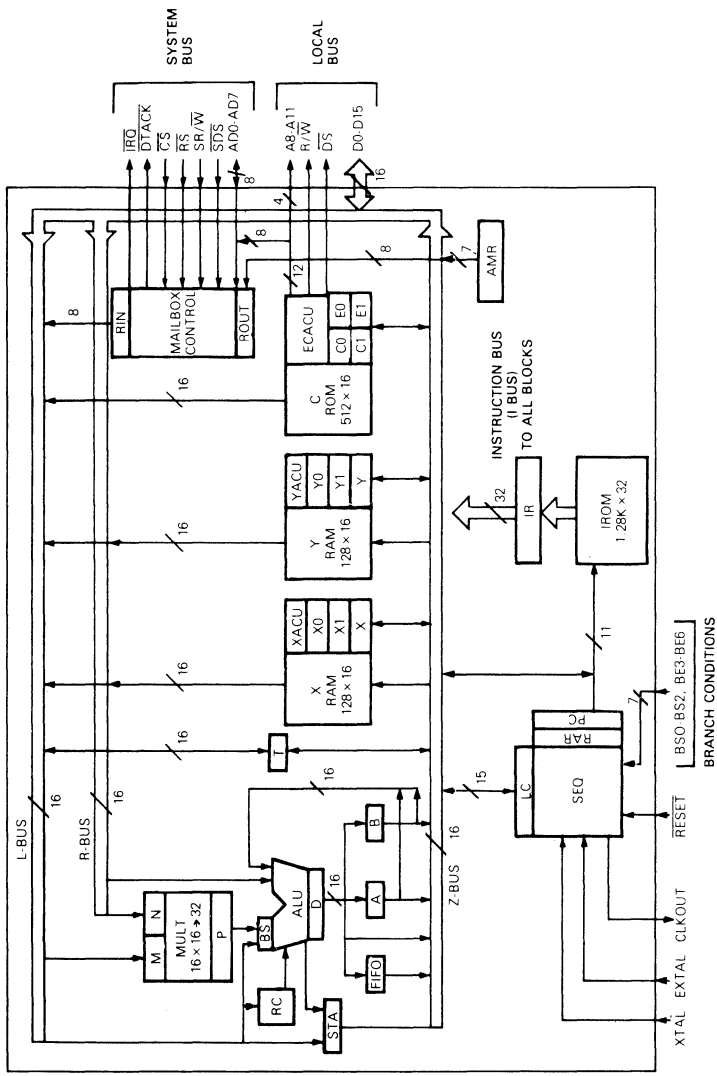


SECTION 2
PIN DESCRIPTION

LOCAL INTERFACE

Name	Pin Type	Pin nb. TS68930	Pin nb. TS68931	Function	Description
D (0:15)	I/O	45-48 1-11	6-21	Data bus	Can be concatenated or separate D (0:7), D (8:15)
A (8:11)	O	35,37,39	45-48	Address bus	High order addresses for local interface
$\overline{DS}$	O	17	27	Data Strobe	Synchronizes the transfer
R/$\overline{W}$	O	18	28	Read/write	Indicates the current bus cycle state
CLKOUT	O	16	26	Clock output	The frequency of CLKOUT is one half the frequency of the input clock or crystal

SYSTEM INTERFACE

Name	Pin Type	Pin nb. TS68930	Pin nb. TS68931	Function	Description
AD (0:7)	I/O	27-34	35-42	System data bus or local address bus	The data exchanges between the processor and a master via a mailbox is the function of this bus. It is also used to generate the addresses of an external RAM.
$\overline{CS}$	I	21	31	Chip Select	Used by a master to gain access to the mailbox and system bus
$\overline{RS}$	I	22	32	Register Select	Used by a master to gain access to the mailbox and system bus
$\overline{SDS}$	I	20	30	System Data Strobe	Synchronizes the transfer on the system bus
SR/$\overline{W}$	I	19	29	System Read/Write	Indicates the current system bus cycle state
$\overline{DTACK}$	O	25	43	Data Transfer Acknowledge	Indicates that the processor has recognized it is being accessed
BA	O	26	44	Bus Available	Indicates availability of system bus to master
$\overline{IRQ}$	O	24	34	Interrupt Request	Handshake signal sent to the master to gain access to the mailbox

EXTERNAL BRANCH CONDITIONS

Name	Pin Type	Pin nb. TS68930	Pin nb. TS68931	Function	Description
BS (0:2)	I	42-40	49-51	Branch on State	External conditions. Can be programmed on a high or low state
BE (3:6)	I	44 43 26 25	53 52 44 43	Branch on Edge	External conditions. Falling edge is memorised and reset when tested. BE5 shares pin with $\overline{BA}$ BE6 shares pin with $\overline{DTACK}$

OTHER PINS

Name	Pin Type	Pin nb. TS68930	Pin nb. TS68931	Function	Description
EXTAL	I	15	25	Clock	Crystal input pin for internal oscillator or input pin for external oscillator
XTAL	I	14	24	Clock	Together with EXTAL it is used for the external 25 MHz crystal
VDD	I	38	23-65	Power supply	
VSS	I	13	22-64	Ground	
$\overline{RESET}$	I	23	33	Reset	

INSTRUCTION INTERFACE (TS68931 only)

Name	Pin Type	Pin nb.	Function	Description
I (0:31)	I/O	1-5 56-63 56-84	Instruction Address/data bus Coefficient ROM address bus	Instruction bus - 32-bit data Instruction address - (I16 - I31) External coefficient ROM address - (I6 - I15) 10-bit (9-bit address + output enable signal)
$\overline{HALT}$	I	54	Halt Signal	Halts the processor. This signal freezes the program counter and loop counter
INCYCLE	O	55	Instruction cycle clock	160 ns in REAL mode 320 ns in CPLX/DBPR Mode

SECTION 3
SUMMARY OF BASIC HARDWARE

OPERATING MODES

Resource	Paragraph N°	Symbol	Function
Mode register	5.1	MODE	2-bit register defining the operating mode (real/complex/double precision).

CONTROL BLOCK

Resource	Paragraph N°	Symbol	Function
Instruction ROM	5-2-1	IROM	1280 x 32-bit word read-only-memory containing program code and immediate data.
Instruction register		IR	32-bit register containing instruction.
Program Counter	5-2-2	PC	16-bit register containing address of program memory.
Sequencer	5-2-3	SEQ	The sequencer can test directly 16 conditions programmed on a high or low state.
Return Address Register	5-2-4	RAR	16-bit register for saving program counter in case of subroutine call.
Loop Counter	5-2-5	LC	15-bit register containing a control word for automatic loop. It is divided as follows
		LCI	4-bit register containing the number of instructions to be executed in the loop.
		LCR	8-bit register containing the number of loops.
		LCD	3-bit register containing the number of instructions between declaration and start of the loop.

PROCESSING BLOCK

Resource	Paragraph N°	Symbol	Function
Pipeline Multiplier	5-3-1	MULT	16 x 16 → 32 parallel pipeline multiplier + 16-bit adder/substractor to execute complex multiplications.
		M, N	2 x 16-bit registers containing multiplier operands.
		P	2 x 16-bit register containing multiplier result.
Barrel Shifter	5-3-2	BS	Variable 0 - 15-bit right shift, left shift, right rotation barrel shifter.
Arithmetic Logic Unit	5-3-3	ALU	2 port 16-bit arithmetic logic unit. 5 possible sources, 4 possible destinations, 27-functions. Works on 32-bit in 2 cycles.
		D	ALU output register.
Saturation	5-3-4	SAT	Flag. Indicates saturation mode
Status	5-3-5	STA	15-bit register containing status of ALU, mode, status of address calculation units.
Accumulators	5-3-6	A	2 x 16-bit accumulator.
		B	2 x 16-bit accumulator.
Fifo	5-3-7	F	4 x 16-bit first in first out register.
Empty Fifo		EF	Flag.Indicates that the fifo is empty ; can be set by software.
Replace Code register	5-3-8	RC	6-bit register allowing replacement of ALU operation code by a data coming from L-BUS.
Transfer register	5-3-9	T	2 x 16-bit register providing direct transfer between L-BUS and Z-BUS.

MEMORY BLOCK

Resource	Paragraph N°	Symbol	Function
Data RAMs	5-4-1	XRAM YRAM	2 × 128 × 16-bit word random access memories containing data.
Data ROM		CROM	512 × 16-bit word read only memory containing coefficients or constants.
Address Calculation Units	5-4-3	XACU YACU	2 × 7-bit arithmetic units providing incrementation, decrementation, automatic loop of address. XACU is dedicated to XRAM. YACU is dedicated to YRAM.
		ECACU	12-bit arithmetic unit providing incrementation, decrementation of address. Shared between CROM and ERAM (external RAM).
Pointers	5-4-4	X0, X1 X	2 × 7-bit registers used for indirect addressing of XRAM. Supplementary register used for circular addressing.
		Y0, Y1 Y	2 × 7-bit registers used for indirect addressing for YRAM. Supplementary register used for circular addressing.
		C0, C1	2 × 9-bit registers used for indirect addressing of CROM.
		E0, E1	2 × 12-bit registers used for indirect addressing of ERAM.
XRAM Circular Flag	5-4-5	XC	Flag. Indicates the circular addressing mode for XRAM.
YRAM Circular Flag		YC	Flag. Indicates the circular addressing mode for YRAM.

INPUT/OUTPUT BLOCK

Resource	Paragraph N°	Symbol	Function
Access Mode Register	5-5	AMR	7-bit register defining the access mode on the 2 external buses (local and system).
Input Register	6-4	RIN	3 × 8-bit shift register. Mailbox input.
Output Register		ROUT	3 × 8-bit shift register. Mailbox output.
Ready Out Internal	6-5	RDYOIN	Flag used in the protocol to indicate which processor has access to the mailbox.

SECTION 4
ARCHITECTURE

4.1. INTERNAL ARCHITECTURE

4.1.1. Parallel processing

The processor internal architecture is organized around the following blocks :
- the arithmetic logic unit and its associated working registers
- the multiplier
- the 3 memories and their associated address calculation units
- the transfer register
- the I/O unit.

All these blocks can work simultaneously and independently.

4.1.2. Three-bus structure

To avoid memory access bottlenecks the processor architecture includes 3 data buses. Two read buses (L-BUS and R-BUS) continuously feed the operating units. Thus making it possible to load the ALU and the multiplier with the two operands simultaneously. The write bus (Z-BUS) is used to transfer the results back into the RAMs (internal or external).

4.1.3. Wide instruction word

The 32-bit wide instruction format allows the processor to execute the following operations in 1 instruction cycle:
- Read two operands (from internal or external memories)
- Execute an ALU operation
- Start a multiplication
- Use the result of the multiplication started 2 cycles before
- Write a result in internal/external memory
- Post-modify 3 pointers independently
- Store data into the transfer register.

4.1.4. Pipeline (cf. fig. 4.1.)

The figure 4.1. outlines the overlap of the instruction prefetch and execution as well as the pipelined data operation.

By using a pipeline structure, the processor performs efficiently on all digital signal processing algorithms. For example the result of a multiplication started at instruction IN will be available at IN + 2. That will not prevent from starting a new multiplication at IN + 1 which in turn will be available at IN + 3, etc... in effect, giving a multiplier throughput of 1 multiplication every cycle.

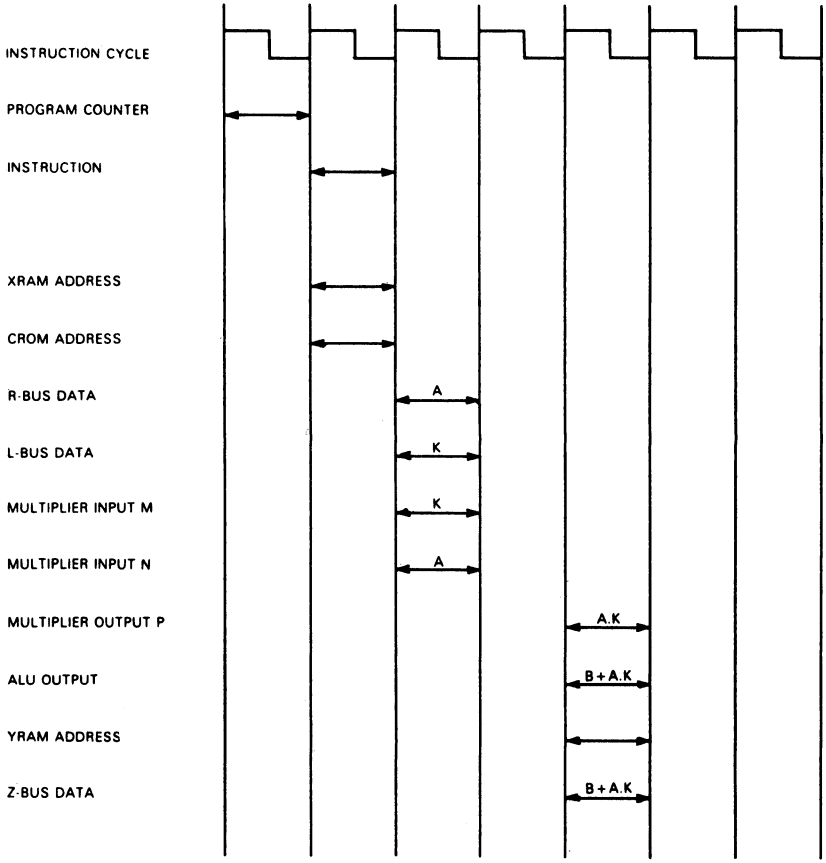


FIGURE 4.1.A. - PIPELINE DELAY

Example: READ A(XRAM), READ K(CROM), MULTIPLY A and K, ADD B(ACCUMULATOR), WRITE RESULT A.K + B INTO YRAM.

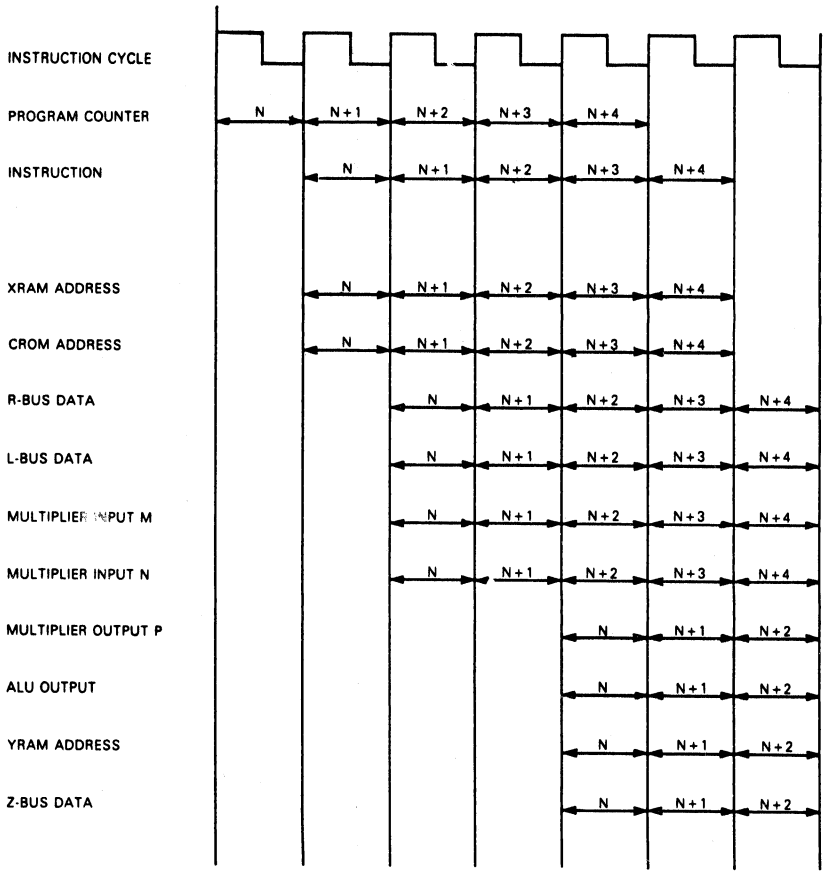
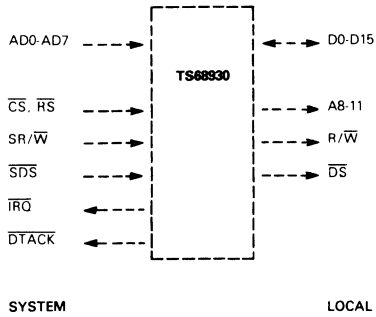


FIGURE 4.1.B. - PIPELINE THROUGHPUT

Example: The operation A.K + B (described in fig. 4.1.A.) is executed every cycle.

4.2. EXTERNAL ARCHITECTURE

The TS68930 is provided with two external buses:
— the system bus: AD0-AD7
— the local bus: D0-D15.
The processor is a slave on the system bus.
The processor is a master on the local bus.



SYSTEM BUS

The main use of the system bus is for the processor to exchange information with a general purpose microprocessor or another TS68930 in a multiprocessor environment.

The informations are exchanged through a mailbox with a flag ($\overline{IRQ}$) indicating to the master (the other processor) that it can gain access to the mailbox.

LOCAL BUS

The main use of the local bus is for the processor to exchange information with an external memory, a peripheral, a data converter or another TS68930 in a multiprocessor environment. All these external circuits are defined as slaves.

The processor is the master of its local bus, i.e it generates the address and control signals which direct the exchange on the local bus. This bus is a direct extension of the internal structure and all external circuits connected on it, work in exactly the same way as the internal operating units.

SECTION 5
FUNCTIONAL DESCRIPTION

5.1. OPERATING MODES

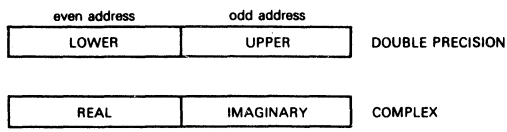
The processor provides three operating modes set by programming, each mode representing a different data type :
- REAL = 16-bit data
- COMPLEX (CPLX) = 2 x 16-bit data
- DOUBLE PRECISION (DBPR) = 32-bit data.

The modes are made transparent to the programmer as all operating units and all working registers are provided with the right length.

Main differences between real mode and complex or double precision mode:

a) In complex and double precision mode the memory space is reduced by half as all operands are 32-bit long (cf. format below).

b) The instruction cycle time is doubled (320 ns instead of 160 ns) as all operations are made sequentially.



5.2. CONTROL BLOCK

5.2.1. Instruction ROM: IROM

The instruction ROM has a capacity of 1280 x 32-bit in the MCU version. It can be extended to 64 K x 32-bit in the MPU version.

5.2.2. Program counter: PC

The program counter is 16-bit wide, 11 bits are used in the MCU version.

5.2.3. Sequencer: SEQ

The sequencer increments the program counter except in case of sequence jump which are listed below:
a) immediate branch
b) computed branch
c) jump to subroutine } (cf 5.2.4.)
d) return from subroutine }
e) automatic loop } (cf 5.2.5.)

In case of immediate branch the PC is loaded with an immediate value whereas in case of computed branch the PC is loaded with a value coming from the accumulators (A, B), the FIFO (F) or the transfer register (T).

The sequencer can test directly 16 conditions programmed on a high or low state:

BRANCH NEVER/ALWAYS

STATUS CONDITIONS

- SR Sign (Real)
- SI Sign (Imaginary)
- CR Carry (Real)
- CI Carry (Imaginary)
- Z Zero
- OVF Overflow
- MOVF Memorized overflow

The memorized overflow (MOVF) is reset when tested by the branch instruction.

EXTERNAL CONDITIONS

- BS0-BS2 } External pins
- BE3-BE6 }

The falling edges of BE3-BE6 are memorized internally and reset when tested by the branch instruction.

The external test conditions are used to synchronise different processes or as a ready input flag in multiprocessor system.

MAILBOX FLAG

- RDYOIN Internal mailbox flag

5.2.4. Return address register : RAR

The JSR instruction allows one level of subroutine nesting with automatic saving of the PC on to the return address register (RAR).

Multiple level of subroutine nesting can be implemented in RAM using either of the two pointers as stack pointer.

In this case the RAR is used as the last level of nesting.

5.2.5. Loop counter: LC

a) The efficiency of executing repeated calculations often encountered in Digital Signal Processing is considerably improved by using the loop counter since the instructions for counter increment and range check are no longer needed.

This counter can implement a loop of up to 16 instructions repeated 256 times with a delay of up to 8 instructions.

b) **DESCRIPTION:**

LCI : Instruction Loop Counter : 4-bit
Counts the number of instructions to be executed in the loop

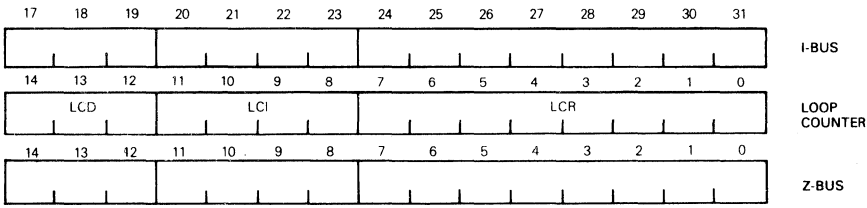
LCR : Repeat Loop Counter: 8-bit.
Gives the number of times the loop will be repeated.

LCD : Delay Loop Counter: 3-bit.
Gives the delay between the declaration and the start of the loop.

c) **USE:**

A loop is declared by loading the instruction loop counter and the delay loop counter with a constant (INI Instruction) and LCR with a constant or a variable (INI or OPDI instruction).

The loop counter contents can be saved (SVR instruction) with the following format:



Asserting $\overline{\text{HALT}}$ will freeze the state of the LC.

Asserting $\overline{\text{RESET}}$ will reset the LC.

5.3. PROCESSING BLOCK

5.3.1. Multiplier

a) The multiplier executes a 16 x 16 → 32-bit signed multiplication every instruction cycle with a delay of 2 cycles independently of the operating mode.

The number representation is signed 2's complement and the result format for the 3 modes is shown in figure 5.3.1.

b) **USE:**

The multiplier is always active. To start a multiplication the two operands are loaded into the two input registers(M, N).

The multiplication will be repeated every cycle until one or both operands are changed. The processor offers the possibility of loading the two input registers independently.

The result is available in the product register (P) two cycles later.

c) **COMPLEX MULTIPLICATION:**

The processor executes a complex multiplication:
$(A+jB) \cdot (C+jD) = AC - BD + j(AD+BC)$
every 320 ns thanks to an internal 80 ns clock.

As it can be seen from the equation the complex multiplication can generate an overflow. In this case the multiplier overflow (OVFM) is memorised inside the status register.

d) **NOTES:**

No provision is made for the operation 8000 x 8000 (hexadecimal).
If this condition arises the product will be 8000 (hexadecimal).

After changing modes the product P is calculated following the new mode.

The signal HALT (cf. Input/output) will inhibit the loading of the product register P.

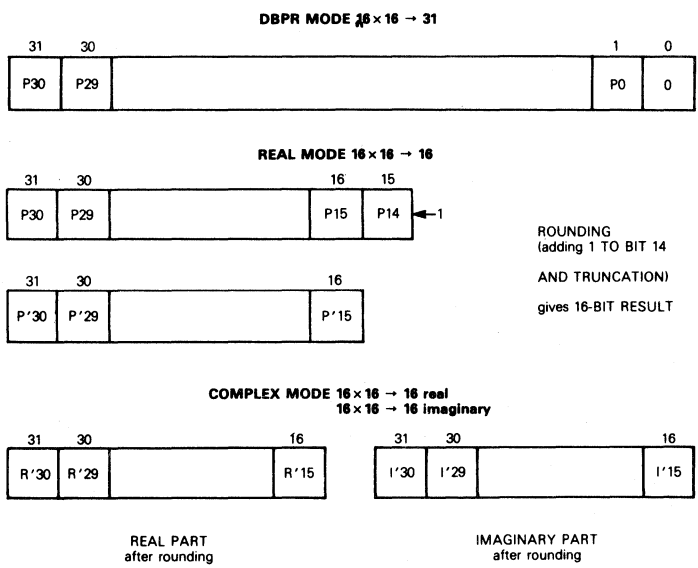


FIGURE 5.3.1. - MULTIPLICATION OUTPUT REGISTER (P) FORMATS

5.3.2. Barrel Shifter (BS)

All shift and rotation operations are performed at the L-side (left) ALU input. The operand can come from two sources:
- LBUS
- P (product register)

There are two types of shift and rotate operations:

1) The operations which are part of the ALU code:
- arithmetic shift right by 1 (ASR)
- logical shift right by 1 (LSR)
- arithmetic shift left by 1 (ASL)
- logical shift left by 1 (LSL)
- logical shift right by 8 (LSRB)
- logical shift left by 8 (LSLB)
- rotate right by 1 (ROR)

2) The operations which are implemented through dedicated instructions:
- ASR (0 → 15) arithmetic shift right by N $0 \leqslant N \leqslant 15$
- LSR (0 → 15) logical shift right by N
- LSL (0 → 15) logical shift left by N
- ROR (0 → 15) rotation right by N

Note:
In double precision the shift operations are not executed on 32 bits, but on 2 x 16-bit as the barrel shifter is a 16-bit unit. In complex mode the shift operations are executed on the real and imaginary parts.

5.3.3 ALU

The ALU inputs are called L-Side (Left) and R-Side (Right).

There are two possible sources on the L-Side:
- L BUS
- P (multiplier output).

There are two possible sources on the R-Side:
- R BUS
- Accumulators A or B.

The selection between A or B is made by the field ALU destination (refer to operating codes). If the ALU destination field is B then the ALU source is B. In all other cases A will be used.

The ALU output is called D.

There are four possible destinations for D:
- Accumulator A
- Accumulator B
- FIFO
- Z-BUS (no working registers are modified).

ALU CODES
There are 27 ALU codes. The list is shown in figure 7.9.

5.3.4. Saturation mode (SAT)

If the saturation mode is set (SAT flag) the circuit will behave as follows :
- Positive overflow = ALU result is forced to 7FFF (hexadecimal)
- Negative overflow= ALU result is forced to 8000 (hexadecimal)

The saturation mode does not apply to the double precision mode.

5.3.5. Status register: STA

a) DESCRIPTION

15	14	13	12	11	10	9	8	7	6	5	4 3	2	1	0
SR	SI	CR	CI	Z	OVF	MOVF	AOVF	OVFM	EF	SAT	MODE	XC	YC	–

CONDITION CODE REGISTER (CCR):

SR	Sign (real)	Set if the msb of the ALU result is 1. Cleared otherwise.
SI	Sign (imaginary)	Set if the msb of ALU imaginary result is 1. Cleared otherwise.
CR	Carry (real)	Set if a carry is generated out of the msb of the operand for arithmetic and shift operations. Cleared otherwise.
CI	Carry (imaginary)	Set if a carry is generated out of the msb of the imaginary part for arithmetic and shift operations. Cleared otherwise.
Z	Zero	Set if the result equals zero. In complex mode it is equivalent to the imaginary and real parts being both zeros.
OVF	Overflow	Set if there was an arithmetic overflow. This implies that the result is not representable in the operand size. In complex mode it is equivalent to the overflow of the imaginary or real part.
MOVF	Memorised overflow	Set as overflow. Reset when tested by a branch instruction.
AOVF	Advanced overflow	Exclusive or of bit 14 and bit 15 of the ALU. Set if there was an arithmetic overflow on half capacity (15 bits in real/complex mode, 31 bits in double precision mode). Cleared otherwise.
OVFM	Overflow (Multiplier)	Set if the multiplier adder/substractor has overflowed. Only meaningful for complex multiplication. Cleared otherwise.

STATE REGISTER

EF	Empty FIFO	Set if the FIFO is empty. Cleared otherwise.
SAT	Saturation mode flag	Set if the PSI is in saturation mode. Cleared otherwise.
MODE (2 bits)	Operating mode	Real, complex or double precision.
XC	XRAM	Circular addressing mode flag.
YC	YRAM	Circular addressing mode flag.

b) USE

The status can be saved (instruction SVR).

The condition code register can be read (in OPIN instruction) and it can be loaded from a RAM via L-BUS (ALU code LCCR) without passing through the ALU.

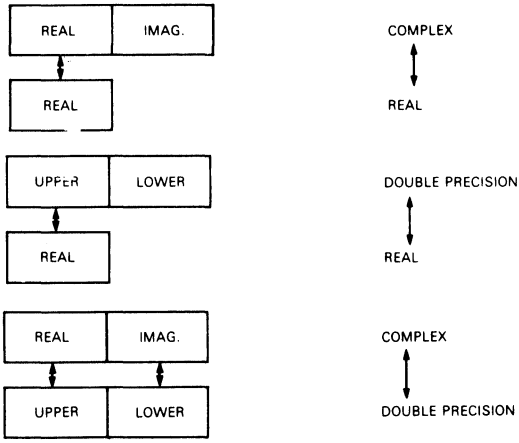
The state register can be programmed by an INI instruction.

5.3.6. Accumulators: A,B

a) The processor provides two distinct accumulators (A and B). In real mode they are 16-bit long. In complex and double precision mode they are 32-bit long.

b) Changing modes, changes the length of the accumulator and the relation between the words described below.

CHANGING MODES



It must be noted that the imaginary (respectively lower) part of the word remains unmodified when switching to real mode.

5.3.7. FIFO: F

a) **FUNCTION**

Highly pipelined algorithms require a series of pipeline registers between the ALU output and the memories in order to store intermediate results.

This is precisely the function of the 4 x 16-bit first-in first-out (FIFO) register.

b) **DESCRIPTION**

It is a 4 x 16-bit deep register that becomes 2 x 32-bit in complex and double precision modes (cf. format below).

c) **USE**

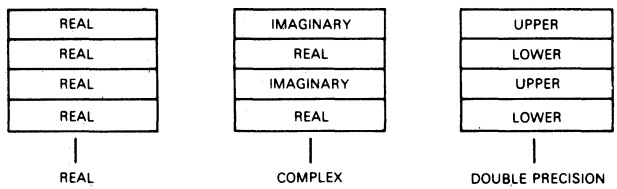
When the FIFO is full it becomes impossible to write into it.

When the FIFO is empty a status bit (EF) is set.

This bit can also be set by programmation.

d) **NOTE**

In real mode, a result loaded at instruction IN into an empty FIFO will be available for transfer to the RAM at IN + 2. In all other cases it will be at IN + 1.



5.3.8. Replace code register: RC

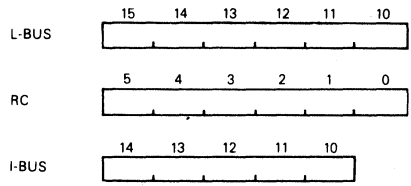
a) **FUNCTION**

The function of this register is to control the ALU by a data coming from the memories via L-BUS instead of an instruction. In other words it allows the data to take control of program sequencing without using test instructions.

For this reason it can be said that the **instructions are data controlled**.

b) **DESCRIPTION**

It is a 6-bit register with the following format :



BIT 1-5 = ALU code is substituted by this value

BIT 0 = 0 Destination of ALU output = accumulator A
= 1 Destination of ALU output = accumulator B

c) **USE**

This register is controlled by three ALU codes :

ALU code	Function
RCR	Load ALU control code in RC
RCE	Execute ALU control code contained in RC
RCER	Execute ALU control code contained in RC Load new ALU control code in RC

5.3.9. Transfer register: T

a) **FUNCTION**

It is a bidirectionnal register standing between L-BUS, and Z-BUS.

It can be a source and a destination to both buses.

Among its numerous uses, it can perform the function of :
- Loop back to the multiplier in one cycle
- Temporary register between memory and ALU
- Temporary register between memory and multiplier
- Operations between accumulators
- Memory to memory transfer.
- Saving program counter.

b) **DESCRIPTION**

It is a 16-bit register extended to 32 bits in complex and double precision mode.

c) **USE**

The relation between the 32-bit and the 16-bit word in case of mode switching is identical to the accumulators relation.

In branch instruction the register can be used to save the PC.

When the mode is complex the PC (16-bit) is saved into the real part of the register, when the mode is DBPR the PC is saved into the upper part of the register.

T can also be used as a source of the PC:

When the mode is complex the PC is loaded with the real part of the register, when the mode is DBPR the PC is loaded with the upper part of the register.

5.4. MEMORY BLOCK

5.4.1. Data memories : XRAM, YRAM, CROM

The processor architecture allows the connection of four memories:

- 2 internal RAMs
XRAM 128 × 16-bit
YRAM 128 × 16-bit

- 1 internal data ROM separated from the program ROM
CROM 512 × 16-bit
In the microprocessor version this ROM is external.

- 1 external memory
ERAM 4 K × 16-bit
This external memory is accessed in a single cycle (160 ns) in exactly the same way as the internal memories. Moreover it does not require any "glue" parts to be connected to the processor.

Notes :

1. In complex and double precision modes all data are 32-bit long. Hence the available memory space is divided by two.
2. The instruction set allows **any combinations of simultaneous use of these memories** ; the only restraints are :
   - Reading and writing in the same RAM in the same cycle.
   - Accessing CROM and ERAM simultaneously.

5.4.2. Addressing modes

The processor provides four addressing modes:
- Indirect addressing with post modification.
- Direct addressing.
- Immediate addressing.
- Circular addressing mode (also called virtual shift mode).

5.4.3. Address calculation units: ACU

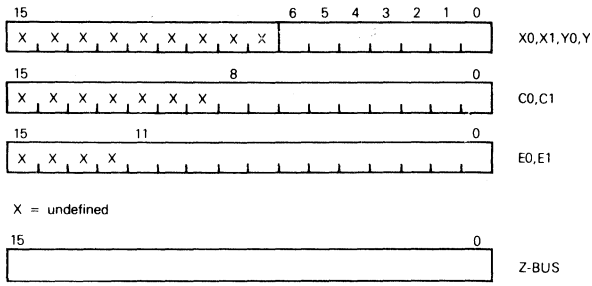
Combining these four addressing modes and the processor 3-bus structure implies the need to generate **at each instruction cycle three different addresses.** To realise these functions each memory is associated with an address calculation unit:
- XRAM with XACU
- YRAM with YACU
- CROM or ERAM with ECACU.

5.4.4. Pointers: X0, X1, Y0, Y1, C0, C1, E0, E1, X, Y

Indirect addressing is the most commonly used addressing mode in vector or signal processing. For this reason the processor offers a large number of pointers (10): X0, X1, Y0, Y1, C0, C1, E0, E1 + X and Y for circular mode.

Each memory can be addressed by two pointers and pointers can be increased (+1) decreased (−1) or held (+0) independently.

They can also be loaded with new addresses (constants or computed values) and saved in case of context switching (cf. format below).



5.4.5. Circular adressing mode

a) FUNCTION

This feature is used to simulate the function of a shift register without moving the data stored. It is particularly useful in filtering and convolution functions.

b) **DESCRIPTION**
X0 : lower limit
X1 : upper limit
X : current address
(respectively Y0, Y1, Y for YRAM)

The algorithm can be described as follows:

1. ADDRESS: ADDRESS + 1 (post-incrementation)
IF ADDRESS **GREATER THAN** UPPER LIMIT **THEN** ADDRESS = LOWER LIMIT

2. ADDRESS: ADDRESS − 1 (post-decrementation)
IF ADDRESS **SMALLER THAN** LOWER LIMIT **THEN** ADDRESS = UPPER LIMIT

c) **USE**

Programming the circular addressing mode is done independently of the operating modes (real, complex or double precision), in the following way. With reference to the instruction OPCODE: example XRAM.

1. Initialization instruction (INI)
Circular addressing bit set (K7 = 1)
Load X0 with lower limit.

2. Initialization instruction (INI)
Circular addressing bit set (K7 = 1)
Load X1 with upper limit.

3. INI or OPDI instruction
Load X with current address (a value between X0 and X1).

After the first instruction the circular addressing mode is effective.

From now on the programmer has access only to pointer X and X1. All instructions referencing pointer X0 will now physically reference pointer X.

To gain access again to pointer X0 the programmer goes back to the normal mode by an initialisation instruction.

d) **FLAGS**

When a RAM is in the circular addressing mode, a flag (XC, YC) is set inside the status.

5.4.6. ODD/EVEN addresses

a) In complex and double precision modes the processor automatically generates the two addresses of the word (even then odd).

	COMPLEX WORD	DBPR WORD
even address odd address	real part imaginary part	lower part upper part

The processor offers the possibility to inverse this order by writing a 1 into the ADOF bit (refer to OPCODE).

ADOF

0 even followed by odd
1 odd followed by even.

b) **USE**

This feature is made available independently or simultaneously for XRAM and YRAM.

With reference to OPCODE.

XRAM

Initialization instruction (INI)
- select complex or double precision mode
- select pointer X0 or X1 and load it with J constant
- select ADOF bit as wanted (0 or 1).

YRAM

Initialization instruction (INI)
- select complex or double precision mode
- select pointer Y0 or Y1 and load it with K constant
- select ADOF bit as wanted (0 or 1).

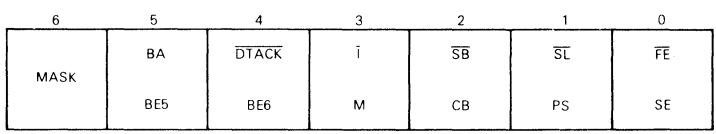
5.5. ACCESS MODE REGISTER: AMR

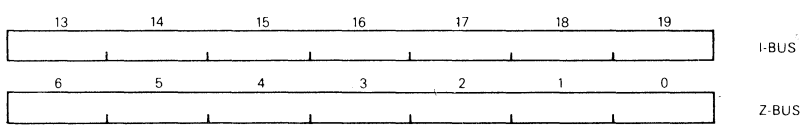
a) **DESCRIPTION**

This register defines the processor external access modes.
Its contents can be initialized with a constant and saved into memory, (cf. format below).

It is a 7-bit register each bit being defined as shown below:

$\overline{FE}$/SE :Fast exchange/slow exchange on local bus
$\overline{SL}$/PS :Slave/pseudo-Slave on system bus
$\overline{SB}$/CB :Concatenated or separate local bus
$\overline{I}$/M :Local bus control signal types
$\overline{DTACK}$/BE6 :BE6 pin redefinition
BA/BE5 :BE5 pin redefinition
MASK :Allows the AMR to be masked by the external halt (microprocessor version only).





BIT 0: $\overline{FE}$/SE

0 FAST EXCHANGE = external access in 160 ns (1 cycle)

1 SLOW EXCHANGE = external access in 320 ns (2cycles).

The slow exchange mode:
- Can only be used in the real mode.
- The circuit automatically repeats the instruction which defines the external transfer.
- The control of the multiplier, ALU, ACUs, loop counter is the responsibility of the programmer who must take into account the repetition of the instruction.

BIT 1: $\overline{SL}$/PS

0 = Slave
1 = Pseudo Slave.

A pseudo-slave processor can address an external RAM using the system bus (AD0-AD7) as address lines for its own local bus. Consequently the system bus is no more available for exchanging data between the pseudo-slave processor and the bus master.

The pseudo-slave processor behaves differently from a slave processor since in case of exchange it must relinquish this bus to the master following an exchange protocol. (Reference to I/O)

BIT 2: $\overline{SB}$/CB

0 = Separate bus
1 = Concatenated bus.

The local bus can be used as two independent 8-bit buses (D0-D7), (D8-D15) or a single 16 bit-bus (D0-D15).

BIT 3: I/M

0 = Control pulses Read ($\overline{RD}$) and Write ($\overline{WR}$) are generated
1 = Control pulses data strobe ($\overline{DS}$) and Read/Write (R/$\overline{W}$) are generated.

The local bus supports the two main types of interchange signal:
- A slave processor, a data converter such as the MAFE, a 68000 peripheral, etc. requiring a data strobe and a read/write pulse.
- The standard bytewide RAM requiring a read and a write pulse.

BIT 4: $\overline{DTACK}$/BE6

0 = $\overline{DTACK}$ Indicates transfer acknowledge on the system bus to insure 68000 family compatibility.
1 = BE6 External test condition.

BIT 5: BA/BE5

0 = BA BUS available. Indicates to the master that the pseudo-slave is not using the system bus for generating addresses on local bus.
1 = BE5 External test condition.

BIT 6: MASK (TS68931 only)

0 = AMR is not masked. When an external halt is applied to the processor the AMR register does not change.
1 = AMR is masked. When an external halt is applied to the processor the AMR register changes to the following state: FAST EXCHANGE, PSEUDO-SLAVE, CONCATENATED BUS, $\overline{RD}$ and $\overline{WR}$ control pulses.

This bit can be modified by the programmer even while the $\overline{HALT}$ is asserted.

5.6 RESET

The reset signal has the following effects on the different blocks on the circuit :

SEQUENCER
PC, LC cleared to zero.
IR loaded with NOP instruction.

STATUS:
- REAL mode
- no saturation
- empty FIFO (EF = 1)
- memorised overflow (MOVF) = 0.

X or YRAM
- no circular addressing mode.

AMR
- Fast exchange
- Slave
- Concatenated bus
- $\overline{RD}$ and $\overline{WR}$
- BE6
- BE5.

RESET must be maintained for a minimum of 3 clock cycles (480 ns) to be effective.

5.7 HALT (TS68931 only)

The external halt signal will freeze the program counter and the loop counter. The instruction register can then be loaded from an external source. This signal is used for system development. If the MASK bit = 1 it will force the AMR into the following state: FAST EXCHANGE, SLAVE, SEPARATE BUS, RD and WR control pulses.

SECTION 6
INPUT/OUTPUT

6.1. DUAL-BUS INTERFACE

In order to permit a maximum versatility the processor interface provides two buses :
- the system Bus AD0-AD7
- the local Bus D0-D5.

This dual-bus interface allows the processor to be used in the following ways :
a) a microprocessor peripheral (fig. 6.A.)
b) a slave of another processor (fig. 6.B.)
c) a stand-alone unit connected to a peripheral or a data converter (fig. 6.C.)
d) a processor and its external memory (fig. 6.D.)
e) an intelligent peripheral connected to a general purpose microprocessor (fig. 6.E.)

These are some examples of the possibilities offered by the dual-bus interface. In addition very sophisticated multiprocessor machines can be built based on the principle of tree hierarchy (fig. 6.F.). In effect each processor becomes nested in the multiprocessor machine in the same way as subroutines are nested in a program tree.

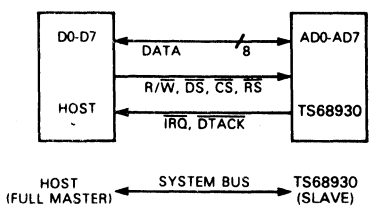


FIGURE 6.A. - HOST/TS68930

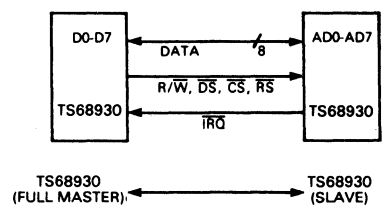


FIGURE 6.B. - TS68930/TS68930

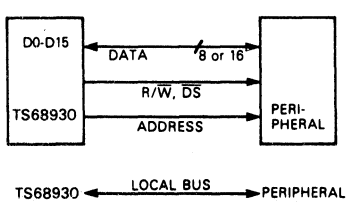


FIGURE 6.C. - TS68930/PERIPHERAL

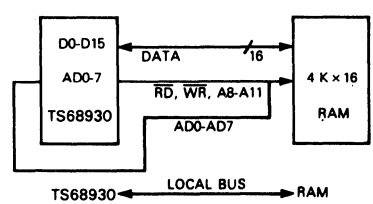


FIGURE 6.D. - TS68930/RAM

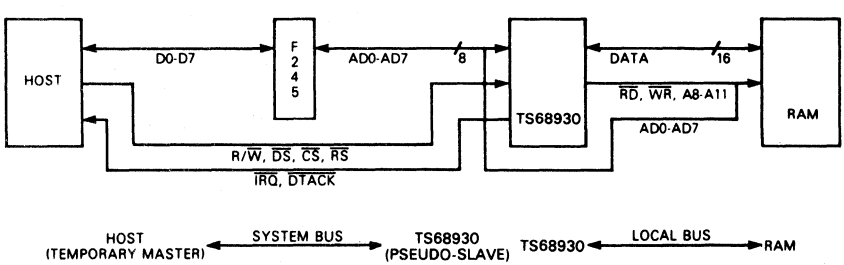


FIGURE 6.E. - TEMPORARY MASTER/PSEUDO-SLAVE

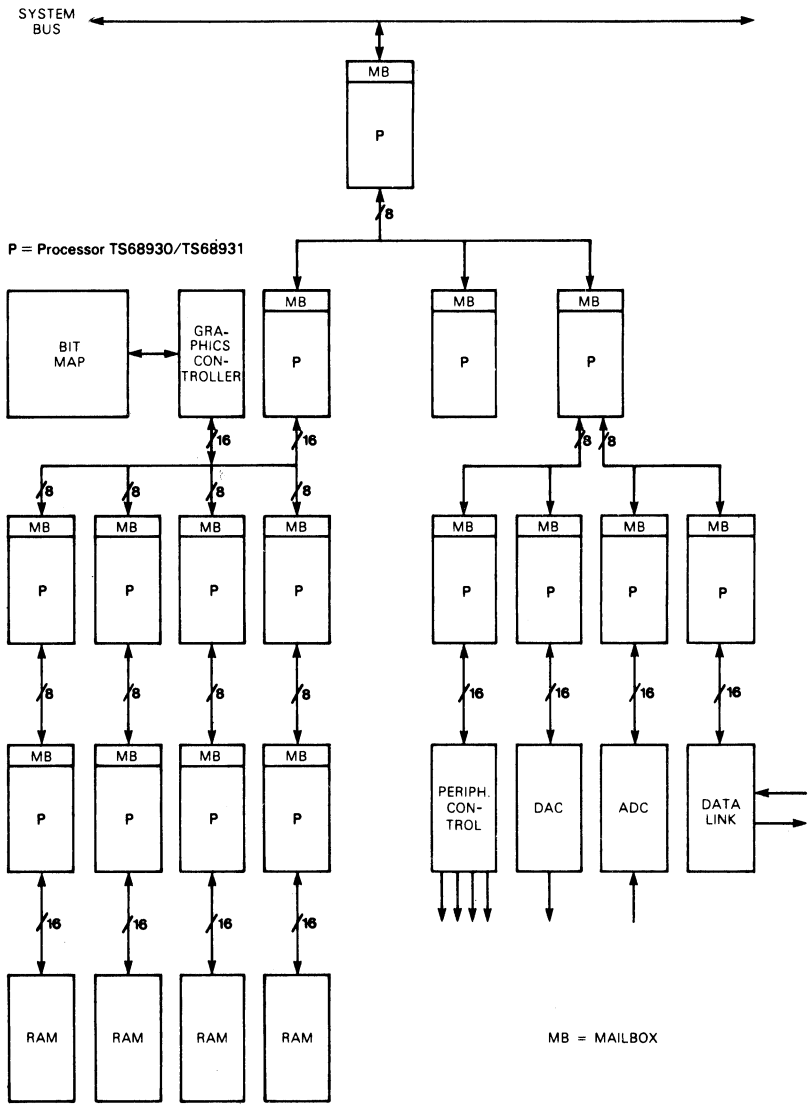


FIGURE 6.F. - MULTIPROCESSING MACHINE

6.2. MASTER/SLAVE

The processor is **a master on its local bus** and **a slave on its system bus.** There are times where the processor needs to access an external RAM and for that purpose will use the system bus to generate the addresses.

In this case this circuit prevents the master from using the bus freely and for that reason is called **a pseudo-slave.** Since the master can only gain access to the bus temporarily it is now defined as a **temporary master**.

It is the programmer who decides whether the processor should behave as a slave or a pseudo-slave.

This is done by programming the Access Mode Register.

That gives four different types of processor configurations:

PSI type	Definition
SLAVE (SL)	Its system bus is used to exchange data with a full master.
PSEUDO-SLAVE (PS)	Its system bus is also used to generate addresses for its local external memory.
FULL-MASTER (FM)	It has complete mastership of its local bus.
TEMPORARY-MASTER (TM)	Its local bus is shared with another processor which uses it to generate addresses.

These exchange type can be summarized to three possible connections:
1) Full master ↔ slave
2) Full master ↔ memories or peripherals
3) Temporary master ↔ pseudo-slave.

Connection 1 (with reference to fig. 6.A., 6.B.):

The data is exchanged through a mailbox and the exchange follows the mailbox protocol.

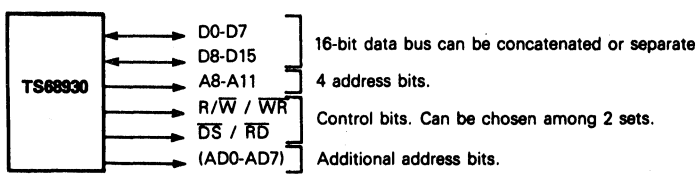
Connection 2 (example 6.C., 6.D., 6.E.):

The exchange is equivalent to reading and writing of data into locations or registers.

Connection 3 (example 6.E.):

The data is exchanged through a mailbox and the exchange follows the mailbox protocol.

6.3. LOCAL BUS PIN DESCRIPTION



$\overline{DS}$ = data strobe. Synchronizes the transfer.
R/$\overline{W}$ = indicates the direction of data.
$\overline{RD}$ = read clock pulse.
$\overline{WR}$ = write clock pulse.

The bus can take the form of two independent 8-bit buses or a single 16-bit bus.

There are four address bits (A8-A11) which are sufficient to address many slaves without requiring additionnal circuitry.

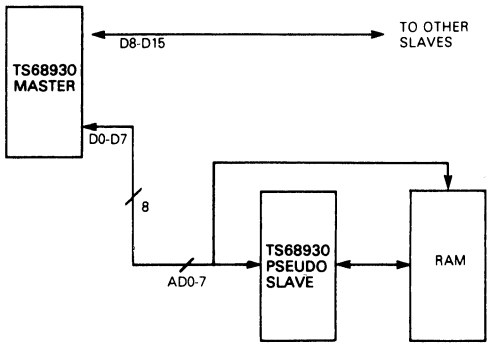
The address bus can be extended to 12 bits (AD0-AD7) to access an external memory.

If a peripheral is too slow to answer in one instruction cycle the processor can be programmed into a slow exchange mode. This mode is particularly useful for peripherals such as data converters, or the dedicated analogue interface circuit fabricated by THOMSON for modem applications. (The MAFE: Modem Analog Front-End).

SEPARATION OF LOCAL BUS

The processor offers the possibility of dividing the local bus D0-D15 into two independent 8-bit buses. This is used when a pseudo-slave monopolizes the bus to generate its own RAM addresses (fig. 6.3.) on D0-D7. By separating the bus, the processor can remain a full-master on D8-D15 even while being a temporary master on D0-D7, and it does not require the use of a bus transceiver on D0-D7.

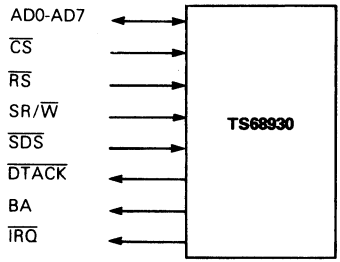
The selection between the 2 × 8-bit buses is made by the addresses A10-A11.



A11	A10	SELECTION
0	0	D0-D7
0	1	D8-D15
1	0	D8-D15
1	1	D8-D15

FIGURE 6.3. - SEPARATE LOCAL BUSES

6.4. SYSTEM BUS AND MAILBOX



AD0-AD7 = 8-bit data bus.
$\overline{CS}$ } = Mailbox control signal. Also used by master to gain access to bus.
$\overline{RS}$ }
SR/$\overline{W}$ = System Read/Write } Generated by external circuit (master)
$\overline{SDS}$ = System data strobe. }
$\overline{IRQ}$ = Handshake signal. Used by the master to gain access to mailbox (and bus).
$\overline{DTACK}$ = Data acknowledge. Compatibility with 68000 family.
BA = Bus available. The PSI is not currently using the system bus to generate addresses.

MAILBOX

The mailbox is comprised of two sets of registers : RIN and ROUT.

RIN (3 × 8-bit shift register).

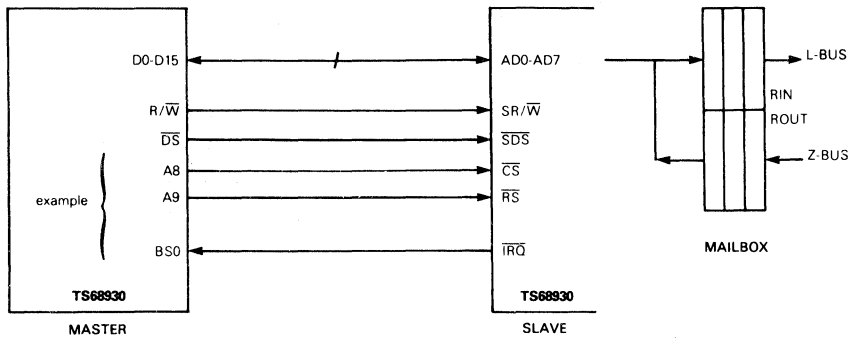
This register is read internally on the upper byte of L-BUS (L8-L15) and written externally from the system bus.

After each write operation (commanded by the external master) or slave read operation the data is shifted by 1.

ROUT (3 × 8-bit shift register).

This register is written internally with the upper byte of the Z-BUS (Z8-15) and read externally on the system bus by the external master. After each master read operation or slave write operation the data is shifted by 1.

6.5. MAILBOX PROTOCOL



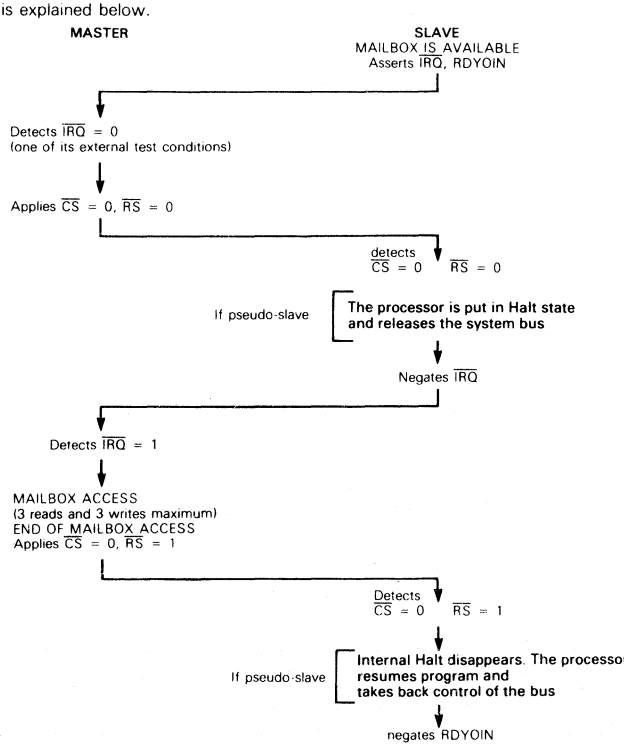
This protocol is hardwired on the slave side and programmed on the master side. The mailbox is included in the slave. The two slave address pins ($\overline{CS}$, $\overline{RS}$) are directly connected to two master address lines.

Therefore, the slave is seen as two external memory locations by the master which will address it by generating an external address directly or indirectly (pointer E0 or E1).

By addressing the location 00 the master echoes the $\overline{IRQ}$ to the slave and accesses the mailbox.

By addressing the location 01 the master releases the bus.

The complete protocol is explained below.



SIGNAL MEANING

RDYOIN

Internal flag indicating the property of the mailbox.
0 = Slave has access to the mailbox
1 = Master has access to the mailbox.

a) RDYOIN is set by the slave and reset by the master. That means that the slave gives the mailbox to the master when it finishes using it and vice-versa. In no case can the master or the slave request the mailbox, it can only wait for the other to give it back.

b) From the slave point of view, RDYOIN is a flag :
- tested by a branch instruction
- set by an initialization instruction.

$\overline{IRQ}$

Handshake signal used by the master to gain access to the mailbox;

a) **$\overline{IRQ}$ is asserted by the slave** to indicate the availability of the mailbox (at the same time as RDYOIN).

b) The master (**after testing $\overline{IRQ}$**) knows that it can access the mailbox but does not know if it has access to the bus (since it does not know if the slave is behaving as a pseudo-slave).
It requests the bus by generating the address $\overline{CS}$ = 0, $\overline{RS}$ = 0.

c) The slave internal I/O sequencer answers back by **negating $\overline{IRQ}$.** The master has now full control of the bus and the mailbox.
When the master has completed the exchange it generates the address CS = 0, $\overline{RS}$ = 1 and the slave internal I/O sequencer resets RDYOIN.

HALT (internal)

The internal halt has the following effects on the circuit :
- the program is stopped at the end of the current instruction; the program and loop counters are frozen
- a NOP is generated on the instruction bus
- no more addresses are generated on the system bus.

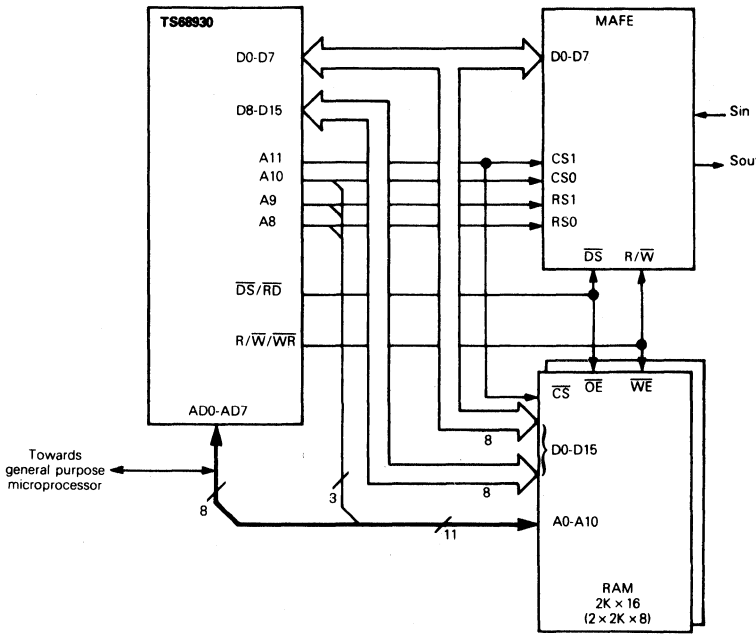
6.6. INSTRUCTION BUS (TS68931 only)

For the TS68931, CROM (512 x 16-bit) and IROM (64k x 32-bit) are external. They are read using the I-BUS, on which are multiplexed:
— the 16-bit instruction ROM address
— the 9-bit coefficient ROM address + 1 Output Enable bit (ENCROM)
— the 32-bit instruction code.

In order to synchronize the exchanges, an additional signal is generated: INCYCLE.
It is the internal instruction clock.

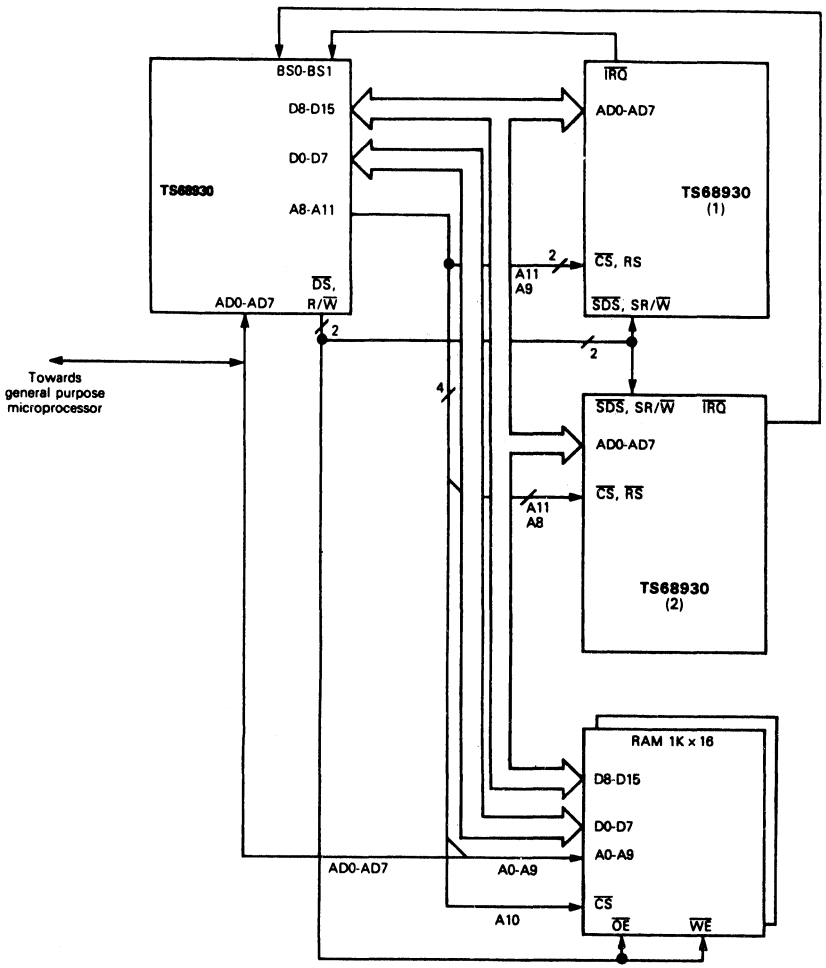
Data from CROM are read on the local bus.

6.7. APPLICATION EXAMPLES



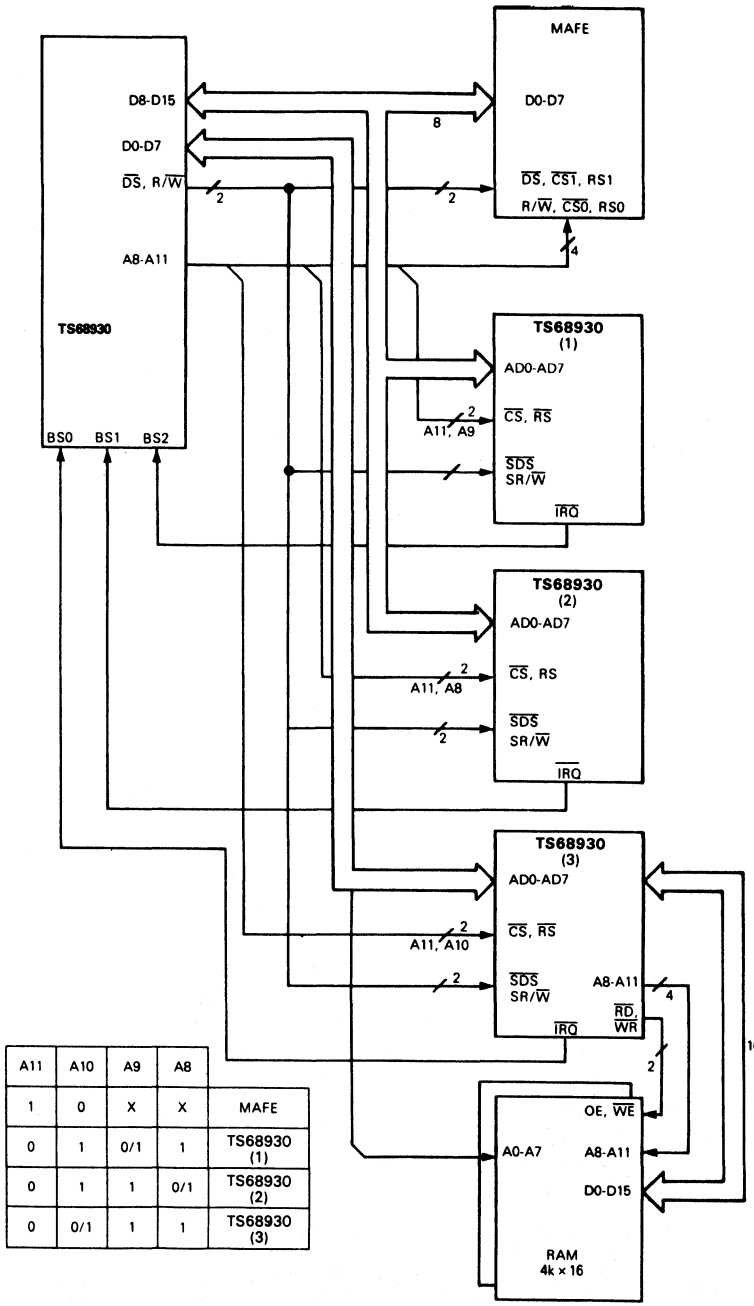
A11	A10	A9	A8	
1	0	X	X	MAFE
0	X	X	X	RAM

FIGURE 6.7.A. - CONFIGURATION EXAMPLE: TS68930 + RAM + MAFE



A11	A10	A9	A8	
0	1	0/1	1	TS68930 (1)
0	1	1	0/1	TS68930 (2)
1	0	X	X	RAM

FIGURE 6.7.B. - CONFIGURATION EXAMPLE: 3 TS68930 + RAM



A11	A10	A9	A8	
1	0	X	X	MAFE
0	1	0/1	1	TS68930 (1)
0	1	1	0/1	TS68930 (2)
0	0/1	1	1	TS68930 (3)

FIGURE 6.7.C. - CONFIGURATION EXAMPLE: 4 TS68930 + MAFE + RAM

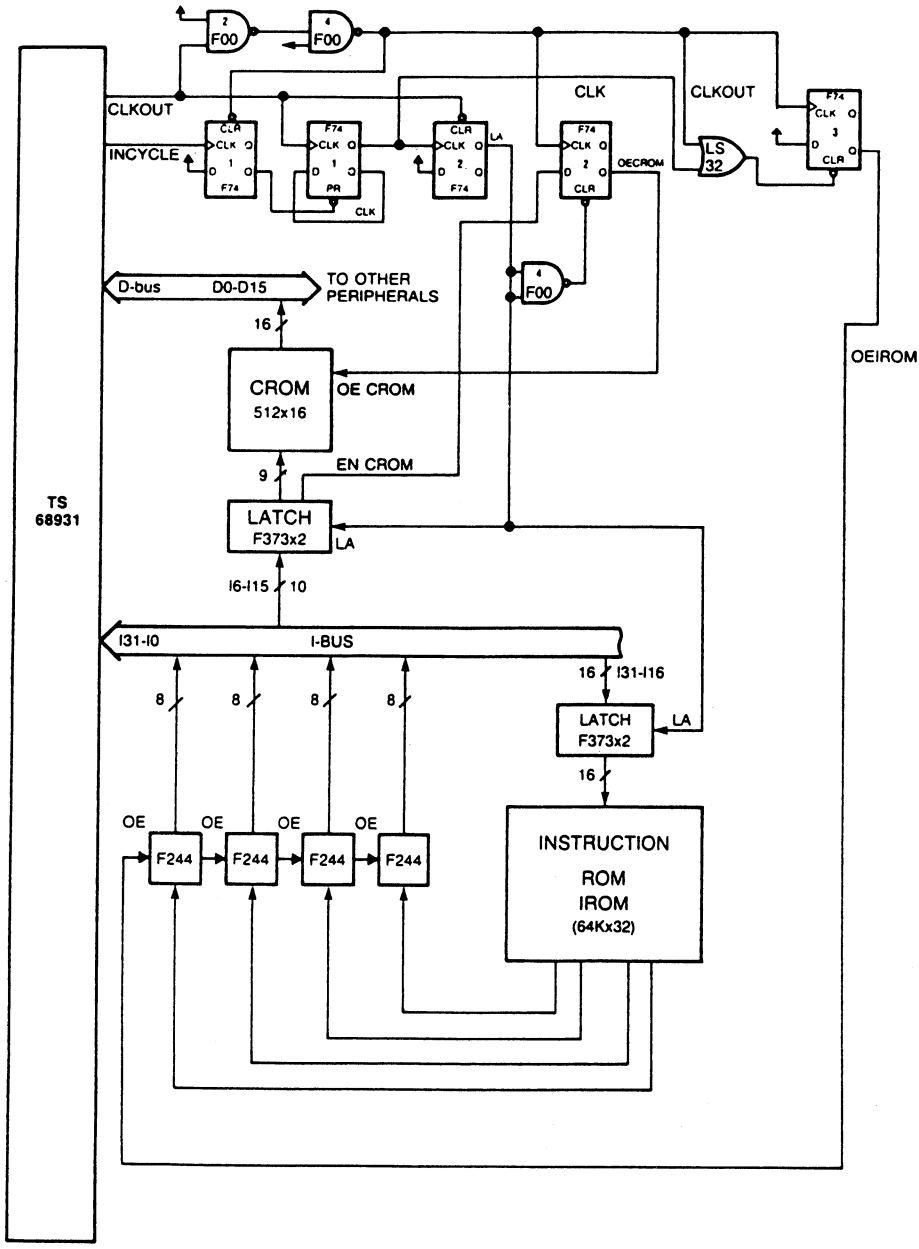


FIGURE 6.7.D. - I-BUS INTERFACE (TS68931)

SECTION 7
INSTRUCTION SET

Type	Mnemonic	Operation	Number of cycles	
			REAL	CPLX DBPR
Calculation, instruction with indirect addresing	OPIN	This instruction refers to operands indirectly addressed	1	2
Calculation, instruction with direct addressing	OPDI	The operand sourcing the L-BUS is directly addressed	1	2
Calculation, instruction with immediate operand	OPIM	An immediate operand is read on R-RUS	1	2
General shift Instruction	ASR ASL LSR ROR	The operand sourcing the L-BUS can be shifted/rotated by 0 → 15 bits	1	2
Immediate branch Instruction	BRI	Conditional / unconditional branch to direct address	2	2
Computed branch Instruction	BRC	Conditional / unconditional branch to computed address	2	2
Data transfer Instruction	SVR	This instruction is used to save register contents in external or internal RAM	1	2
Initialization and control instruction	INI	Pointers, access mode register, loop counter, mode initialization	1	2

INSTRUCTION SET LANGUAGE DEFINITIONS

LDT	Load L-BUS source into transfer register T
R SRC	R-BUS source
L SRC	L-BUS source
SL	ALU input selection - left side
SR	ALU input selection - right side
ALU DST	ALU output destination
ALUCODE	ALU codes
LDM	Load L-BUS source into multiplier input M
LDN	Load R-BUS source into multiplier input N
Z SRC	Z-BUS source
Z DST	Z-BUS destination
ZT	Load Z-BUS into transfer register T
ACE	Post incrementation: pointers CROM or ERAM
AY	Post incrementation: pointers YRAM
AX	Post incrementation: pointers XRAM
BRA	Branch address source
FT	False / True condition
SVPC	Save program counter
JDST	Destination register for J constant
KDST	Destination register for K constant
MODE	Operating mode
SAT	Saturation flag
ADOF	Even / odd flag
J7	YRAM circular addressing mode flag
J constant	8-bit constant used to initialize registers
K7	XRAM circular addressing mode flag
K constant	12-bit constant used to initialize registers.

7.1. OPERATING CODE FORMATS

Bit	Field	Operations and codes
0 1	OP CODE	00
2	LDT	0-NO LOAD, 1-LBUS → T
3 4	R SRC	00 01 10 11 [X0] [E0] [Y0] [Y1]
5 6 7	L SRC	000 001 010 011 100 101 110 111 [X0] [X1] [Y0] RIN T [E1] [C0] [C1]
8	SL	0-LBUS / 1-P
9	SR	0-RBUS / 1-A/B (REFER TO ALU DST)
10 11 12 13 14	ALU CODE	CF. SPECIAL TABLE
15 16	ALU DST	00 01 10 11 D F A B
17 18 19	Z SRC	000 001 010 011 100 101 110 111 D F A B T CCR — —
20	LDM	0-NO LOAD / 1-LBUS → M
21	LDN	0-NO LOAD / 1-RBUS → N
22 23	ACE	00 01 10 11 +0 +1 — −1
24 25	AY	00 01 10 11 +0 +1 — −1
26 27	AX	00 01 10 11 +0 +1 — −1
28 29 30	Z DST	000 001 010 011 100 101 110 111 NONE ROUT [Y0] [Y1] [E0] [E1] [X0] [X1]
31	ZT	0-NO LOAD / 1-ZBUS → T

FIGURE 7.1. - OPIN: CALCULATION INSTRUCTION WITH INDIRECT ADDRESSING

Bit	Field	Operations and codes
0 1 2	OP CODE	010
3 4	R SRC	00 01 10 11 [X0] [E0] [Y0] [Y1]
5 6 7	L SRC	000 001 010 011 100 101 110 111 X — Y RIN T E — C
8	Z SRC	0-D / 1-F
9	SR	0-RBUS / 1-A
10 11 12 13 14	ALU CODE	CF. SPECIAL TABLE
15	ALU DST	0-F / 1-A
16 17 18 19 20 21 22 23 24 25 26 27	LBUS DIRECT ADDRESS	MSB LSB
28 29 30 31	Z DST	0000 0010 0100 0110 1000 1010 1100 1110 NONE ROUT [Y0] [Y1] [E0] [E1] [X0] LCR 0001 0011 0101 0111 1001 1011 1101 1111 X0 X1 Y0 Y1 E0 E1 C0 C1

FIGURE 7.2. - OPDI: CALCULATION INSTRUCTION WITH DIRECT ADDRESSING

OPERATING CODE FORMATS (Continued)

Bit	Field	Operations and codes
0 1 2 3 4	**OP CODE**	**01110**
5 6 7	**L SRC**	000 001 010 011 100 101 110 111 **[X0] [X1] [Y0] RIN T [E1] [C0] [C1]**
8	**SL**	**0-LBUS / 1-P**
9	**SR**	**0-RBUS / 1-A**
10 11 12 13 14	**ALU CODE**	**CF. SPECIAL TABLE**
15	**ALU DST**	**0-F / 1-A**
16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31	**IMMEDIATE VALUE**	**MSB** **LSB**

FIGURE 7.3. - OPIM: CALCULATION INSTRUCTION WITH IMMEDIATE OPERAND

Bit	Field	Operations and codes
0 1 2 3 4	**OP CODE**	**01111**
5 6 7	**L SRC**	000 001 010 011 100 101 110 111 **X — Y RIN T E — C**
8	**SL**	**0-LBUS / 1-P**
9 10	**ALU CODE**	00 01 10 11 **ASR LSL LSR ROR**
11 12 13 14	**SHIFT VALUE**	0000 0001 ..... 1111 **0 1 ..... 15**
15	**ALU DST**	**0-F / 1-A**
16 17 18 19 20 21 22 23 24 25 26 27	**LBUS DIRECT ADDRESS**	**MSB** **LSB**
28 29 30 31		

NOTE: When LSR, ASR, ROR shift value is complemented to 2

FIGURE 7.4. - ASR, LSL, LSR, ROR: SHIFT INSTRUCTIONS

OPERATING CODE FORMATS (Continued)

Bit	Field	Operations and codes
0 1 2	OP CODE	100
3	BRA	0-IR, 1-RAR
4	FT	0-FALSE, 1-TRUE
5 6 7 8	COND	REFER TO SPECIAL TABLE
9	SVPC	0-NO SVPC, 1-PC → RAR
10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25	BRANCH ADDRESS	MSB LSB
26 27	AX	00 01 10 11 +0 +1 — −1
28 29 30	Z DST	000 001 010 011 100 101 110 111 NONE — [Y0] [Y1] — — [X0] [X1]
31	ZT	0-NO LOAD, 1-ZBUS → T

FIGURE 7.5. - BRI: IMMEDIATE BRANCH INSTRUCTION

Bit	Field	Operations and codes
0 1 2 3	OP CODE	1010
4	FT	0-FALSE, 1-TRUE
5 6 7 8	COND	REFER TO SPECIAL TABLE
9	SVPC	0-NO SVPC, 1-PC → RAR
10 11 12 13 14 15		
16 17 18 19	BRANCH SOURCE	000 001 010 011 100 101 110 111 — F A B T — — —
20 21 22 23 24 25		
26 27	AX	00 01 10 11 +0 +1 — −1
28 29 30	Z DST	000 001 010 011 100 101 110 111 NONE — [Y0] [Y1] — — [X0] [X1]
31	ZT	0-NO LOAD, 1-ZBUS → T

FIGURE 7.6. - BRC: COMPUTED BRANCH INSTRUCTION

OPERATING CODE FORMATS (Continued)

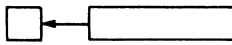
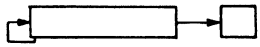
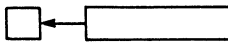
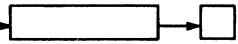
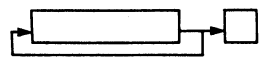
Bit	Field	Operations and codes
0 1 2 3 4 5	OP CODE	011000
6 7 8 9	Z SRC	0000 X0 1000 AMR 0001 X1 1001 LC 0010 Y0 1010 A 0011 Y1 1011 F 0100 E0 1100 D 0101 E1 1101 STA 0110 C0 1110 — 0111 C1 1111 —
10 11 12 13 14 15		
16 17 18 19 20 21 22 23 24 25 26 27	ZBUS DIRECT ADDRESS	MSB LSB
28 29 30	Z DST	000 NONE 001 ROUT 010 Y 011 — 100 E 101 — 110 X 111 —
31	ZT	0-NO LOAD, 1-ZBUS → T

FIGURE 7.7. - SVR: DATA TRANSFER INSTRUCTION

Bit	Field	Operations and codes
0 1	OP CODE	11
2 3 4	J DST	000 AMR 001 LCD 010 Y0 011 Y1 100 — 101 RDYOIN 110 EF 111 NONE
5 6 7	K DST	000 X0 001 X1 010 LCI-LCR 011 NONE 100 E0 101 E1 110 C0 111 C1
8 9	MODE	00 — 01 REAL 10 DBPR 11 CPLX
10	SAT	0 NO SATURATION MODE 1 SATURATION MODE
11	ADOF	0 NO INVERSION 1 INVERSION LSB ADDRESS X/Y RAM
12 13 14 15 16 17 18 19	J7 J CONSTANT J0	J7 0 YRAM NORMAL MODE 1 YRAM CIRCULAR ADDRESSING MODE
20 21 22 23 24 25 26 27 28 29 30 31	K11 K CONSTANT K0	K7 0 XRAM NORMAL MODE 1 XRAM CIRCULAR ADDRESSING MODE

FIGURE 7.8. - INI: INITIALIZATION AND CONTROL INSTRUCTION

7.2. ALU CODES

MNEMO-	Function	SR	SI	CR	CI	Z	OV F	MO VF	AO VF	CODE
ADD	A + B	*	*	*	*	*	*	*	*	00010
ADDC	A + B + CARRY	*	*	*	*	*	*	*	*	00011
ADDS	B + A/16	*	*	*	*	*	*	*	*	00001
ADDX	B + A* (COMPLEX CONJUGATE)	*	*	*	*	*	*	*	*	01010
AND	A . B	*	*	0	0	*	0	–	*	01110
ASL	CARRY  0	*	*	*	*	*	*	–	*	01011
ASR	 CARRY	*	*	*	*	*	0	–	*	01111
CLR	CLEAR	0	0	0	0	1	0	–	0	10011
COM	COMPLEMENT A	*	*	0	0	*	0	–	*	10110
COM	COMPLEMENT B	*	*	0	0	*	0	–	*	11000
LCCR	LBUS → CCR	*	*	*	*	*	*	*	*	01001
LSL	CARRY  0	*	*	*	*	*	0	–	*	11011
LSLB	LSL BYTE	*	*	*	*	*	0	–	*	11001
LSR	0  CARRY	*	*	*	*	*	0	–	*	00111
LSRB	LSR BYTE	*	*	*	*	*	0	–	*	11010
NOP		–	–	–	–	–	–	–	–	00000
OR	A ∧ B	*	*	*	0	*	0	–	*	01101
RCE	EXECUTE RC	*	*	*	*	*	*	*	*	10001
RCER	EXECUTE RC / LOAD NEW CODE	*	*	*	*	*	*	*	*	10000
RCR	LOAD RC									10010
ROR	 CARRY	*	*	*	*	*	0	–	*	10111
SBC	A + $\overline{B}$ + CARRY	*	*	*	*	*	*	*	*	00101
SBCR	$\overline{A}$ + B + CARRY	*	*	*	*	*	*	*	*	01000
SET		*	*	0	0	0	0	–	0	11100
SUB	A + $\overline{B}$ + 1	*	*	*	*	*	*	*	*	00100
SUBR	$\overline{A}$ + B + 1	*	*	*	*	*	*	*	*	00110
TRA	TRANSFER A	*	*	0	0	*	0	–	*	10100
TRA	TRANSFER B	*	*	0	0	*	0	–	*	10101
XOR	A ⊕ B	*	*	0	0	*	0	–	*	01100

* Affected bit.

Notes :

1) A/B refer to ALU inputs (RESP. LSIDE/RSIDE) not to accumulators A/B

2) In ASL the Carry bit is equivalent to exclusive - or of bit 14 and 15.

7.3. TEST CONDITIONS

TRUE CONDITION	FALSE CONDITION	CODE
BE3	NO BE3	0100
BE4	NO BE4	0010
BE5	NO BE5	0011
BE6	NO BE6	0001
BRANCH ALWAYS	BRANCH NEVER	0000
BS0	NO BS0	1100
BS1	NO BS1	1101
BS2	NO BS2	1110
CI	NO CI	1010
CR	NO CR	0110
MOVF	NO MOVF	1011
OVF	NO OVF	0111
RDYOIN	NO RDYOIN	1111
SI	NO SI	1001
SR	NO SR	0101
Z	NO Z	1000

SECTION 8
PERFORMANCE EVALUATION

	TIME (μs)
TRANSVERSAL FILTER (N COEFFICIENTS) - (1)	
REAL COMPLEX ADAPTIVE REAL ADAPTIVE CMPLX	0.160 x N 0.320 x N 0.320 x N 0.640 x N
BIQUAD FILTER - 4 COEFF	0.960
LATTICE FILTER - 10 STAGE (1)	6.4
AUTOCORRELATION - 10 th ORDER (2) (240 samples) (32-bit result)	 8 μs/sample 1.8 ms total
FFT (RADIX 2 - DIF - algorithm) (2) (3)	
64 - POINT COMPLEX 128 - POINT REAL 256 - POINT COMPLEX	265 270 2000
COSINE CALCULATION	2.4

Notes :
(1) Excluding initialization, context switching, pipeline.
(2) Using external RAM.
(3) Including loading/unloading, scaling, bit reserve.

SECTION 9
ELECTRICAL SPECIFICATIONS

9.1. MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply voltage	V_{CC}*	−0.3 to 7.0	V
Input voltage	V_{in}*	−0.3 to 7.0	V
Operating temperature range	T_A	0 to 70	°C
Storage temperature range	T_{stg}	−55 to 150	°C
Max. power dissipation	P_{Dmax}	3	W

* With respect to V_{SS}

Stresses above those hereby listed may cause permanent damage to the device. The ratings are stress ones only and functional operation of the device at these or any conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. Standard MOS circuits handling procedure should be used to avoid possible damage to the device.

9.2. DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0 V ± 5 %, V_{SS} = 0, T_A = 0 to + 70°C (Unless otherwise specified)

Characteristic	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.75	5	5.25	V
Input low voltage	V_{IL}	−0.3	–	0.8	V
Input high voltage	V_{IH}	2.4	–	V_{CC}	V
Input leakage current	I_{in}	–	–	10	μA
Output high voltage (I_{load} = −300 μA)	V_{OH}	2.7	–	–	V
Output low voltage (I_{load} = 3.2 mA)	V_{OL}	–	–	0.5	V
Power dissipation	P_D	–	1.5	–	W
Input capacitance	C_{in}	–	10	–	pF
Three state (off state) input current	I_{TSI}	–	–	10	μA

9.3. AC ELECTRICAL SPECIFICATIONS - CLOCK AND CONTROL PINS TIMING

(V_{CC} = 5.0 V ± 5 %, T_A = 0° to + 70°C; see figure 9.1.)

OUTPUT LOAD = 50 pF + DC characteristics I load

REFERENCE LEVELS: V_{IL}: 0.8 V V_{IH}: 2.4 V
V_{OL}: 0.8 V V_{OH}: 2.4 V

tr, tf ⩽ 5 ns for input signals

Characteristic	Symbol	Min	Typ	Max	Unit
External clock cycle time	tcex	40		160	ns
External clock fall time	tfex			5	ns
External clock rise time	trex			5	ns
EXTAL to CLKOUT high delay	tcoh		25		ns
EXTAL to CLKOUT low delay	tcol		25		ns
CLKOUT rise time	tcor			10	ns
CLKOUT fall time	tcof			10	ns
CLKOUT to $\overline{DS}$, $\overline{RD}$, $\overline{WR}$ low	tdsl		5		ns
CLKOUT to DS, RD, WR high	tdsh		5		ns
Control inputs set-up time (BS0...BS2, BE3...BE6, Reset, halt)	tsc	20			ns
Control inputs hold time (BS0...BS2, BE3...BE6, $\overline{Reset}$, halt)	thc	10			ns
CLKOUT to control output low ($\overline{IRQ}$, BA)	tdlc			50	ns
CLKOUT to control output high (BA)	tdhc			50	ns

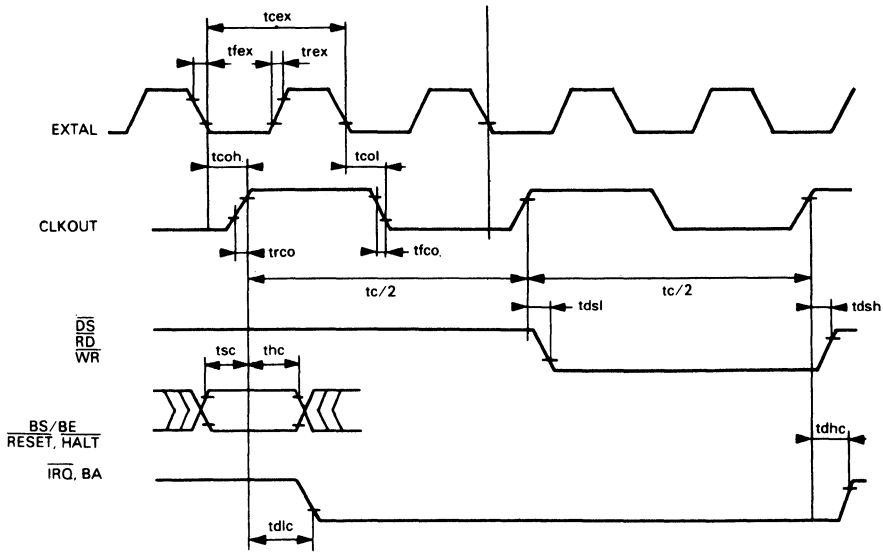
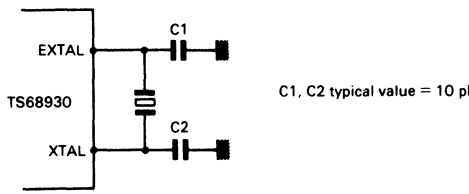


FIGURE 9.1. - CLOCK AND CONTROL PINS TIMING

INTERNAL CLOCK OPTION

A crystal oscillator can be connected across XTAL and EXTAL. The frequency of CLKOUT: tc/2 is half the crystal fundamental frequency.



9.4. AC ELECTRICAL SPECIFICATIONS - LOCAL BUS TIMING

(V_{CC} = 5.0 V ± 5 %, T_A = 0° to + 70°C; see figure 9.2.)

Characteristic	Symbol	Min.	Max.	Unit
$\overline{RD}$, $\overline{WR}$, $\overline{AS}$ pulse width	t_{PW}	1/2 tc - 15	1/2 tc	ns
address hold time	t_{AH}	10	–	ns
data set-up time, write cycle	t_{DSW}	25	–	ns
data hold time, write cycle	t_{DHW}	10	–	ns
data set-up time, read cycle	t_{DSR}	20	–	ns
data hold time, read cycle	t_{DHR}	5	–	ns
address valid to $\overline{WR}$, $\overline{AS}$, $\overline{RD}$ low	t_{ARW}	1/2 tc - 40	–	ns

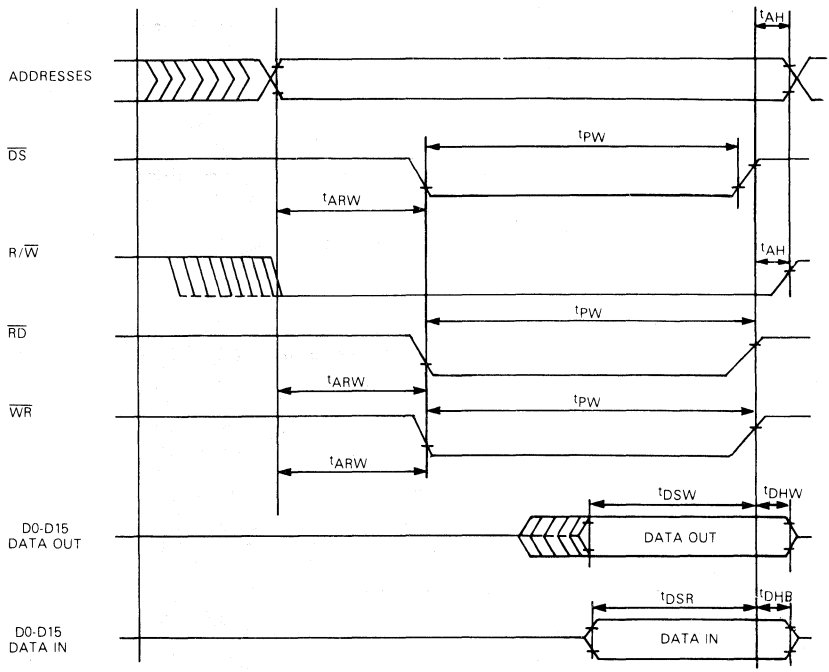


FIGURE 9.2. - LOCAL BUS TIMING DIAGRAM

9.5. AC ELECTRICAL SPECIFICATIONS - SYSTEM BUS TIMING

(V_{CC} = 5.0 V ± 5 %, T_A = 0° to + 70°C; see figure 9.3.)

Characteristic	Symbol	Min.	Max.	Unit
$\overline{SDS}$ pulse width	t_{SPW}	60	–	ns
SR/$\overline{W}$, $\overline{CS}$, $\overline{RS}$ set-up time	t_{SAW}	20	–	ns
SR/$\overline{W}$, $\overline{CS}$, $\overline{RS}$ hold after $\overline{SDS}$ high	t_{SAH}	5	–	ns
data set-up time, read cycle	t_{SDSR}	20	–	ns
data hold time, read cycle	t_{SDHR}	5	–	ns
data set-up time, write cycle	t_{SDSW}	–	35	ns
data hold time, write cycle	t_{SDHW}	10	50	ns
$\overline{SDS}$ low to $\overline{DTACK}$ low	t_{DSLDT}	–	50	ns
$\overline{SDS}$ high to $\overline{DTACK}$ high*	t_{DSHDT}	–	50	ns
$\overline{SDS}$ high to $\overline{IRQ}$ high	t_{DSHIR}		50	ns

* DTACK is an open drain output test load include R_L = 820 Ω at V_{CC}

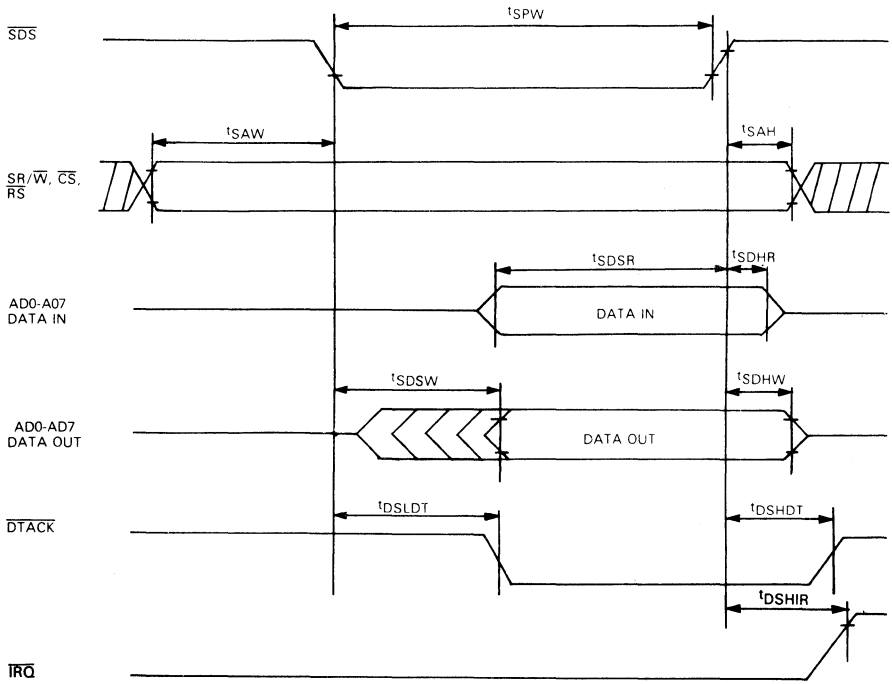


FIGURE 9.3. - SYSTEM BUS TIMING DIAGRAM

9.6. - AC ELECTRICAL SPECIFICATIONS - INSTRUCTION BUS TIMING

(V_{CC} = 5.0 V ± 5 %, T_A = 0° to + 70°C; see figure 9.4.)

Characteristic	Symbol	Min	Max	Unit
CLKOUT high to INCYCLE high	t_{INCH}	5	15	ns
CLKOUT low to INCYCLE low	t_{INCL}	5	15	ns
CLKOUT high to address valid	t_{IASW}		40	ns
I-BUS address hold	t_{IAHW}	20	40	ns
Instruction valid	t_{IISR}	20		ns
Instruction hold	t_{IIHR}	10		ns
CROM data set-up time	t_{DSR}	tc/2 - 40		ns
CROM data hold time	t_{DHR}	5		ns

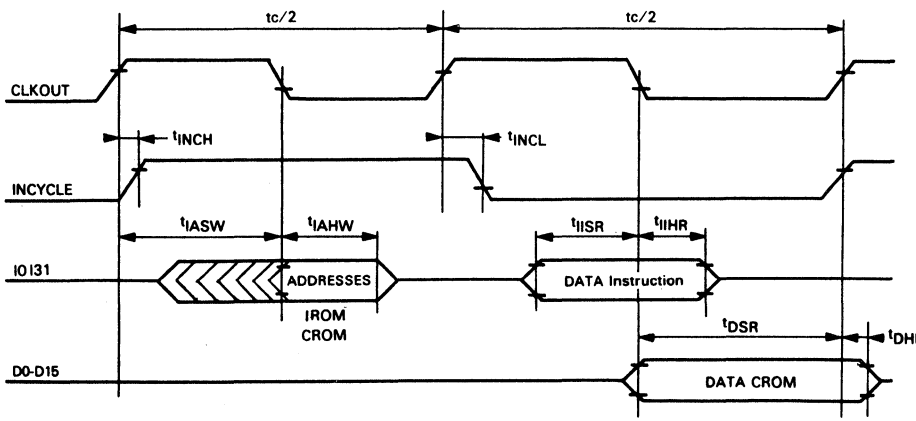
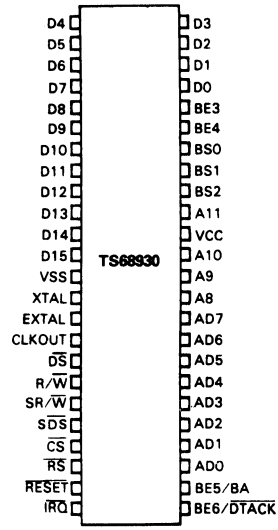


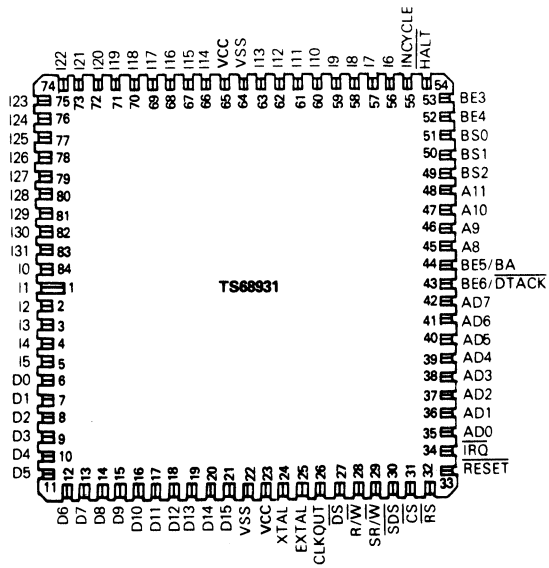
FIGURE 9.4. - I-BUS TIMING DIAGRAM

SECTION 10
PIN ASSIGNMENTS AND MECHANICAL DATA

10.1. - PIN ASSIGNMENTS



48-Pin Dual-in-Line Package



84-Terminal Chip Carrier (LCCC)

TS68931 84-Pin Grid Array (see table 10-1 Pin Assignments)

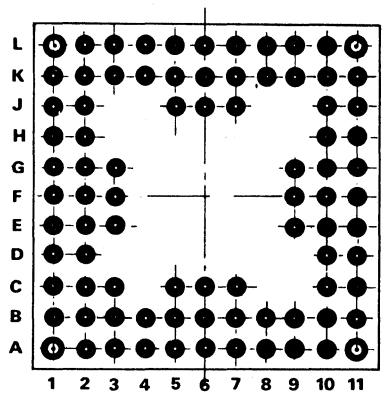
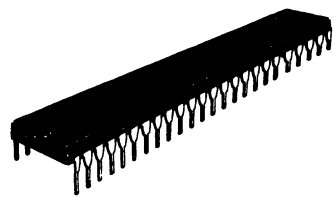


TABLE 10-1 PIN ASSIGNMENTS

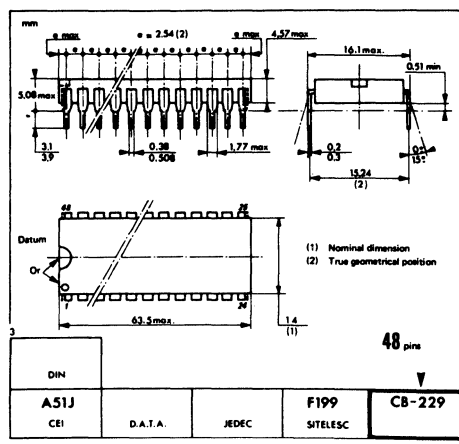
A1	I22	B11	B50	F9	BE6/$\overline{\text{DTACK}}$	K2	D6
A2	I20	C1	I26	F10	AD4	K3	D7
A3	I19	C2	I24	F11	BE5/BA	K4	D10
A4	I17	C5	I16	G1	I3	K5	D13
A5	I14	C6	VSS	G2	I4	K6	D15
A6	VCC	C7	I13	G3	I2	K7	EXTAL
A7	I12	C10	BE4	G9	AD7	K8	R/$\overline{\text{W}}$
A8	I9	C11	BS1	G10	AD5	K9	$\overline{\text{CS}}$
A9	I7	D1	I28	G11	AD6	K10	$\overline{\text{RESET}}$
A10	I6	D2	I27	H1	D0	K11	AD0
A11	BE3	D10	BS2	H2	D1	L1	D5
B1	I25	D11	A11	H10	AD2	L2	D8
B2	I23	E1	I31	H11	AD3	L3	D9
B3	I21	E2	I30	J1	D2	L4	D11
B4	I18	E3	I29	J2	D4	L5	D14
B5	I15	E9	A10	J5	D12	L6	CLKOUT
B6	I10	E10	A9	J6	VSS	L7	XTAL
B7	I11	E11	A8	J7	VCC	L8	$\overline{\text{DS}}$
B8	I8	F1	I5	J10	$\overline{\text{IRQ}}$	L9	SR/$\overline{\text{W}}$
B9	INCYCLE	F2	I0	J11	AD1	L10	$\overline{\text{SDS}}$
B10	$\overline{\text{HALT}}$	F3	I1	K1	D3	L11	$\overline{\text{RS}}$

10.2. - PACKAGE DIMENSIONS

CB-229



TS68930
P SUFFIX
PLASTIC PACKAGE



SECTION 11
ORDERING INFORMATION

Package Type	Temperature Range	Part Number
Plastic DIL P Suffix	0°C to + 70°C −40°C to + 85°C	TS68930CP TS68930VP
Ceramic DIL C Suffix	0°C to + 70°C −40°C to + 85°C	TS68930CC TS68930VC
LCCC E Suffix	0°C to + 70°C −40°C to + 85°C	TS68931CE TS68931VE
PGA R Suffix	0°C to + 70°C	TS68931CR

As the TS68930 is a programmable circuit, a special ordering procedure has to be used. In order to get information about this procedure as well as the customer ordering sheet, please contact our sales representatives.

FEATURES

- ☐ Versions available for: VAX - VMS, UNIX, ULTRIX PC/MS-DOS - ISM PC, XT, AT
- ☐ Macro Definition and Macro Call
- ☐ Conditional Assembly
- ☐ Simulation File Generation
- ☐ Data Memory File Generation
- ☐ Multiple Output Format Generation
- ☐ High Level Language Loop Facility
- ☐ Powerful Expression Facility

A DSP program has as one of its main objectives the most rapid execution possible. This goal can easily be met with the TS68930 DSP due to its 32-bit instructions and 3 data-bus structure which allow implementation and execution of sophisticated algorithms at maximum speeds. However, a DSP program must also have the characteristics of any other program. It must be fast to develop, easy to read, and simple to check. The TS68930/68931 Macro-Assembler has been developed with these goals in mind.

The TS68930/68931 Macro-Assembler (PSIMAC) is currently available for the VAX/VMS, VAX/UNIX, uVAX/ULTRIX, and the IBM PC-XT/AT MS/PC-DOS operating systems. The PC configuration requires a minimum of 640 Kb of RAM and a hard disk.

Assembly language is a computer-oriented language for writing programs, consisting of symbolic instructions and assembler directives. In assembly instructions, the user assigns symbolic addresses to memory locations and specifies instructions by means of symbolic (mnemonic) operation codes. The user specifies instruction operands by means of symbolic addresses and numbers.

Assembler directives control and process of making a machine language program from the assembly language program, placing data in the program and assigning symbols to values to be placed in the program. Assembler directives that place data in memory locations allow the user to assign symbolic addresses to those locations. Other advantages are the use of expressions as operands and the use of decimal numbers in expressions.

Conditional assembly allows the user to have more flexible programs.

Macro calls provide the means to create a macro language that is capable of calling source statements from other locations within the program. A macro call fetches the source statements defined by the macro and substitutes them for the macro as if they had been written in that location in the program. The obvious advantage to using macro code is that less source code must be written, and this in turn means that the programs become easier to read and debug. In addition, macros are executed faster than a comprable absolute code routine because no branching is involved.

FEATURES

- ☐ Version Available for VAX-VMS and IBM PC-XT/AT
- ☐ 1000 Instructions Per Second on a VAX Computer
- ☐ Step by Step Execution
- ☐ Break-Point on Value or Address
- ☐ Trace
- ☐ Access to All Internal Registers and Memories
- ☐ File-Associated I/O Simulation of Conventional Peripherals Connected to the DSP
- ☐ Force Contents of DSP Memories
- ☐ Detailed Help Function

The TS68930 Functional Simulator (PSIMUL) is a software program that simulates the internal operation of the TS68930 DSP for effective software development and program verification in non-realtime. Use of the Functional Simulator allows development and debugging of TS68930 software without the requirement of hardware.

The TS68930 Functional Simulator is currently available for the VAX (VMS) and IBM PC-XT/AT. The PC configuration requires a minimum of 640 Kb of RAM and a hard disk.

The simulator uses a coded form of the TS68930 DSP object code produced by the TS68930 Macro-Assembler. Simulation of A/D Converters, D/Converters, and other conventional peripherals is accomplished using associated input and output files.

All internal registers and memories of the TS68930 can be modified during a simulation session. During execution of the program, the internal registers and memories of the simulated TS68930 are modified as the host computer interprets each instruction. Simple or high level breakpoints may be used to suspend execution at a selected point in the program so that the internal registers and memories can be inspected and/or modified.

On-line help with the simulator commands is available by entering a simple HELP command.

FEATURES

- ☐ Multiplication/Accumulation Routines
- ☐ Operations on Complex Numbers
- ☐ Double Precision Shifts (32-bit Word)
- ☐ DSP Functions: Real, Complex and Adaptive Complex FIR
  Biquadratic Filter Routine
  Autocorrelation Routine
  Lattic Filter Routine
- ☐ Fast Fourier Transforms: Butterfly
  8-Point FFT
  64-Point FFT
- ☐ Arithmetic Functions: Normalization and Denormalization
  32 × 32 Multiplication
  Square Root
  Division and Inversion
  Rectangular to Polar Coordinates
  Sine and Cosine of an Angle
- ☐ Macros, Modules and Hints for DSP Software Development

The TS68930/68931 DSP Module Library contains the major DSP routines required in the implementation of the algorithms used in DSP applications. These routines and macros were all written in TS68930/1 source code and can readily be incorporated into the users program.

The DSP Module Library (PSILIB) is available for the IBM PC, XT, AT and VAX-VMS (1600 BPI magnetic tape) as well as in printed form (publication no. 4430225).

FEATURES

- ☐ Full Speed TS68930/68931 Emulation (160 ns)
- ☐ Step by Step Execution
- ☐ Simple and High Level Breakpoints
- ☐ 68000 Based Monitor
- ☐ Line Assembler and Disassembler
- ☐ Program Down-loading from VAX, IBM PC-XT/AT or HDS-PSI
- ☐ Program RAM of 2K × 32
- ☐ Read and Modify all Registers and Memories of the DSP
- ☐ Two RS232 Serial Links for Terminal, Host or Printer

DESCRIPTION

The TS68930/68931 Evaluation and Emulation Board (EVAPSI) is a powerful-stand-alone development tool intended for the evaluation of the TS68930/1 DSP. The EVAPSI board has been designed to be compatible with the Macro-Assembler, Functional Simulator and Hardware Development System (HDS-PSI) development tools. The EVAPSI allows full application development and implementation.

The 68000 based interactive monitor features a menu-driven display and also supports a Line Assembler and Disassembler as well as Communication Software enabling Uplink/Downlink with VAX, IBM PC or HDS-PSI configured as hosts. All software required for operation of the EVAPSI is resident within 4 on-board EPROMs.

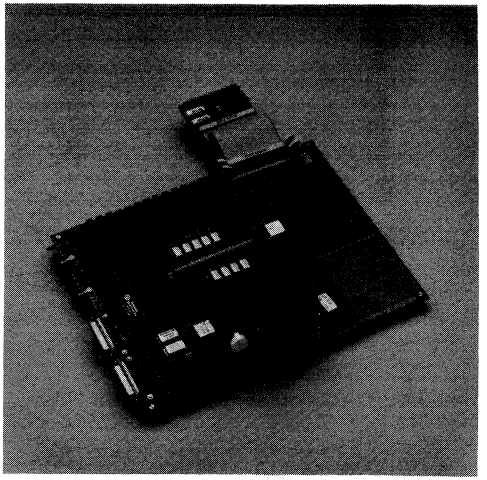


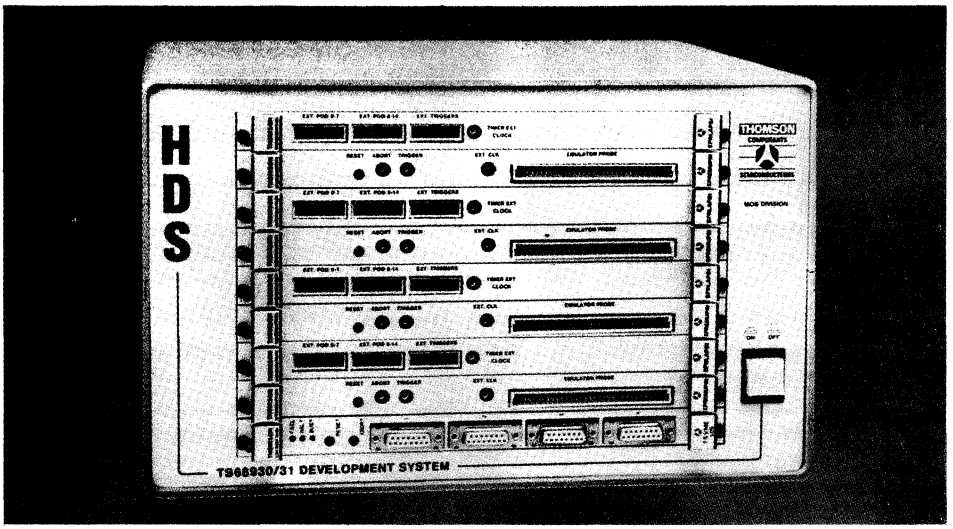
Figure 1. EVAPSI

The EVAPSI board offers two probes for connection to the target application:

- One 85-pin PGA probe for TS68931 emulation
- One 48-pin DIP probe for TS68930 emulation

A 2K × 16 battery backed-up CMOS RAM board is also available for use with the EVAPSI to facilitate uploading/downloading of Program and Coefficient Memory.

The EVAPSI board is an excellent low-cost tool for software development, debugging, and emulation of the TS68930/68931.



EMULATION - LOGIC ANALYSIS FOR

TS68930: MCU Version
(1.28K Prog. ROM, 512 Coef.)
TS68931: MPU Version
(64K External Prog. memory)

MULTIPROCESSING

- up to 4 emulators board and 4 dedicated logic analysers

MULTIUSER:

- up to 4 Independent emulation/logic analysis station

USER-FRIENDLY USER INTERFACE

- Menu driven
- Symbolic debugging
- Resident Line assembler with full screen editor
- Controlled by standard terminals or IBM - PC hosted
- Direct link to PROM programmer
- Battery backup of configurations (breakpoints, mode,...)

EMULATION FEATURES

- Full speed (Tcyc = 160 ns)

EMULATION FEATURES (cont'd)

- 64k Program memory
- 4k External data memory, mapping on a word basis
- 20 simple breakpoints (break at ADRESS 1)
- 8 complex breakpoints (break after N ADR.1 followed by M ADR.2)
- Pseudo real time trace of internal registers without perturbing execution

LOGIC ANALYSER

- Realtime trace (2k depth, 95 bits)
- Synchronous on D.S.P. busses
- Asynchronous on D.S.P. system bus and on 15 external inputs.
- Triggering conditions:
  - on program adress in conjunction with complex conditions (N times Adr.1 followed by M times Adr.2)
  - on local data bus value
  - on external branch D.S.P. inputs configurations
  - on external inputs configurations
  - on start of mailbox exchange
- Before, after and Window triggering
- Time measurement function

FEATURES

- ☐ Analog Interface for use with TS68930/1 DSP
- ☐ Front End Circuit Designed To Implement High Speed Voice-Grade Modems up to 19200 bps
- ☐ Two-Channel DAC for Transmit and Echo-Cancelling Signals
- ☐ Programmable Attenuation of 22 dB in 2 Db steps
- ☐ Programmable Low-Pass, Band-Pass, and Band-Reject Filters
- ☐ Continuous-Time Anti-Aliasing and Smoothing Filters
- ☐ Programmable Gain Amplifier of 0 - 46.5 dB in 1.5 dB steps
- ☐ Carrier Level Detector with Programmable Threshold
- ☐ Independent Tx and Tx Clock Generators Using DPLLs
- ☐ Telephone Line Interface

DESCRIPTION

The EVM MAFE is an Analog Front End evaluation board for use with the TS68930/1 DSP and development tools. The EVM MAFE is based on the Modem Analog Front End chip set TS68950, 68951, 68952. The MAFE chip set interfaces directly to the DSP via its 8-bit bus using the TS68930/1 mailbox protocol.

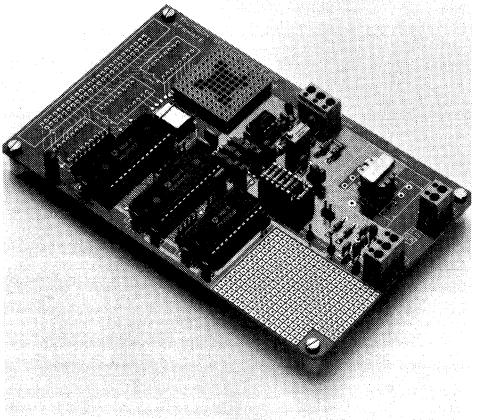


Figure 1. EVM MAFE

The EVM MAFE offers a very simple and straightforward means of interfacing the TS68930/1 to analog signals. It is especially well suited for development and debugging of modem applications designed to meet CCITT V.22, V.26, V.27, V.29, V.32 and V.33 recommendations as well as the Bell 212A, 208 and 209 standards.

PSIREPROM

PSI-REPROM MODULE

TS68930/31 SUPPORTS TOOLS

COMMUNICATIONS PRODUCTS

FEATURES

- ☐ Plug and function compatible to TS68930
- ☐ Include program and coefficient REPROM's
- ☐ Capacity of the program REPROM memory is 2K.32bit words as compared with 1.28K. 32bit for the TS68930 version
- ☐ Capacity of the coefficient REPROM memory is 512.16bit words
- ☐ Height of the module is 68mm above the DIL-48 socket on the application
- ☐ Vertical and horizontal (bended) versions
- ☐ Compatible with the use of a crystal on the input pins EXTAL and XTAL, or an external clock on the input pin EXTAL
- ☐ The 5-Volt supply for the module is either provided on the DIL-48 socket of the target application or by an external power supply
- ☐ The average power consumtion with all REPROMs on-board is typically 3 watts

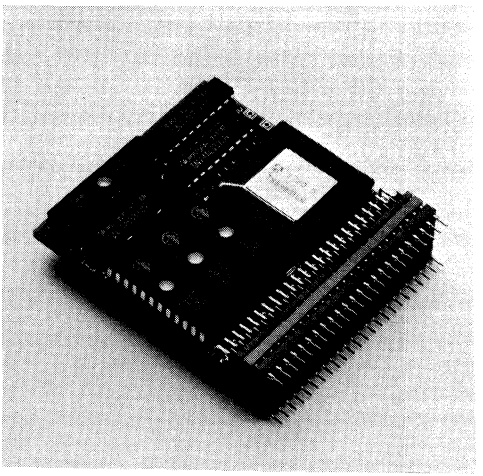


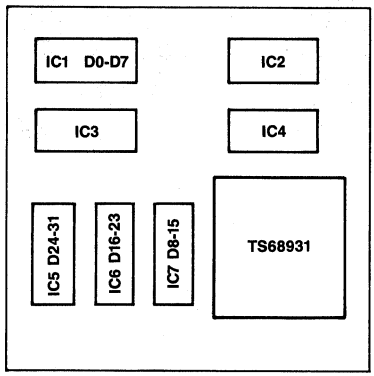
Figure 1. PSIREPROM-H V1R1

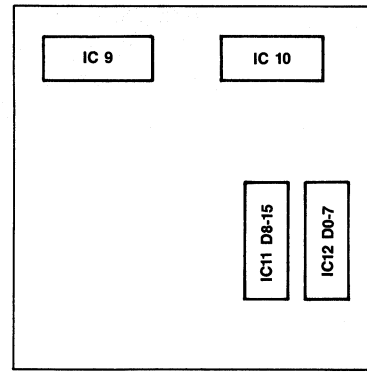
DESCRIPTION

The PSI-REPROM module (TS68930/31 support tools) is a high performance board which permits the replacement of the TS68930 (DSP ROM version) by the TS68931 (DSP ROMLESS version) including external coefficient and program REPROM memories.

BENEFITS

- Useful during prototyping
- Advantage of using the PSI REPROM module is to be able to develop and test software before ordering the final TS68930 masked-version
- Another advantage is to be able to develop low-quantity applications, eliminating masking costs
- Design to physically occupy the same board surface areas as the TS68930

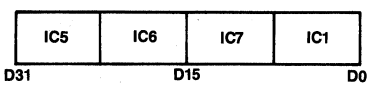




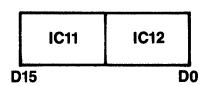
IC1-IC5-IC6-IC7 = REPROM PROGRAM

IC11-IC12 = REPROM COEFFICIENT

PROGRAM WORD



COEFFICIENT WORD



NOTE:
The REPROMs used are manufactured by CYPRESS, 2Kx8bit, reference CY7C291-35WC.
They are programmable on Data I/O equipment with the Code "EEAF". The programming is totally taken care of by the Thomson HDS PSI development system or the Thomson EVAPSI emulator board. The developed program will be loaded from the Data I/O by use of the monitor menu "PROG".

Figure 2. PSI-REPROM Module Layout

DATA SHEET

CMOS

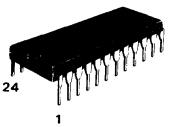
MODEM TRANSMIT ANALOG INTERFACE

The TS68950 is a transmit (Tx) analog front-end circuit designed to implement high speed voice-grade modems up to 19200 bps according to the CCITT V.22, V.26, V.27, V.29, V.32 and V.33 recommendations or the BELL 212A, 208 and 209 standards. This circuit is particularly suited to work with the TS68951 receive (Rx) analog front-end circuit, the TS68952 clock generator and the TS68930/31 digital signal processors (DSPs).

Main features

- Two-channel digital to analog converter (DAC) for Tx and echo-cancelling signals.
- 6th-order low-pass filter (switched-capacitor filter with output continuous-time smoothing cell).
- Programmable attenuation over a 22 dB range with 2 dB steps.
- Direct interface with MPU standard 8 bit bus.

CASE CB-68

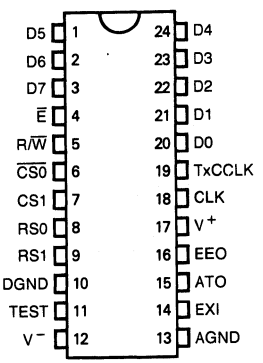


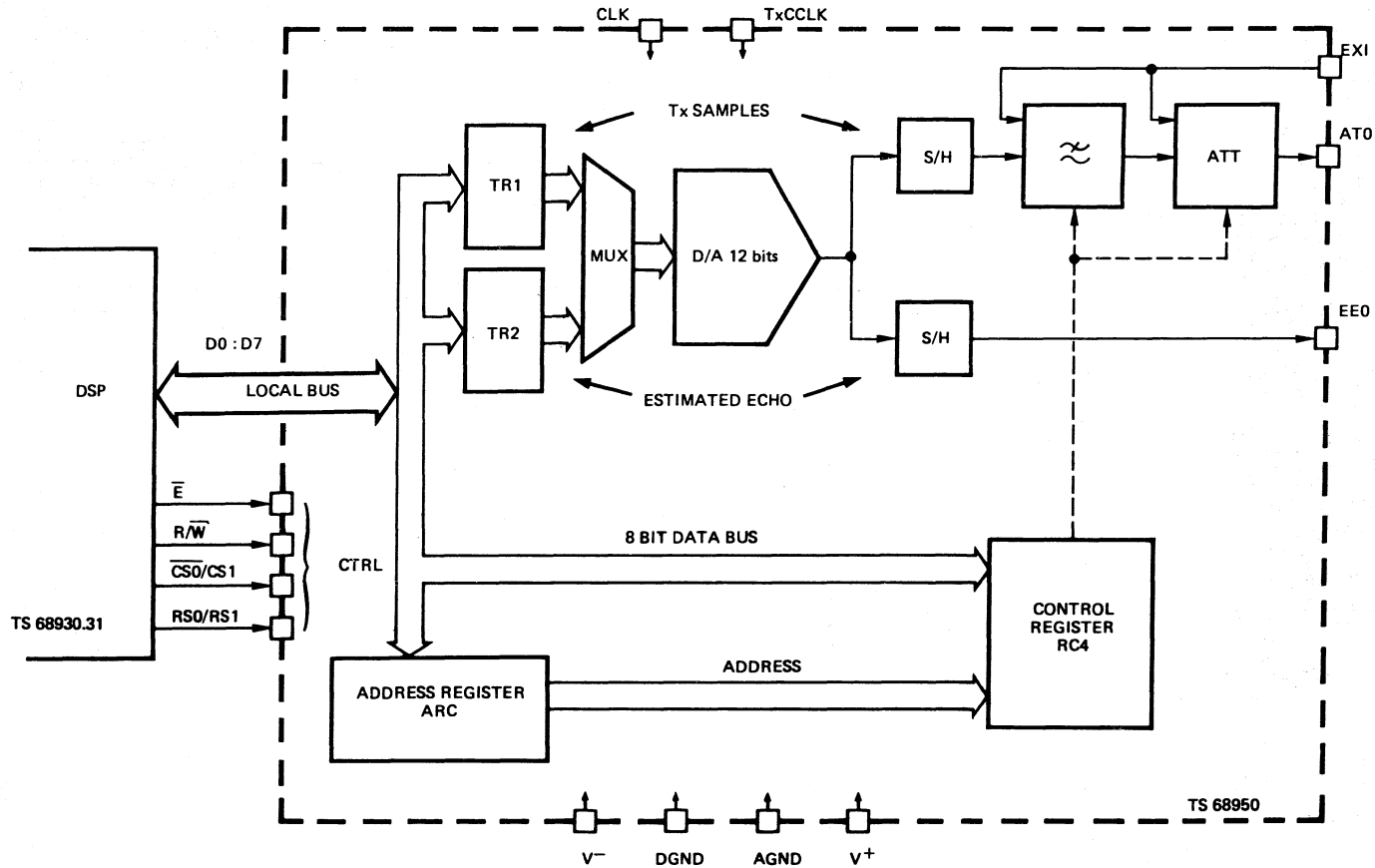
P SUFFIX
PLASTIC PACKAGE

ALSO AVAILABLE
C SUFFIX
CERAMIC PACKAGE

J SUFFIX
CERDIP PACKAGE

PIN ASSIGNMENT




CLK
TxCCLK
EXI
Tx SAMPLES
AT0
TR1
MUX
D/A 12 bits
S/H
ATT
TR2
S/H
EE0
D0 : D7
DSP
LOCAL BUS
ESTIMATED ECHO
E
R/W
CS0/CS1
RS0/RS1
CTRL
8 BIT DATA BUS
TS 68930.31
CONTROL REGISTER RC4
ADDRESS
ADDRESS REGISTER ARC
TS 68950
V−
DGND
AGND
V+

PIN DESCRIPTION

Name	No.	Function
D5-D7	1-3	8 bit data bus inputs giving access to Tx, estimated echo, control and address registers. (With pins 20-24).
$\overline{E}$	4	Enable input. Data are strobed on the positive transitions of this input.
R/$\overline{W}$	5	Read/write selection input. Internal registers can be written when R/$\overline{W}$ = 0. Read mode is not used.
$\overline{CS0}$-CS1	6-7	Chip select inputs. The chip set is selected when $\overline{CS0}$ = 0 and CS1 = 1.
RS0-RS1	8-9	Register select inputs. Used to select D/A input registers or control/address registers in the write mode.
DGND	10	Digital ground = 0 V. All digital signals are referenced to that pin.
TEST	11	Test input. Used to reduce testing time. That pin must be connected to DGND in all applications.
V−	12	Negative power supply voltage = −5 V ± 5%
AGND	13	Analog ground = 0 V. Reference point for analog signals.
EXI	14	Programmable analog input tied to filter or attenuator input according to the RC4 register content.
ATO	15	Analog transmit output.
EEO	16	Analog echo cancelling output.
V+	17	Positive power supply voltage: +5 V ± 5%.
CLK	18	1.44 MHz clock input. Used for internal sequencing.
TxCCLK	19	Transmit conversion clock input. Must be derived from CLK.
D0-D4	20-24	See pins No. 1-3.

FUNCTIONAL DESCRIPTION

The TS68950 is a transmit analog interface circuit dedicated to voice-grade MODEMs, telephony and speech applications. The TS68950, the TS68951 (receive analog front-end circuit) and the TS68952 (clock generator) constitute an analog front-end chip set useful for implementation of synchronous MODEMs operating on two or four wires according to the CCITT V.26, V.26 bis, V.27, V.27 bis, V.27 ter and V.29 recommendations or BELL 208 and 209 standards, or in two wires full-duplex according to CCITT V.22, V.22 bis or BELL 212A (split band) and CCITT V.26 ter and V.32 (echo cancelling).
By receiving digital samples from a DSP like the TS68930/31, the TS68950 delivers two analog signals: the transmitted (Tx) signal that will be sent on the line and the estimated echo signal that will be subtracted from the received (Rx) signal on the TS68951 Rx chip.
The digital Tx and estimated echo samples are converted to analog during the low state and the high state of the TxCCLK clock, respectively.

MAIN FUNCTIONS (See block diagram)

- 12 bit digital to analog converter multiplexed on two channels.
- Tx signal sample and hold running with Tx sampling frequency TxCCLK.
- Tx low-pass filter with continuous-time smoothing.
- Programmable attenuator from 0 to −22 dB with 2 dB steps.
- Estimated echo sample and hold running with Tx sampling frequency TxCCLK.

DSP INTERFACE SIGNALS

The TS68950 interfaces to the signal processor via an 8 bit data bus (only used in writing mode), two chip select lines, two register select lines, a read/write line and an enable line.

Data bus (D0-D7) - The write only data lines allow the transfer of data from the DSP to the TS68950. Input buffers are high-impedance devices.

Enable ($\overline{E}$) - The enable pulse ($\overline{E}$) is the basic timing signal that is supplied to the TS68950. All the other signals are referenced to the leading and trailing edges of the $\overline{E}$ pulse.

Read/Write (R/$\overline{W}$) - This signal is generated by the DSP to control the direction of data transfers on the data bus. A low level state on the TS68950 read/write line enables the input buffers and data is transferred from the DSP to the TS68950 on the $\overline{E}$ signal if the circuit has been selected. The device is unselected when a high level signal is applied to the R/$\overline{W}$ pin.

Chip Select ($\overline{CS0}$, CS1) - These two input signals are used to select the chip. $\overline{CS0}$ must be low and CS1 must be high for selection of the device. Data transfers are then performed under the control of the enable and R/$\overline{W}$ signals. The chip select lines must be stable for the duration of the $\overline{E}$ pulse.

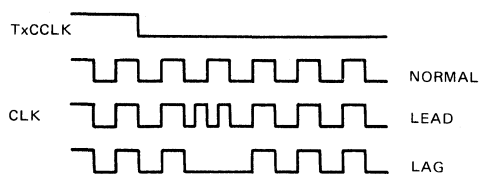
Register Select (RS0, RS1) - The two register select lines are used to access the different registers inside the chip. For instance these two lines are used in conjunction with the internal control register ARC to select a particular register RC4. The register select lines must be stable when the $\overline{E}$ signal is low.

CLOCK INTERFACE BETWEEN TS68950 AND TS68952

The TS68950 receives two clock lines from the Clock Generator TS68952.

Master clock sequencing (CLK)

The typical frequency is 1.44 MHz but the recurrence frequency must be an exact multiple of the terminal clock frequency. The Tx DPLL included in the clock generator circuit (TS68952) operates by adding or subtracting pulses to a 2.88 MHz internal clock. This corresponds to phase leads or phase lags of about 350 ns duration. To ensure correct device operation, clock synchronization must be done immediately after the negative-going transition of TxCCLK clock.



Transmit Conversion Clock (TxCCLK)

The conversion clock TxCCLK must be derived from the master clock CLK. Three nominal values are possible: 9.6 kHz, 8 kHz and 7.2 kHz. 9.6 kHz is the highest allowable frequency. To run properly the TxCCLK clock must be a submultiple of CLK/5:

TxCCLK x 5 x N = CLK (with N integer)

This is ensured when using the TS68952 clock generator.
The sampling clock of the switched capacitor filter section is obtained by dividing the CLK frequency by five and performing internal synchronization on the leading edges of TxCCLK.
The Tx samples are converted from digital to analog during the low state of TxCCLK. The estimated echo samples are converted during the high state of TxCCLK.

INTERNAL CONTROLS

Power-on

The chip contains internal power-on reset logic to initialize the RC4 control register in order to avoid undesirable signal transmission on the telephone line.

Internal addressing

RS0	RS1	Access	320 ns cycle number
0	0	TR1 transmitted sample register	2
0	1	TR2 estimated echo sample register	2
1	0	ARC address register	1
1	1	RC4 control register (if addressed by ARC)	1

Sample registers (TR1 and TR2)

TR1 is the transmitted sample register and TR2 the estimated echo sample register. TR1 and TR2 store two's complement 12 bit data (DAC0 to DAC11). As indicated below, writing each sample requires two cycles.

	D7	D6	D5	D4	D3	D2	D1	D0
First cycle	DAC 3	DAC 2	DAC 1	DAC 0	X	X	X	X
Second cycle	DAC 11	DAC 10	DAC 9	DAC 8	DAC 7	DAC 6	DAC 5	DAC 4

An internal flip-flop is used to select the first or the second byte. It advances one count on the positive-going edge of the $\overline{E}$ pulse when the sample registers are selected ($\overline{CS0}$ = 0, CS1 = 1 and RS0 = 0). When the sample registers are disabled, the latch is reset on any $\overline{E}$ positive-going edge. Both TR1 and TR2 registers are sampled by the DAC on the falling edge of TxCCLK. Therefore their contents must remain stable during this edge.

Control register (RC4)

The RC4 control register has two different functions. Its four most significant bits give the transmit attenuator gain following the table below.

D7	D6	D5	D4	D3	D2	D1	D0	RC4 REGISTER
ATT 4	ATT 3	ATT 2	ATT 1	–	EM2	EM1	–	Attenuation (dB)
0	0	0	0					0
0	0	0	1					2
0	0	1	0					4
0	0	1	1					6
0	1	0	0					8
0	1	0	1					10
0	1	1	0					12
0	1	1	1					14
1	0	0	0					16
1	0	0	1					18
1	0	1	0					20
1	0	1	1					22
1	1	0	0					Infinite
1	1	0	1					Infinite
1	1	1	0					Infinite
1	1	1	1					Infinite

Depending on the EM1 and EM2 states in the RC4 register, the programmable analog input (EXI) can be connected to the filter input or to the transmit attenuator input.

D7	D6	D5	D4	D3	D2	D1	D0	RC4 REGISTER
ATT 4	ATT 3	ATT 2	ATT 1	–	EM2	EM1	–	EXI INPUT
					0	0		disabled
					0	1		transmit filter input
					1	0		transmit attenuator input
					1	1		disabled

Following power-up, all RC4 bits are preset at one, EXI input is disabled and the transmit signal is cancelled.

D0 and D3 bits are not used in the RC4 register.

Address register (ARC)

The address register stores 3 bits (D5, D6 and D7). Among the 8 possible addresses, only one is used inside the TS68950 (RC4 address).

	D7	D6	D5	D4	D3	D2	D1	D0
RC 4	0	1	1	X	X	X	X	X

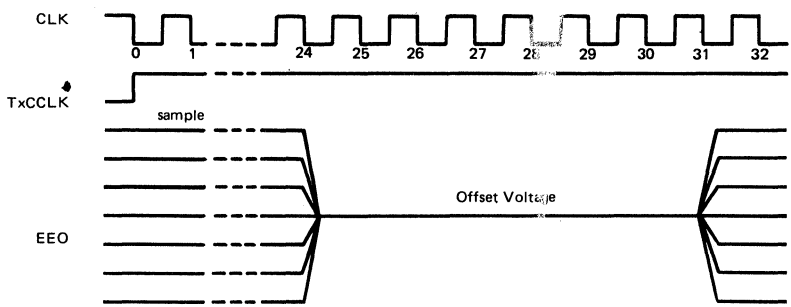
X: don't care

The address of the ARC register is automatically increased by one each time the control register is accessed. This allows indirect or cyclical addressing to RC4.

EEO OUTPUT WAVEFORM

The EEO output is not valid during S/H sampling. The output presents at this time the S/H offset voltage.
This offset voltage appears at the 24th CLK period after rise transition of TxCCLK and disappears at the 31th.

Waveform



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
DGND digital ground to AGND analog ground		− 0.3 to + 0.3	V
V^+ supply voltage to DGND or AGND ground		− 0.3 to + 7	V
V^- supply voltage to DGND or AGND ground		− 7 to + 0.3	V
Voltage at any digital input or output	V_I	DGND − 0.3 to V^+ + 0.3	V
Voltage at any analog input or output	V_{in}	V^- − 0.3 to V^+ + 0.3	V
Analog output current	I_{out}	− 10 to + 10	mA
Power dissipation	P_{tot}	500	mW
Operating temperature range	t_{amb}	0 to + 70	°C
Storage temperature range	t_{stot}	− 65 to + 150	°C
Pin temperature (soldering 10 s.)	t_{sold}	+ 260	°C

Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. Standard CMOS handling procedures should be employed to avoid possible damage to device.

ELECTRICAL OPERATING CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit
Positive Supply Voltage	V^+	4.75	5	5.25	V
Negative Supply Voltage	V^-	− 5.25	− 5.0	− 4.75	V
V^+ Operating current	I^+	–		15	mA
V^- Operating current	I^-	− 15		–	mA

D.C. AND OPERATING CHARACTERISTICS

Unless otherwise noted, electrical characteristics are specified over the operating range. Typical values are given for $V^+ = +5$ V, $V^- = -5$ V and $t_{amb} = 25°C$.

DIGITAL INTERFACE

Parameter	Symbol	Min	Typ	Max	Unit
Input low level voltage	V_{IL}			0.8	V
Input high level voltage	V_{IH}	2.2			V
Input low level current $DGND < V_I < V_{ILmax}$	I_{IL}	− 10		10	μA
Input high level current $V_{IHmin} < V_I < V^+$	I_{IH}	− 10		10	μA

ANALOG INTERFACE, EXI PROGRAMMABLE INPUT

Parameter	Symbol	Min	Typ	Max	Unit
Input voltage swing	V_{in}	− 2.5		+ 2.5	V
Input current (Input Tx filter selected)	I_{in}	− 10		+ 10	μA
Input capacitance (Input ATT selected) f < 50 kHz f > 50 kHz	C_{in}			 50 20	 pF pF
Input resistance (Input ATT selected)	R_{in}	20			kΩ

ANALOG INTERFACE, ATO TRANSMIT OUTPUT

Parameter	Symbol	Min	Typ	Max	Unit
Output DC offset	V_{os}	− 250		+ 250	mV
Load capacitance	C_L			50	pF
Load resistance	R_L	1200			Ω
Output voltage swing $R_L > 1200\ \Omega$ and $C_L < 50$ pF	V_{out}	− 2.5		+ 2.5	V
Output resistance	R_{out}			5	Ω

ANALOG INTERFACE, EEO ESTIMATED ECHO OUTPUT

Parameter	Symbol	Min	Typ	Max	Unit
Output DC offset	V_{os}	— 100		+ 100	mV
Load capacitance	C_L			50	pF
Load resistance	R_L	10			kΩ
Output voltage swing $R_L > 10$ kΩ and $C_L < 50$ pF	V_{out}	— 2.5		+ 2.5	V
Output resistance	R_{out}	350	500	650	Ω

DAC TRANSFER CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit
Converter resolution			12		Bit
Nominal output peak to peak amplitude	V_{out} (max)		5.0		V
Least significant bit amplitude	LSB		1.2		mV
Integral linearity error		— 1		+ 1	LSB
Differential linearity error		— 0.7		+ 0.7	LSB

TRANSMIT FILTER TRANSFER CHARACTERISTICS (see annexe 1)

Parameter	Symbol	Min	Typ	Max	Unit
Absolute passband gain at 1 kHz	G_{AR}		0		dB
Gain relative to gain at 1 kHz without sin x/x correction of DAC sampling	G_{RR}				
Below 3100 Hz		— 0.5		0.2	dB
3200 Hz		— 3			dB
4000 Hz				— 36	dB
5000 Hz to 12000 Hz				— 46	dB
12000 Hz and above				— 50	dB
Absolute delay 600 Hz to 3000 Hz	D_{AR}	160		680	μs

ATTENUATOR TRANSFER CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit
Absolute gain at 0 dB nominal value	A_{TT}		0		dB
Attenuation relative to nominal value	R_{AT}	— 5.0		+ 0.5	dB
Maximum attenuation	B_{AT}	40			dB

GENERAL TRANSFER CHARACTERISTICS (from DATA BUS to ATO)

Parameter	Symbol	Min	Typ	Max	Unit
ATO absolute gain at 1 kHz	G_{AX}	— 0.5	0	+ 0.5	dB
ATO psophometric noise				100	μV
ATO positive power supply rejection ratio. V_{ac} = 200 mVpp f = 1 kHz			40		dB
ATO negative power supply rejection ratio. V_{ac} = 200 mVpp f = 1 kHz			40		dB
Signal to harmonic distorsion ratio (psophometric band)		60			dB

GENERAL TRANSFER CHARACTERISTICS (from DATA BUS to EEO)

Parameter	Symbol	Min	Typ	Max	Unit
EEO absolute gain at 1 kHz	G_{AX}	— 0.5	0	+ 0.5	dB
EEO psophometric noise				100	μV
EEO positive power supply rejection ratio. V_{ac} = 200 mVpp f = 1 kHz			40		dB
EEO negative power supply rejection ratio. V_{ac} = 200 mVpp f = 1 kHz			40		dB

BUS TIMING CHARACTERISTICS (See Notes 1 and 2)

Ident number	Characteristic	Symbol	Min	Max	Unit
1	Cycle time	t_{cyc}	320		ns
2	Pulse width, $\overline{E}$ low level	t_{WEL}	180		ns
3	Pulse width, $\overline{E}$ high level	t_{WEH}	100		ns
4	Clock rise and fall time	t_r, t_f		20	ns
5	Control signal hold time	t_{HCE}	10		ns
6	Control signal set-up time	t_{SCE}	40		ns
7	Input data set-up time	t_{SDI}	120		ns
8	Input data hold time	t_{HDI}	10		ns

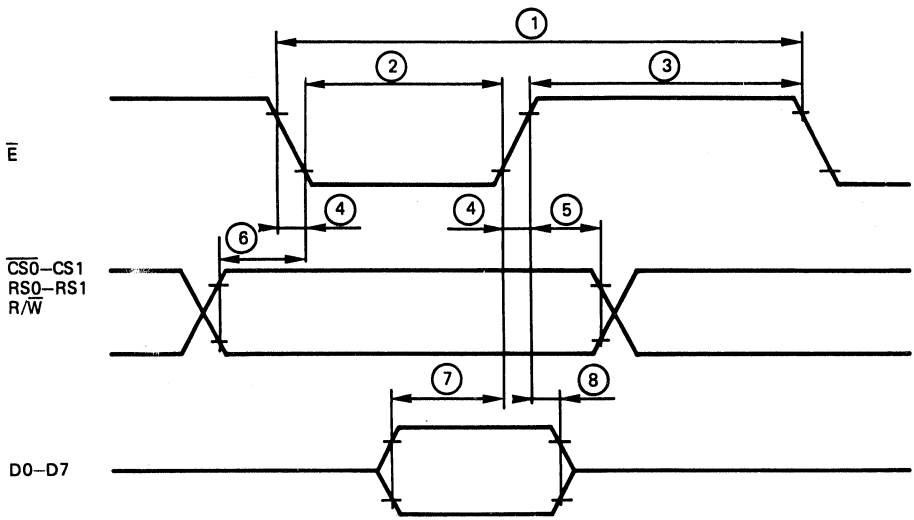


FIGURE 1 – BUS TIMING

Notes :

1. Voltage levels shown are VL < 0.4 V, VH > 2.4 V, unless otherwise specified.
2. Measurement points shown are 0.8 V and 2.2 V, unless otherwise specified.

CLOCK TIMING CHARACTERISTICS

Ident number	Characteristic	Symbol	Min	Typ	Max	Unit
1	CLK clock period	P_C		695		ns
2	CLK phase leading clock period	P_{CL}		348		ns
3	CLK low level width	t_{WCL}	150			ns
4	CLK high level width	t_{WCH}	150			ns
5	CLK rise and fall time	t_{RC}, t_{FC}			100	ns
6	TxCCLK rise and fall time	t_{RT}, t_{FT}			100	ns
7	TxCCLK delay time	t_{DC}	20		130	ns

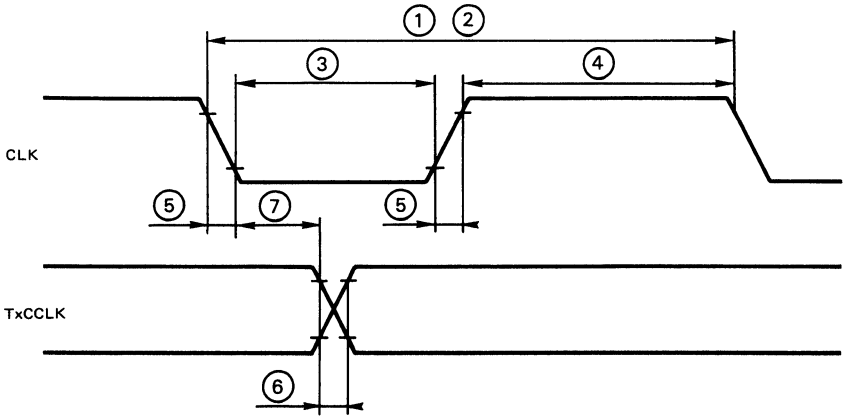
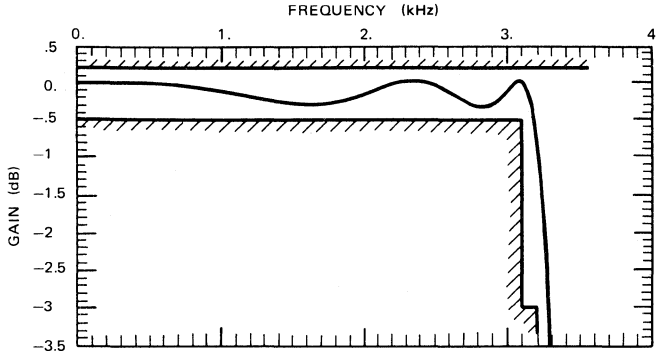
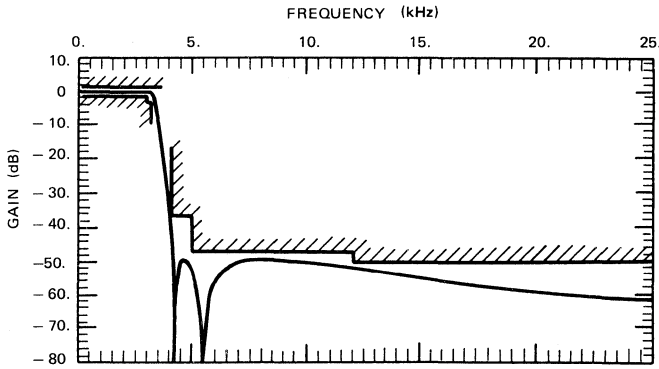


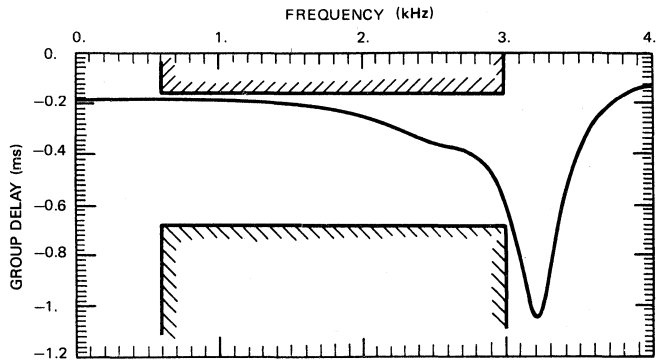
FIGURE 2 – CLOCK TIMING



TRANSMIT LOW-PASS FILTER TYPICAL RESPONSE AND LIMITS CHART

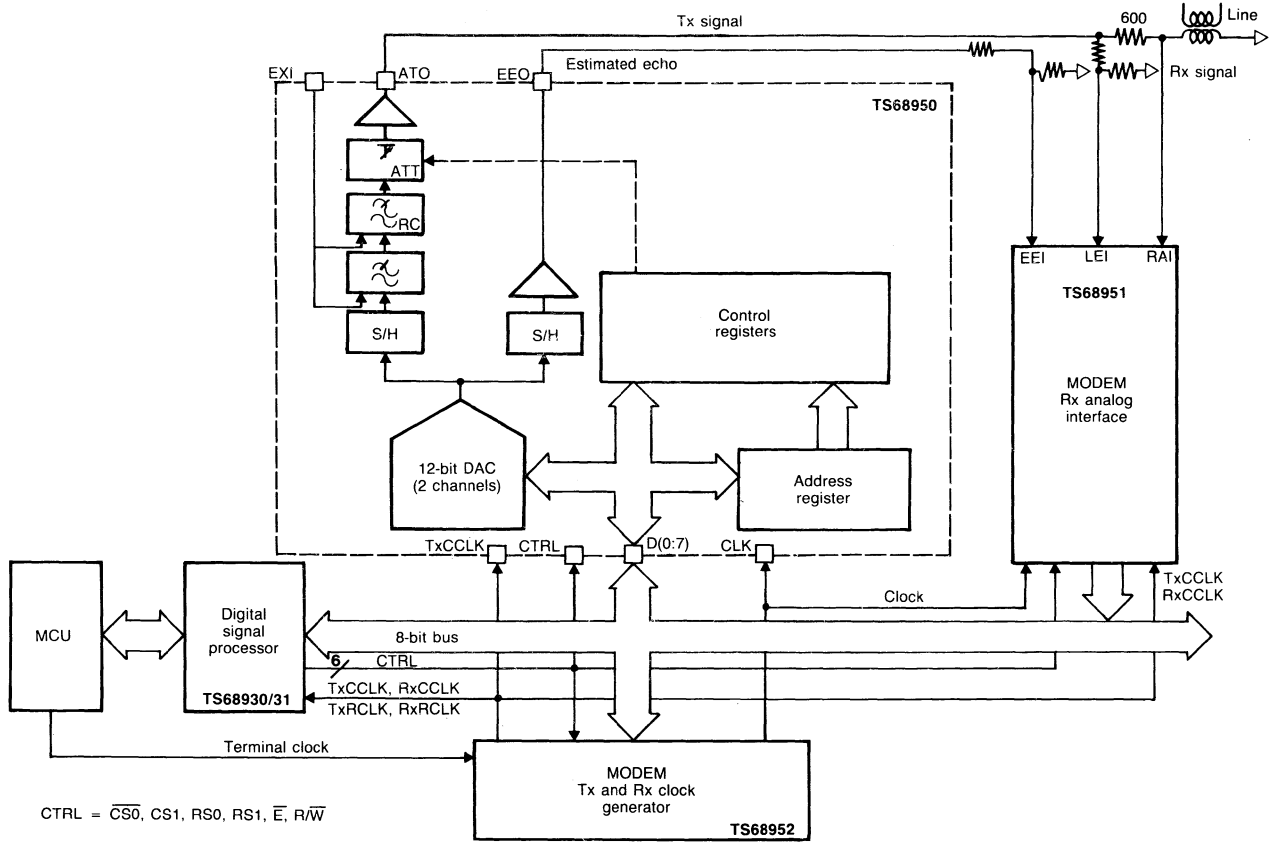


TRANSMIT LOW-PASS FILTER TYPICAL RESPONSE AND LIMITS CHART



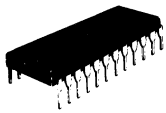
TRANSMIT LOW-PASS FILTER TYPICAL GROUP DELAY AND LIMITS CHART

APPENDIX 1

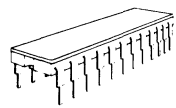

Tx signal
600
Line
Rx signal
Estimated echo
EXI
ATO
EEO
TS68950
ATT
RC
S/H
S/H
Control registers
12-bit DAC (2 channels)
Address register
TxCCLK
CTRL
D(0:7)
CLK
EEI
LEI
RAI
TS68951
MODEM Rx analog interface
TxCCLK
RxCCLK
Clock
MCU
Digital signal processor
TS68930/31
8-bit bus
6
CTRL
TxCCLK, RxCCLK
TxRCLK, RxRCLK
Terminal clock
MODEM Tx and Rx clock generator
TS68952
CTRL = CS0, CS1, RS0, RS1, E, R/W

PHYSICAL DIMENSIONS

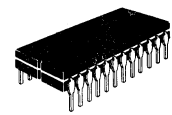
CB-68



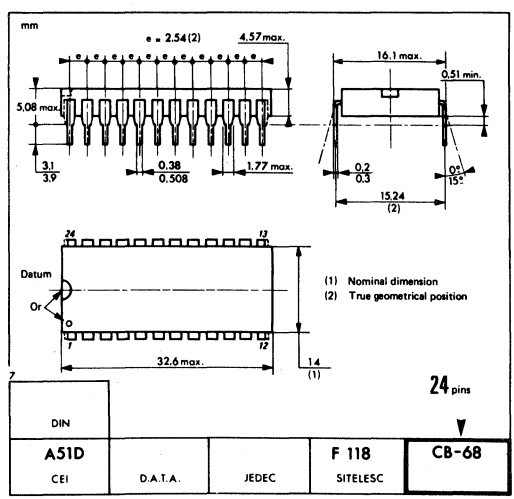
P SUFFIX
PLASTIC PACKAGE



ALSO AVAILABLE
C SUFFIX
CERAMIC PACKAGE



J SUFFIX
CERDIP PACKAGE



THOMSON COMPONENTS MOSTEK

TS68951

MODEM RECEIVE ANALOG INTERFACE

COMMUNICATIONS PRODUCTS

DATA SHEET

CMOS

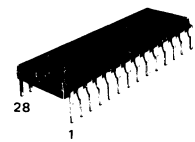
MODEM RECEIVE ANALOG INTERFACE

The TS68951 is the receive section of a MODEM analog front-end. The MODEM consists of TS68950/51/52 analog front-end chip sets and TS68930/31 digital signal processor; it is able to run voice-grade applications, which conforms to CCITT V.22/BIS, V.26/TER, V.27, V.29, V.32 and V.33 recommendations as well as BELL 212A, 208 and 209 standards.

Main features

- Programmable band-pass filter.
- Back channel rejection filter (selected by programming)
- Reconstruction filter (selected by programming)
- Continuous-time anti-aliasing and smoothing filters
- Programmable gain amplifier (from 0 dB to 46.5 dB with 1.5 dB steps)
- 12 bit A/D converter with asynchronous multiplexing of two plesiochronous channels (one channel for echo cancellation)
- Carrier level detector with programmable threshold.
- Digital interface: 8 bit bi-directional data bus, 6 bit control bus.
- Dual power supplies +5 V and −5 V
- Designed to operate with TS68950 transmit unit and TS68952 clock generator.

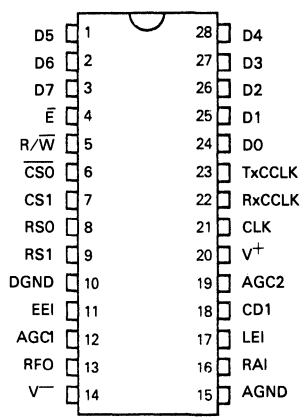
CASE CB-132



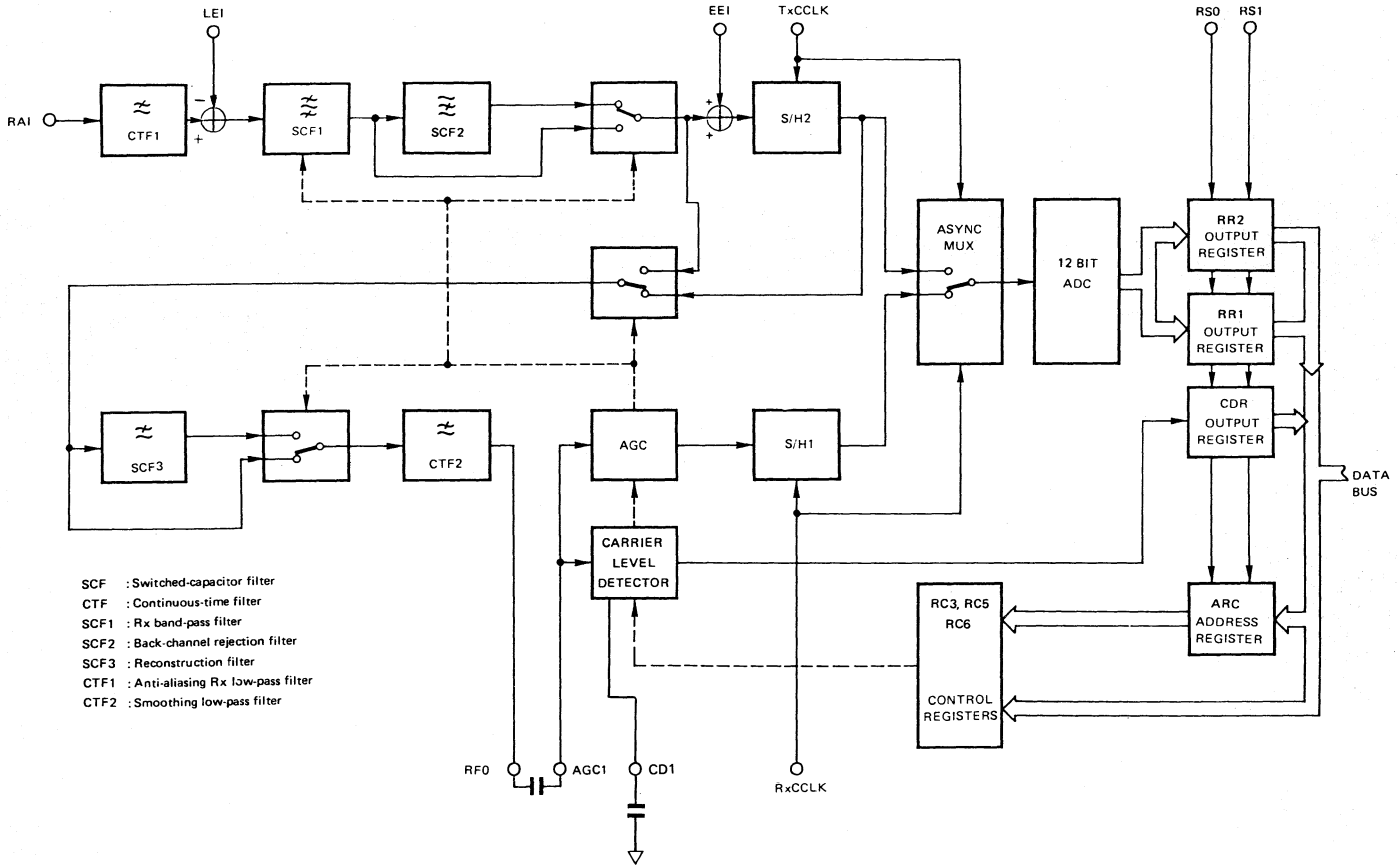
P SUFFIX
PLASTIC PACKAGE

ALSO AVAILABLE
C SUFFIX
CERAMIC PACKAGE
J SUFFIX
CERDIP PACKAGE

PIN ASSIGNMENT



BLOCK DIAGRAM



PIN DESCRIPTION

Name	No.	Description
D5-D7	1-3	Data bus
$\overline{E}$	4	Enable input. Enables selection inputs. Active on a low level for read operation. Active on a positive edge for write operation.
R/$\overline{W}$	5	Read/write Selection input. Read operation is selected on a high level. Write operation is selected on a low level.
$\overline{CS0}$-CS1	6-7	Chip select inputs. The chip set is selected when $\overline{CS0} = 0$ and CS1 = 1.
RS0-RS1	8-9	Register select inputs. Select the register involved in a read or write operation.
DGND	10	Digital ground. All digital signals are referenced to this pin.
EEI	11	Estimated echo input. When operating in echo cancelling mode, this signal is added to the reception band-pass filter output.
AGC1	12	Analog input of the automatic gain control amplifier and of the carrier level detector.
RFO	13	Reception filter analog output. Designed to be connected to AGC1 input through a 1 μF non polarised capacitor.
V$^-$	14	Negative power supply. $V^- = -5\ V \pm 5\%$.
AGND	15	Analog ground. All analog signals are referenced to this pin.
RAI	16	Receive analog input. Analog input tied to the transmission line.
LEI	17	Local echo input. Analog input subtracted from the receive anti-aliasing filter output.
CD1	18	This pin must be connected to the analog ground through a 1 μF non polarised capacitor, in order to cancel the offset voltage of the carrier level detector amplifier.
AGC2	19	This pin must be connected to the analog ground through a 1 μF non polarised capacitor, in order to cancel the offset voltage of the AGC amplifier.
V+	20	Positive power supply $V^+ = +5\ V \pm 5\%$.
CLK	21	Master clock input. Nominal frequency 1.44 MHz.
RxCCLK	22	Receive conversion clock.
TxCCLK	23	Transmit conversion clock.
D0-D4	24-28	Data bus.

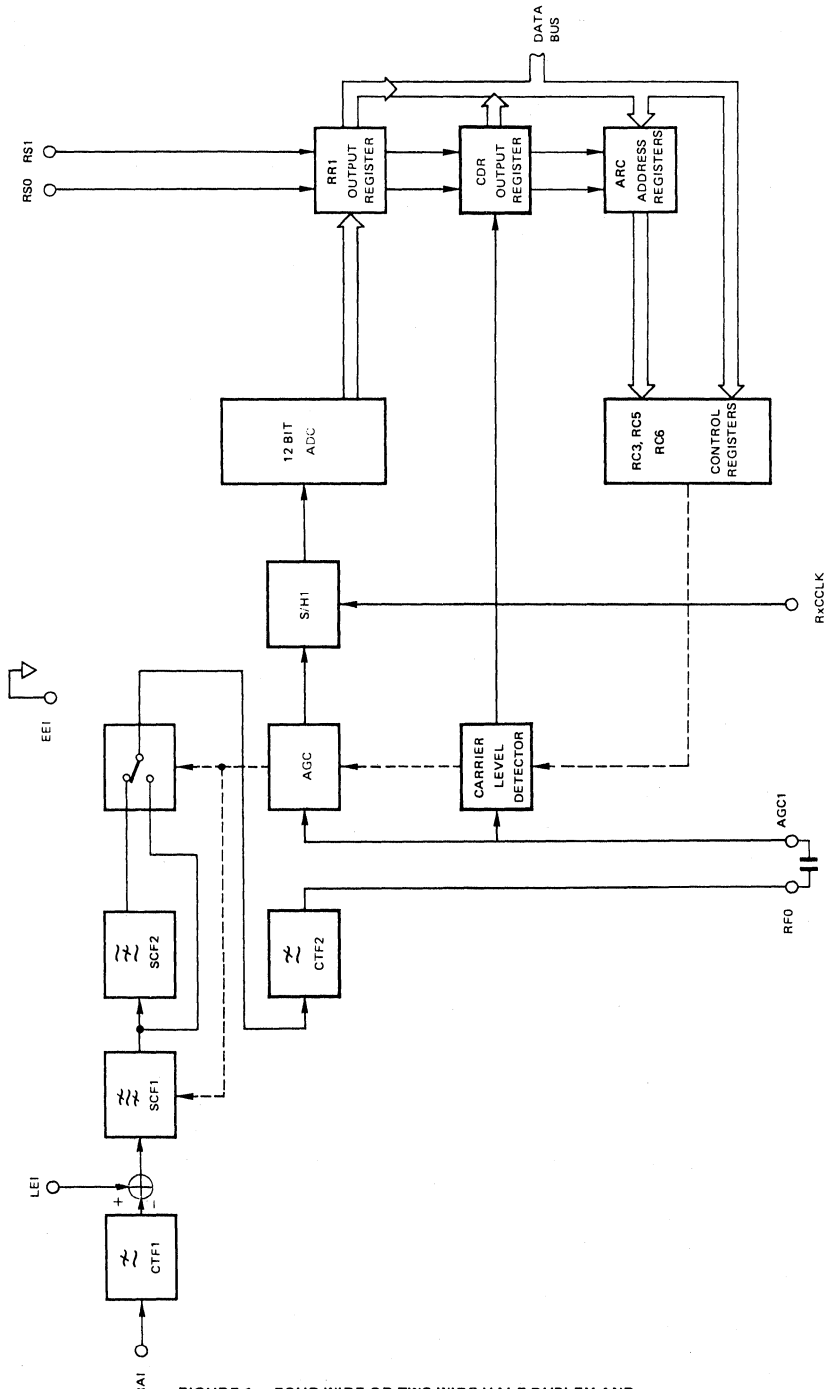


FIGURE 1 – FOUR-WIRE OR TWO-WIRE HALF DUPLEX AND TWO-WIRE BAND-SPLIT ANALOG SIGNAL TREATMENT

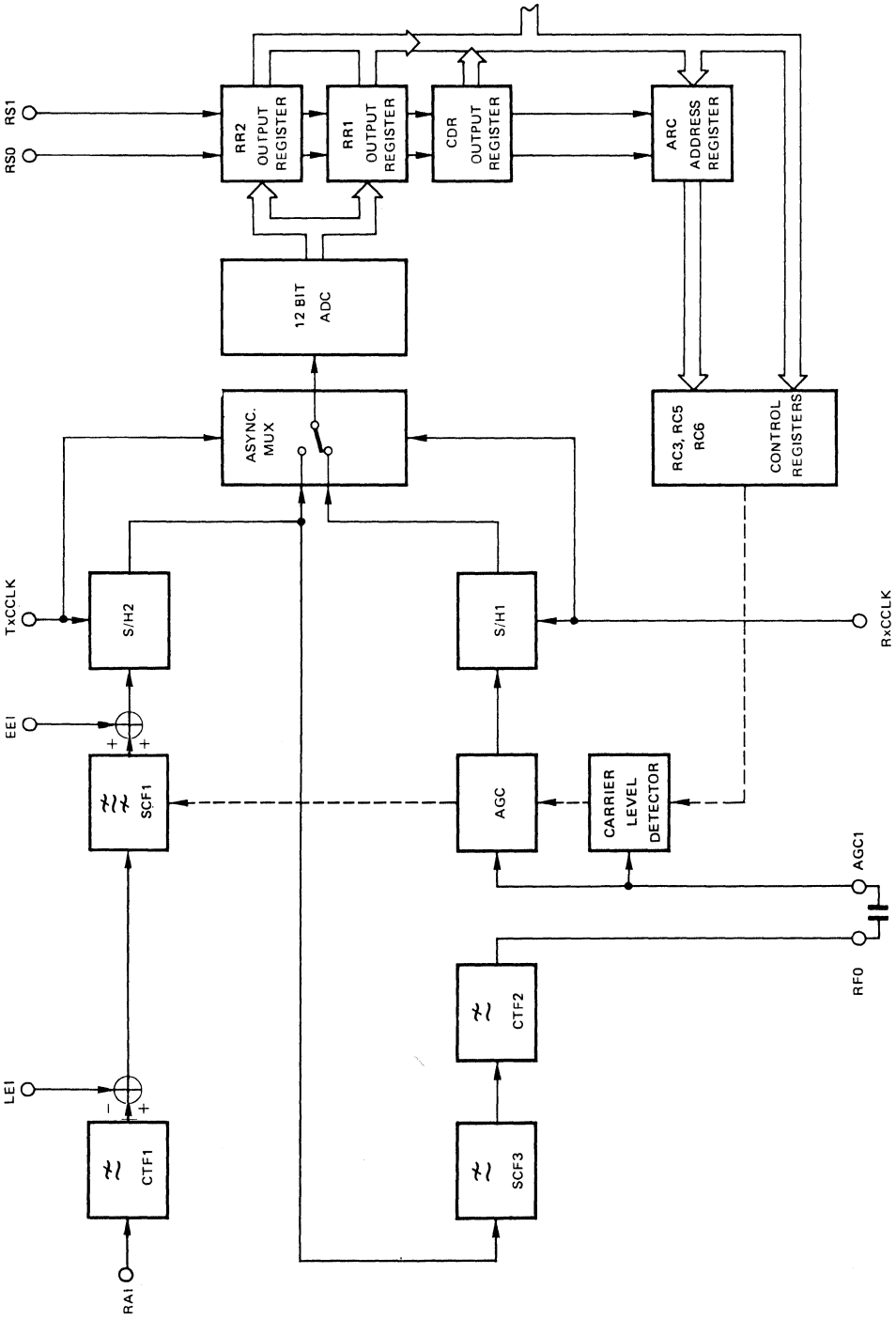


FIGURE 2 – TWO-WIRE ECHO CANCELLING ANALOG SIGNAL TREATMENT

FUNCTIONAL DESCRIPTION

The TS68951 is a receive analog interface for voice-grade MODEM. It is able to perform the receive interface function for three types of synchronous MODEM:

- Four-wire or two-wire half duplex MODEM.
- Two-wire full duplex band-split MODEM.
- Two-wire full duplex echo cancelling MODEM.

Four-wire or two-wire half duplex MODEM and two-wire band-split MODEM

In these modes of operation, EEI input must be tied to the analog ground. The analog signal treatment of receive input is shown in figure 1.
Programming requirements:

- Band-pass filter cut-off frequencies.
- Back channel rejection filter (presence or absence according to the application).
- SCF1 or SCF2 output as input of CTF2.
- AGC gain.
- Carrier level detector threshold.

The receive samples are coded at RxCCLK rate and can be read from receive register (RR1).

Two-wire echo cancelling MODEM

This mode of operation uses the full capabilities of the TS68951. The analog treatment of receive input is shown in figure 2. The echo cancelling operation is achieved by means of subtraction of the LEI signal from the output of CTF1 duplexer and addition of the EEI signal to the output of SC1.
After the local echo reduction by the duplexer the resultant signal consists of the receive signal plus the echo signal generated by the transmission line mismatch: this undesirable signal is then cancelled at the output of the Rx band-pass filter.
Programming requirements:

- Band-pass filter cut-off frequencies.
- SCF1 output as input of S/H2.
- Output of S/H2 as input of SCF3 and output of SCF3 as input of CTF2.
- AGC gain.
- Carrier level detector threshold.

Residual signal samples from S/H2 output are coded at TxCCLK rate and can be read from receive register 2 (RR2), hence the signal processor may correlate them with the transmit samples to update the coefficients of the filter that generates the estimated echo.
The receive signal samples are coded at RxCCLK rate and can be read from receive register 1 (RR1).

FUNCTIONAL SPECIFICATIONS

Bus and Registers Control

For any operation involving bus and registers, the chip select bits $\overline{CS0}$ and CS1 must be valid ($\overline{CS0}$ =0 and CS1 = 1).
The seven internal registers are divided in four write only registers and three read-only registers.

Write operation

There are three control registers (RC3, RC5, RC6) and one address register (ARC) which can be written; but only ARC can be directly addressed.
The control registers are indirectly addressed by the word contained in ARC according to table 1.

Addressed control register	Word contained in ARC							
	D7	D6	D5	D4	D3	D2	D1	D0
RC3	0	1	0	X	X	X	X	X
RC5	1	0	0	X	X	X	X	X
RC6	1	0	1	X	X	X	X	X

X: don't care

TABLE 1

When a write operation is selected (refer to table 3) the data present on the bus are strobed on a positive edge of $\overline{E}$ and the content of ARC is incremented.

Note: Addresses of RC3 and RC5 are separated by two increments.

Read operation

There are two 12 bit receive registers (RR1, RR2) and a 1 bit carrier detector register (CDR).

RR2 contains the coded samples of the residual signal and RR1 the coded samples of the receive signal.

The active bit of CDR is D7: D0 to D6 are forced to 0.

When the RMS value of CTF2 output is greater than the programmed threshold, bit 7 of CDR is set. The nominal response time of the carrier detector to a signal settlement or removal is 1.78 ms.

When a read operation is selected (refer to table 3) the data are sent to the bus on a low level of $\overline{E}$; a high level on $\overline{E}$ sets the output bus drivers in a high impedance state.

As the bus has only 8 bits, the content of RR1 or RR2 must be read in two cycles. The four less significant bits are transferred in the first cycle and the eight most significant bits are transferred in the second cycle according to the format, table 2.

	D7	D6	D5	D4	D3	D2	D1	D0
First cycle	RRx3	RRx2	RRx1	RRx0	0	0	0	0
Second cycle	RRx11	RRx10	RRx9	RRx8	RRx7	RRx6	RRx5	RRx4

TABLE 2

An internal latch selects the first or the second byte and is automatically incremented on a positive edge of $\overline{E}$ when one of the receive registers is addressed. This latch is not reset at power-on, so it needs to be reset before the first read operation: reset occurs on any positive edge of $\overline{E}$ for any operation, provided none of the receive registers is addressed; the first byte is selected when reset.

R/$\overline{W}$	RS0	RS1	Operation
0	1	1	Write control register addressed by ARC
0	1	0	Write address register (ARC)
1	0	1	Read receive register 2 (RR2) (Residual signal sample)
1	0	0	Read receive register 1 (RR1) (Receive signal sample)
1	1	0	Read carrier detector register (CDR)

TABLE 3

RR1 and RR2 output code:
The output code is a 2's complement delivering values from — 2048 up to + 2047. Since the converter codes voltage between $-V_{ref}$ and $+V_{ref}$, the theoretical decision voltage corresponding to code C can be computed as follows:

$$V_c = \frac{2C+1}{4095} V_{ref}$$

where V_{ref} is the reference voltage of the A/D converter, V_{ref} nominal value is 2.5 V and C is the algebraic value of code C.

Example:
Assume the output code is the hexadecimal value $8B1; the algebraic value of this code C = — 1871 therefore V_c = — 2.283 V.

CONTROL REGISTERS DESCRIPTION

Power-on
The control registers are not initialized at power-on; they must be initialized from program before reading any word from the output registers.

Register RC3
The content of RC3 sets the — 3 dB cut-off frequencies of SCF1 receive band-pass filter, determines the presence or the absence of SCF2 back channel rejection filter and of SCF3 reconstruction filter, and selects receive signal path to the second filtering section ; without echo-cancelling the output of SCF1 or SCF2 is selected ; with echo-cancelling the output of S/H2 is selected.

The band-pass filter consists of a 5th-order elliptic low-pass filter and of a 2nd order high-pass filter whose cut-off frequencies can be programmed by (LP1, LP2) and (HP1, HP2) respectively, (refer table 4).

The rejection filter is present when REJ bit is high.

The reconstruction filter is present when REC bit is high.

S/H2 output is selected when S/A bit is high.

D7 HP2	D6 HP1	D5 LP2	D4 LP1	D3 REJ	D2 S/A	D1 REC	D0	RC3 REGISTER		
								LOW-PASS FILTER		
								Sampling frequency (kHz)	— 3 dB Cut-off freq. (Hz)	
		0 0 1 1	0 1 0 1				X X X X	72 144 288 288	800 1600 3200 3200	
								HIGH-PASS FILTER		
								Sampling frequency (kHz)	— 3 dB Cut-off freq. (Hz)	
0 1 1	X 0 1			0 0 0			X X X	36 72 144	250 500 1600	
								HIGH-PASS AND REJECTION FILTER		
								Sampling freq. (kHz)	— 3 dB Cut-off freq. (Hz)	Rejected band (Hz)
1 1	0 1			1 1			X X	72 144	800 2200	370-470 800-1600
								S/H2 SELECTION		
					0 1		X X	Deselected Selected		
								RECONSTRUCTION FILTER SELECTION		
						0 1	X X	Deselected Selected	(Sampling frequency = 288kHz)	

TABLE 4

X: don't care

Register RC5

The content of RC5 sets the gain of the AGC amplifier between 0 dB and 46.5 dB with 1.5 dB steps.

Note: The AGC loop control is performed by the signal processor.

D7	D6	D5	D4	D3	D2	D1	D0	RC5
								AGC gain (dB)
0	0	0	0	0	X	X	X	0
0	0	0	0	1	X	X	X	1.5
0	0	0	1	0	X	X	X	3
0	0	0	1	1	X	X	X	4.5
0	0	1	0	0	X	X	X	6
0	0	1	0	1	X	X	X	7.5
0	0	1	1	0	X	X	X	9
0	0	1	1	1	X	X	X	10.5
0	1	0	0	0	X	X	X	12
0	1	0	0	1	X	X	X	13.5
0	1	0	1	0	X	X	X	15
0	1	0	1	1	X	X	X	16.5
0	1	1	0	0	X	X	X	18
0	1	1	0	1	X	X	X	19.5
0	1	1	1	0	X	X	X	21
0	1	1	1	1	X	X	X	22.5
1	0	0	0	0	X	X	X	24
1	0	0	0	1	X	X	X	25.5
1	0	0	1	0	X	X	X	27
1	0	0	1	1	X	X	X	28.5
1	0	1	0	0	X	X	X	30
1	0	1	0	1	X	X	X	31.5
1	0	1	1	0	X	X	X	33
1	0	1	1	1	X	X	X	34.5
1	1	0	0	0	X	X	X	36
1	1	0	0	1	X	X	X	37.5
1	1	0	1	0	X	X	X	39
1	1	0	1	1	X	X	X	40.5
1	1	1	0	0	X	X	X	42
1	1	1	0	1	X	X	X	43.5
1	1	1	1	0	X	X	X	45
1	1	1	1	1	X	X	X	46.5

TABLE 5

X: don't care

Register RC6

The content of RC6 sets the carrier level detector threshold. (Refer to table 6).

The threshold values are grouped by pair; values belonging to each pair have 2.5 dB separation which allows the signal processor to perform software hysteresis.

D7	D6	D5	D4	D3	D2	D1	D0	RC6
								Threshold (dBm)
0	0	0	X	X	X	X	X	— 29.85
0	0	1	X	X	X	X	X	— 27.35
0	1	0	X	X	X	X	X	— 36.65
0	1	1	X	X	X	X	X	— 34.15
1	0	0	X	X	X	X	X	— 46.75
1	0	1	X	X	X	X	X	— 44.25
1	1	0	X	X	X	X	X	— 46.75
1	1	1	X	X	X	X	X	— 44.25

TABLE 6

X: don't care

CLOCK

The master clock CLK, the receive conversion clock (RxCCLK) and the transmit conversion clock (TxCCLK) are generated in the TS68952 clock generator. There are three possible frequencies for the conversion clocks: 7.2 kHz, 8 kHz and 9.6 kHz.

The frequency of RxCCLK and TxCCLK is controlled by two independant Digital Phase Locked Loops (DPLL). TxCCLK can be synchronised on an external Terminal Clock (TxSCLK) or on the Rx bit rate clock ; in these cases 350 ns discrete phase shifts occurs on CLK and TxCCLK synchronously with TxCCLK negative edge with a repetition rate of 600 Hz, 800 Hz or 1000 Hz according to the programmation of RC1 control register in the TS68952.

AGC and CLD AMPLIFIERS

The AGC consists of two cascaded amplifiers A1 and A2, fig. 3. AC coupling is obtained from C1 and C2 external capacitors. C2 can be used as an auxiliary input for performing an analog loop located after echo cancellation. The carrier level detector (CLD) amplifier A3 also needs an external capacitor C3.

A/D CONVERSION

The A/D converter is a 12 bit resolution, 8 bit minimum integral linearity, monotonic converter. The input voltage ranges from — 2.5 V to + 2.5 V; and the conversion time is better than 50 μs.

ASYNCHRONOUS MULTIPLEXING

Samples on the output of S/H1 and S/H2 are converted respectively at RxCCLK frequency and TxCCLK frequency. Since RxCCLK and TxCCLK are plesiochronous, the order of conversion is determined by an asynchronous logic. The output register RR1 and RR2 are respectively loaded on the negative edge of RxCCLK and TxCCLK.

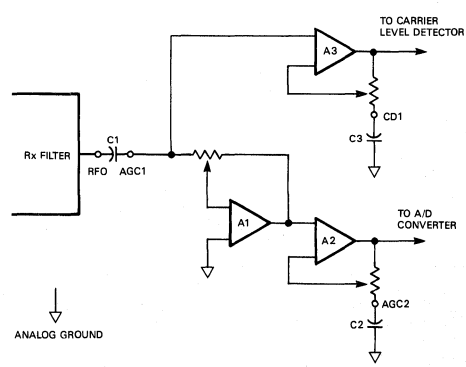


FIGURE 3. Rx AMPLIFIERS SCHEMATIC

ELECTRICAL SPECIFICATIONS

The electrical specifications are given for operating temperature range (0°C, 70°C).

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply voltage between V^+ and AGNC or DGND		— 0.3 to + 7	V
Supply voltage between V^- and AGND or DGND		— 7 to + 0.3	V
Voltage between AGND and DGND		— 0.3 to + 0.3	V
Digital input voltage		DGND−0.3 to V^++0.3	V
Digital output voltage		DGND−0.3 to V^++0.3	V
Digital output current		— 20 to + 20	mA
Analog input voltage		V_{CC}−0.3 to V^++0.3	V
Analog output voltage		V_{CC}−0.3 to V^++0.3	V
Analog output current		— 10 to + 10	mA
Power dissipation		500	mW
Operating temperature	T_{oper}	0 to + 70	°C
Storage temperature	T_{stg}	— 65 to + 150	°C

POWER SUPPLIES

DGND = AGND = 0 V

Characteristic	Symbol	Min	Typ	Max	Unit
Positive power supply	V^+	4.75	—	5.25	V
Negative power supply	V^-	— 5.25	—	— 4.75	V
Positive supply current (receive signal level 0 dBm)	I^+	—	—	20	mA
Negative supply current (receive signal level 0 dBm)	I^-	— 20	—	—	mA

DIGITAL INTERFACE

Control inputs

Voltages referenced to DGND = 0 V

Characteristic	Symbol	Min	Typ	Max	Unit
Low level input voltage	V_{IL}	—	—	0.8	V
High level input voltage	V_{IH}	2.2	—	—	V
Low level input current DGND < V_I < 0.8 V	V_{IL}	— 10	—	10	μA
High level input current 2.2 V < V_I < V^+	V_{IH}	— 10	—	10	μA

DATA BUS

Voltages referenced to DGND = 0 V

Characteristic	Symbol	Min	Typ	Max	Unit
Low level input voltage	V_{IL}	—	—	0.8	V
High level input voltage	V_{IH}	2.2	—	—	V
Low level output voltage (I_{OL} = 2.5 mA)	V_{OL}	—	—	0.4	V
High level output voltage (I_{OL} = 2.5 mA)	V_{OH}	2.4	—	—	V
High impedance output current (when $\overline{E}$ is high and DGND < V_I < V^+)	I_{OZ}	— 50	—	50	μA

ANALOG INTERFACE

All voltages referenced to AGND = 0 V

Characteristic	Symbol	Min	Typ	Max	Unit
Input voltage EEI,LEI,RAI	V_{in}	— 2.5	—	2.5	V
Input current EEI,LEI,RAI (— 2.5 V < V_{in} < 2.5 V)	I_{in}	— 1	—	1	μA
Input resistance AGC1, AGC2	R_{in}	1.5	—	—	kΩ
Input resistance CD1	R_{in}	0.7	—	—	kΩ
Output voltage RFO CL= 50 pF, RL= 1 kΩ	V_{out}	— 2.5	—	2.5	V
Output resistance RFO	R_{out}	—	—	2	Ω
Load resistance RFO	R_L	1	—	—	kΩ
Load capacitance RFO	C_L	—	—	50	pF

BUS TIMING CHARACTERISTICS

(See foot notes 1 and 2 on timing diagrams)

Characteristic		Symbol	Min	Typ	Max	Unit
Cycle time	(1)	t_{CYC}	320	—	—	ns
Pulse width $\overline{E}$ low level	(2)	t_{WEL}	180	—	—	ns
Pulse width $\overline{E}$ high level	(3)	t_{WEH}	100	—	—	ns
Clock rise and fall time	(4)	t_r, t_f	—	—	20	ns
Control signal hold time	(5)	t_{HCE}	10	—	—	ns
Control signal set-up time	(6)	t_{SCE}	40	—	—	ns
Input data set-up time	(7)	t_{SDI}	120	—	—	ns
Input data hold time	(8)	t_{HDI}	10	—	—	ns
Output data set-up time (1 TTL load and CL= 50 pF)	(9)	t_{SDO}	—	—	150	ns
Output high impedance delay time (1 TTL load and CL= 50 pF)	(10)	t_{dz}	—	—	80	ns

RECEPTION CHARACTERISTICS

PERFORMANCE OF THE WHOLE RECEPTION CHAIN (input RAI or LEI, output RR1)

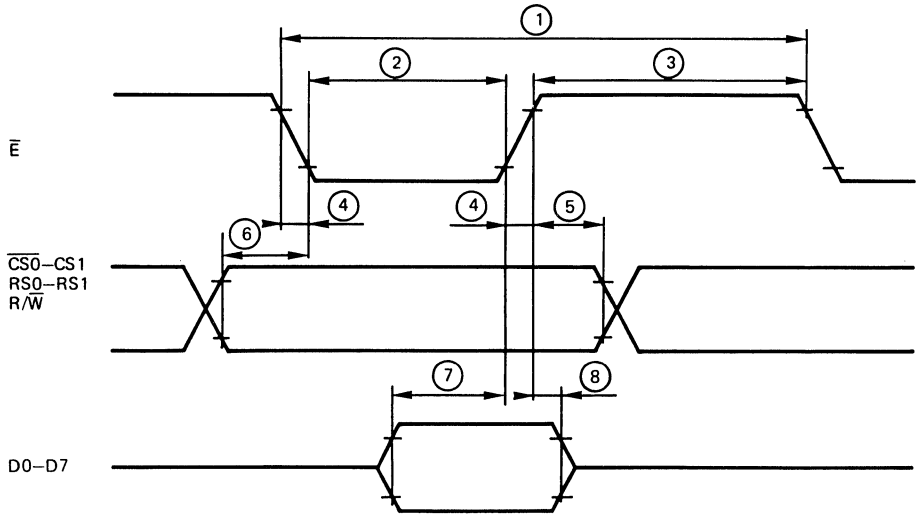
Characteristic	Symbol	Min	Typ	Max	Unit
Gain. (AGC gain = 0 dB, RxCCLK = 9600 Hz, V_{in}=775mV_{eff}, f = 2000 Hz)	G	— 0.5	—	0.5	dB
Total harmonic distortion (AGC gain = 0 dB, RxCCLK = 9600 Hz, V_{in}=775mV_{eff}, f = 2000 Hz)	TD	—	—	−58	dB
Equivalent RMS noise (AGC gain = 0 dB, RAI, LEI, EEI tied to AGND)	N	—	—	1.2	mV_{eff}

Note: Noise depends on AGC gain value.

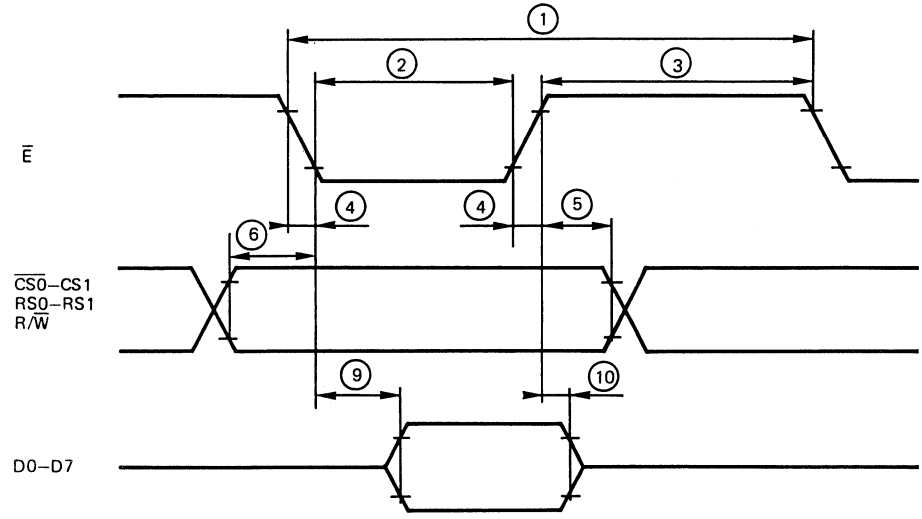
PERFORMANCE OF THE RECEPTION SUB-CHAIN (from RAI input to S/H2 input)

Parameter	Symbol	Min	Typ	Max	Unit
Total distortion (RxCCLK = 9600 Hz, V_{in} = 1.6 V_{eff}, f = 2000 Hz)	TD	—	—	— 72	dB

WRITE OPERATION



READ OPERATION



Notes:

1. Voltage levels shown are $V_{IL} < 0.4$ V, $V_{IH} > 2.4$ V, unless otherwise specified.
2. Measurement points shown are 0.8 V and 2.2 V, unless otherwise specified.

RECEIVE BAND-PASS FILTER AND REJECTION FILTER (input RAI, output RFO)

Characteristic	Symbol	Min	Typ	Max	Unit
Low-Pass filter (F_s=288kHz)					
Reference gain (V_{in} = 775 mV_{eff}, f = 1800 Hz)	G_{ref}	— 0.5	—	0.5	dB
Relative gain to G_{ref}	G_{rel}				
0 Hz < f < 3000 Hz		— 0.4	—	0.3	dB
f = 3200 Hz		— 3	—	0.3	dB
f > 6250 Hz		—	—	— 60	dB
Group propagation delay time (f = 1800 Hz)	T_{gp}	—	—	300	μs
Group propagation delay time distortion (600 Hz < f < 3000 Hz)	T_{gpd}	—	—	360	μs
High-Pass filter (F_s=72kHz)					
Reference gain (V_{in} = 775 mV_{eff}, f = 1800 Hz)	G_{ref}	— 0.5	—	0.5	dB
Relative gain to G_{ref}	G_{rel}				
0 Hz < f < 3000 Hz		— 0.4	—	0.3	dB
f = 500 Hz		— 3	—	0.5	dB
f < 100 Hz		—	—	— 25	dB
Group propagation delay time (f = 1800 Hz)	T_{gp}	—	—	50	μs
Group propagation delay time distortion (600 Hz < f < 3000 Hz)	T_{gpd}	—	—	450	μs
High-Pass filter and rejection filter (F_s=72kHz)					
Reference gain (V_{in} = 775 mV_{eff}, f = 1800 Hz)	G_{ref}	— 1	—	0	dB
Relative gain to G_{ref}	G_{rel}				
f = 100 Hz		—	—	— 25	dB
f = 370 Hz		—	—	— 27	dB
390 Hz < f < 450 Hz		—	—	— 30	dB
f = 470 Hz		—	—	— 27	dB
f = 900 Hz		—	—	0	dB
Group propagation delay time (f = 1800 Hz)	T_{gp}	—	—	75	μs
Group propagation delay time distortion (600 Hz < f < 3000 Hz)	T_{gpd}	—	—	1400	μs

Note: The measurement frequencies are integer sub-multiples of filters sampling frequencies.

RECONSTRUCTION FILTER

Characteristic	Symbol	Min	Typ	Max	Unit
Reconstruction filter (Fs 288kHz)					
Reference gain (V_{in} = 775 mV_{eff}, f = 2000 Hz)	G_{ref}	— 0.3	—	0.3	dB
Relative gain to G_{ref} 0 Hz < f < 2900 Hz f = 3100 Hz f > 6000 Hz	G_{rel}	 — 0.4 — 3 —	 — — —	 0.3 0.3 — 60	 dB dB dB
Group propagation delay time (f = 1800 Hz)	T_{gp}	—	—	300	μs
Group propagation delay time distortion (600 Hz < f < 3000 Hz)	T_{gpd}	—	—	440	μs
Whole reception filtering chain (input RAI or LEI, output RFO)					
Reference gain (V_{in} = 775 mV_{eff}, f = 2000 Hz, RC3 = $A0)	G_{ref}	— 0.5	—	0.5	dB
Noise on RFO (RAI, LEI, EEI tied to AGND 250 Hz < f < 3200 Hz)	N_{rfo}	—	—	300	μV_{eff}

PERFORMANCE OF RESIDUAL SIGNAL CHANNEL AND A/D CONVERTER (input EEI, output RR2)

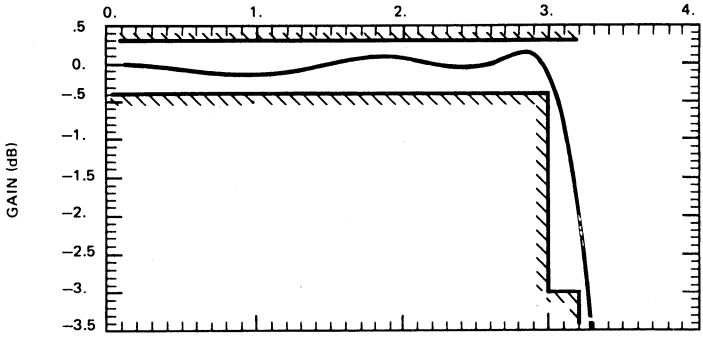
Characteristic	Symbol	Min	Typ	Max	Unit
Input voltage (peak to peak)	V_{in}	—	—	5	V
A/D converter resolution	R_{esh}	—	—	12	Bit
Analog increment	LSB	—	1.2	—	mV
Integral linearity error	E_{il}	— 16	—	16	LSB
Differential linearity error	E_{dl}	— 0.7	—	0.7	LSB
Offset voltage	V_{os}	— 100	—	100	LSB

AGC AMPLIFIER AND A/D CONVERTER (input AGC1, output RR1)

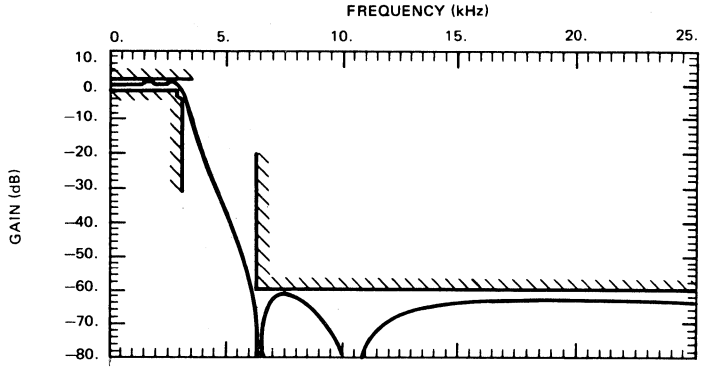
Characteristic	Symbol	Min	Typ	Max	Unit
Relative gain to programmed gain 0 dB ≤ AGC ≤ 24 dB 25.5 dB ≤ AGC ≤ 46.5 dB	G_{rel}	 — 0.5 — 1	 — —	 0.5 1	 dB dB
Offset voltage	V_{os}	— 70	—	70	LSB

CARRIER LEVEL DETECTOR (input AGC1, output CDR)

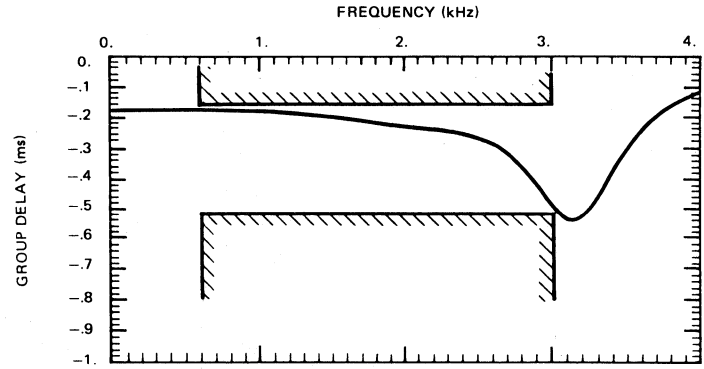
Characteristic	Symbol	Min	Typ	Max	Unit
Relative threshold to programmed gain 0 dB < AGC < 24 dB 25.5 dB ≤ AGC ≤ 46.5 dB	T_{rel}	 — 0.5 — 1	 — —	 0.5 1	 dB dB
Hysteresis	H_{yst}	2	—	3	dB
Input offset voltage 1st threshold pair 2nd threshold pair 3rd threshold pair	V_{os}	 — 1 — 2 — 3	 — — —	 1 2 3	 mV mV mV
Detection delay time 0 mV_{eff} to 775 mV_{eff} transition or 775 mV_{eff} to 0 V_{eff} transition	T_{dd}	1	—	3	ms



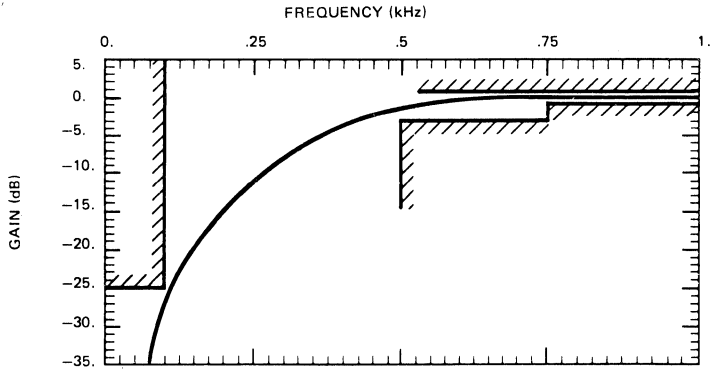
Rx LOW-PASS FILTER TYPICAL RESPONSE AND LIMITS CHART (Fs=288kHz)



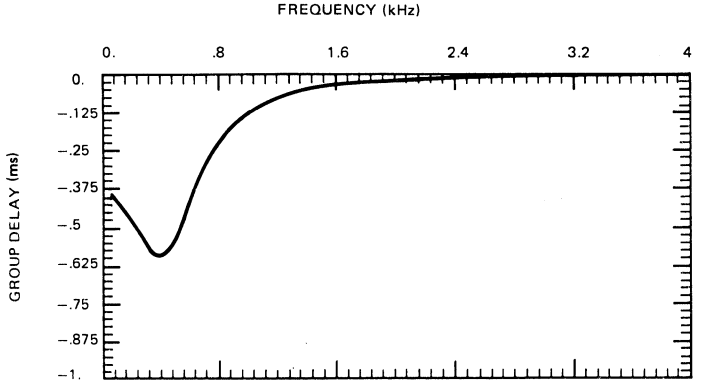
Rx LOW-PASS FILTER TYPICAL RESPONSE AND LIMITS CHART (Fs=288kHz)



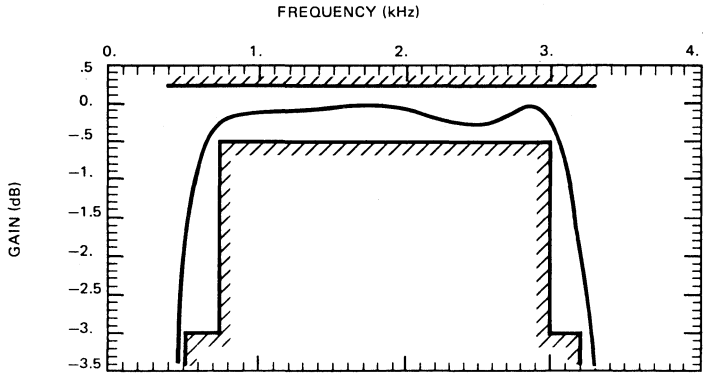
Rx LOW-PASS FILTER TYPICAL GROUP DELAY TIME AND LIMITS CHART (Fs=288kHz)



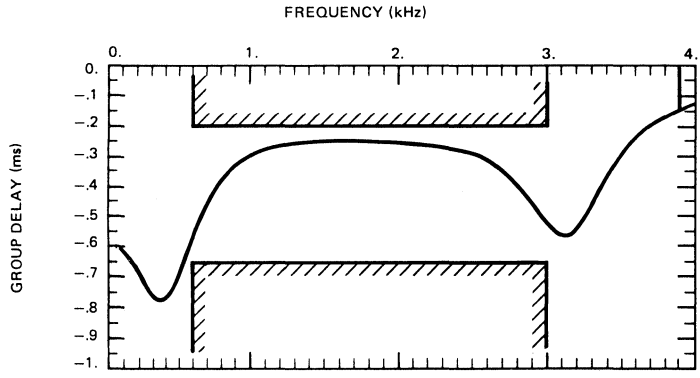
Rx HIGH-PASS FILTER TYPICAL RESPONSE AND LIMITS CHART (Fs=72kHz)



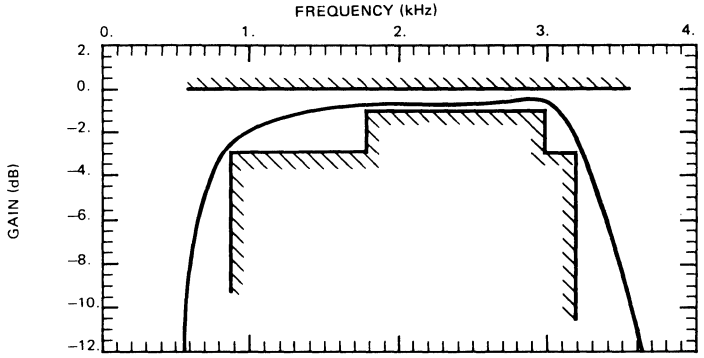
Rx HIGH-PASS FILTER TYPICAL GROUP DELAY TIME AND LIMITS CHART (Fs=72kHz)



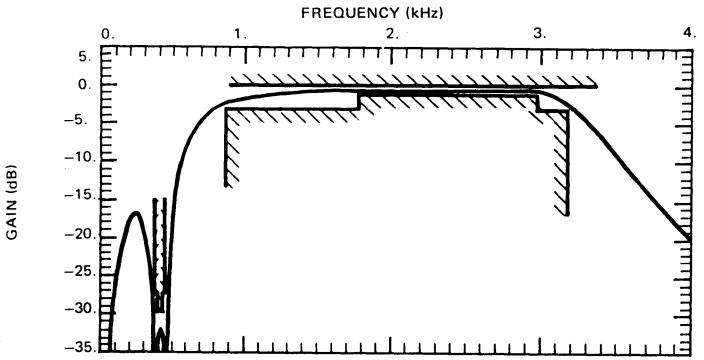
Rx BAND-PASS FILTER TYPICAL RESPONSE AND LIMITS CHART
(HP: Fs=72kHz, LP. Fs=288kHz)



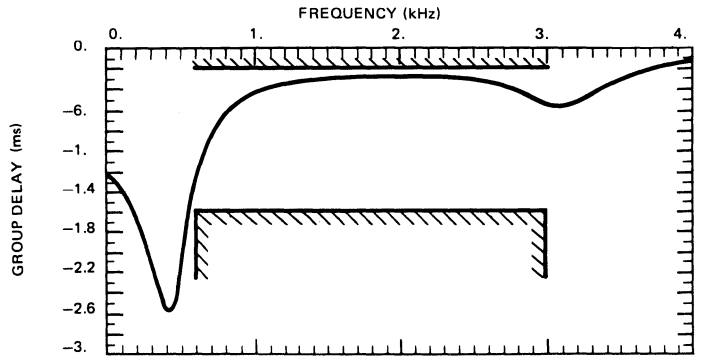
Rx BAND-PASS FILTER TYPICAL GROUP DELAY TIME AND LIMITS CHART
(HP: Fs=72kHz, LP: Fs=288kHz)



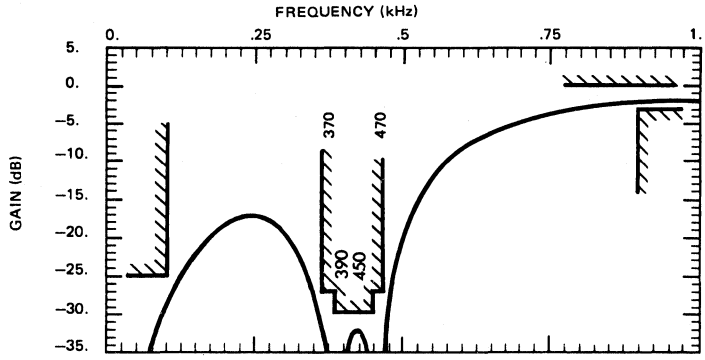
Rx BAND-PASS AND REJECTION FILTER TYPICAL RESPONSE AND LIMITS CHART
(HP AND REJ. : Fs=72kHz, LP: Fs=288kHz)



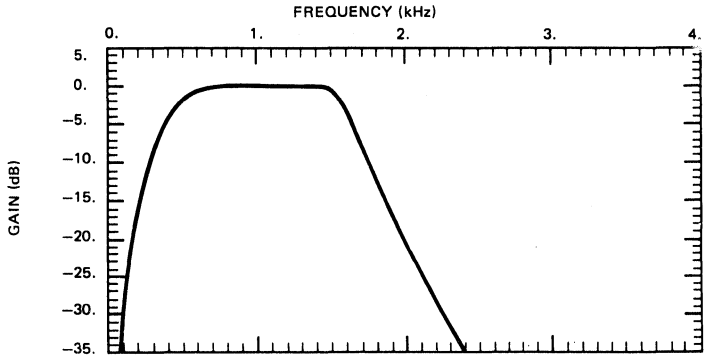
Rx BAND-PASS AND REJECTION FILTER TYPICAL RESPONSE AND LIMITS CHART
(HP AND REJ. :Fs=72kHz, LP: Fs=288kHz)



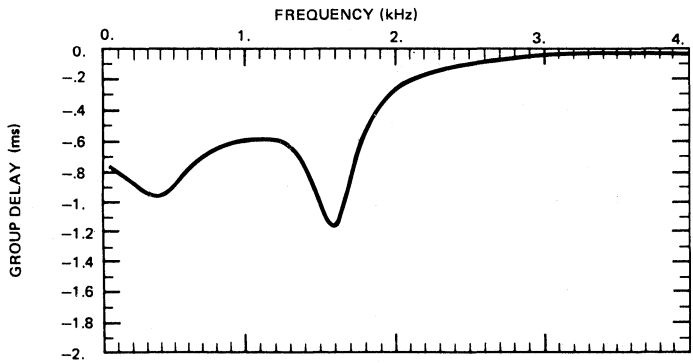
Rx BAND-PASS AND REJECTION FILTER TYPICAL GROUP DELAY TIME AND LIMITS CHART
(HP AND REJ. : Fs=72kHz, LP: Fs=288kHz)



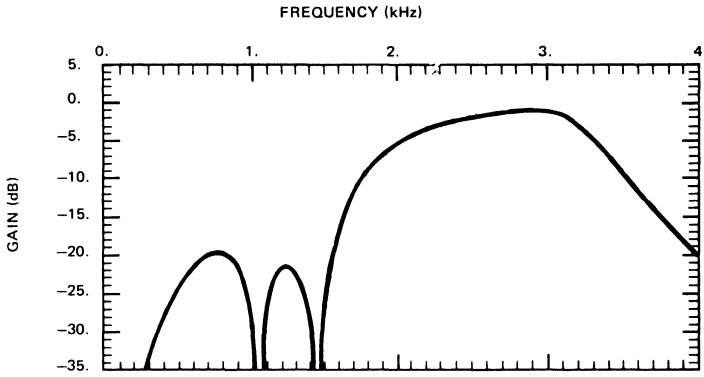
Rx HIGH-PASS AND REJECTION FILTER TYPICAL RESPONSE AND LIMITS CHART (Fs=72kHz)



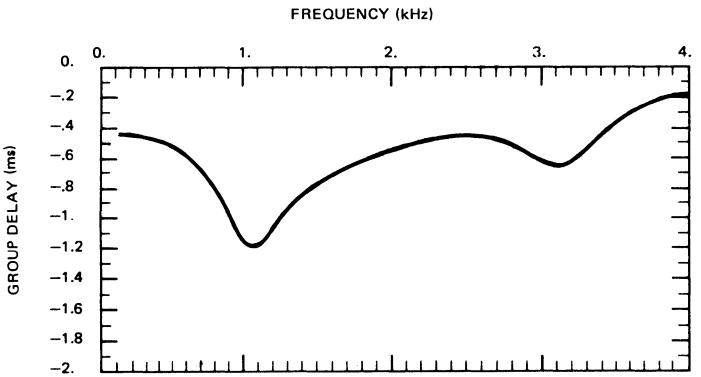
Rx BAND-PASS FILTER TYPICAL RESPONSE FOR V.22 MODE (LOW CHANNEL)
(HP: Fs=72kHz, LP: fs=144kHz)



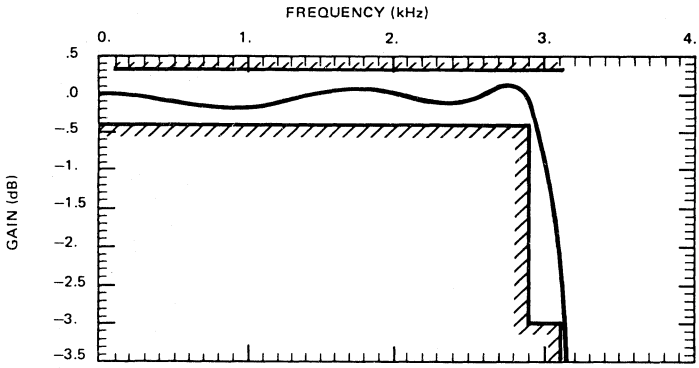
Rx BAND-PASS FILTER TYPICAL GROUP DELAY TIME FOR V.22 MODE (LOW CHANNEL)
(HP: Fs=72kHz, LP: Fs=144kHz)



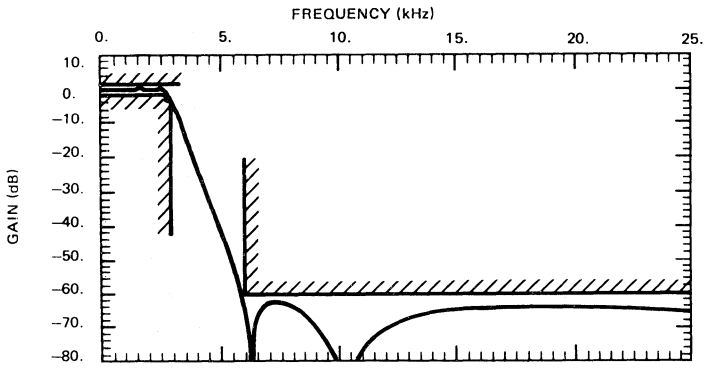
Rx BAND-PASS FILTER TYPICAL RESPONSE FOR V.22 MODE (HIGH CHANNEL)
(HP AND REJ.: Fs=144kHz, LP: Fs=288kHz)



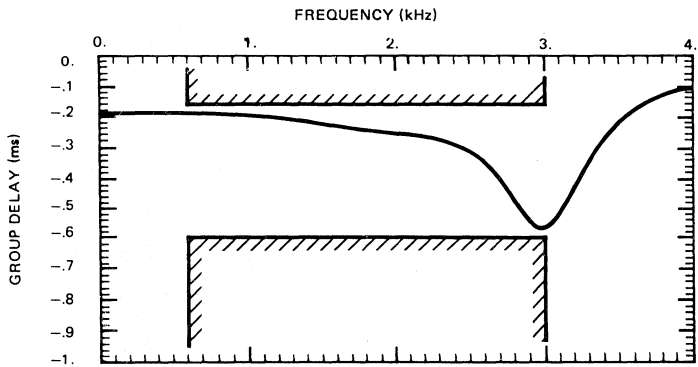
Rx BAND-PASS FILTER TYPICAL GROUP DELAY TIME FOR V.22 MODE (HIGH CHANNEL)
(HP AND REJ.: Fs=144kHz, LP: Fs=288kHz)



RECONSTRUCTION FILTER TYPICAL RESPONSE AND LIMITS CHART



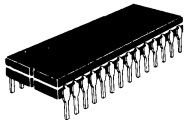
RECONSTRUCTION FILTER TYPICAL RESPONSE AND LIMITS CHARTS

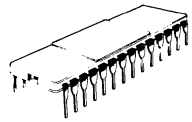


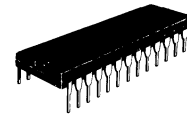
RECONSTRUCTION FILTER TYPICAL GROUP DELAY TIME AND LIMITS CHART

PHYSICAL DIMENSIONS

CB-132



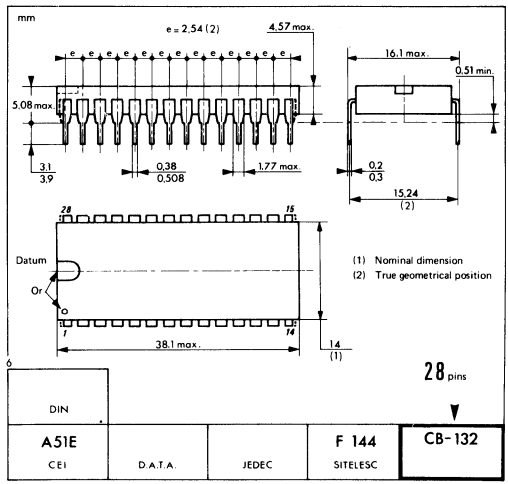




J SUFFIX
CERDIP PACKAGE

ALSO AVAILABLE
C SUFFIX
CERAMIC PACKAGE

P SUFFIX
PLASTIC PACKAGE



DATA SHEET

SILICON GATE CMOS

MODEM TRANSMIT/RECEIVE CLOCK GENERATOR

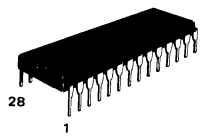
The TS68952 generates all the clock frequencies needed to implement standard voice-grade MODEMS up to 19200 bps according to the CCITT V.22, V.26, V.27, V.29, V.32 and V.33 or BELL 212A, 208 and 209 recommendations.

It can be associated with the TS68950 and the TS68951 to give a MODEM Analog Front-End Chip Set.

Main features:

- Independent Tx and Rx clock generators with Digital Phase Locked Loops (DPLLs).
- Tx DPLL synchronization on external terminal clock or internal Rx clock.
- Four external clocks available (plesiochronous on Tx and Rx channels): bit rate clock, baud rate clock, sampling clock and multiplexing clock.
- Chip programming and control via a standard 8 bit bus.

CASE CB-132

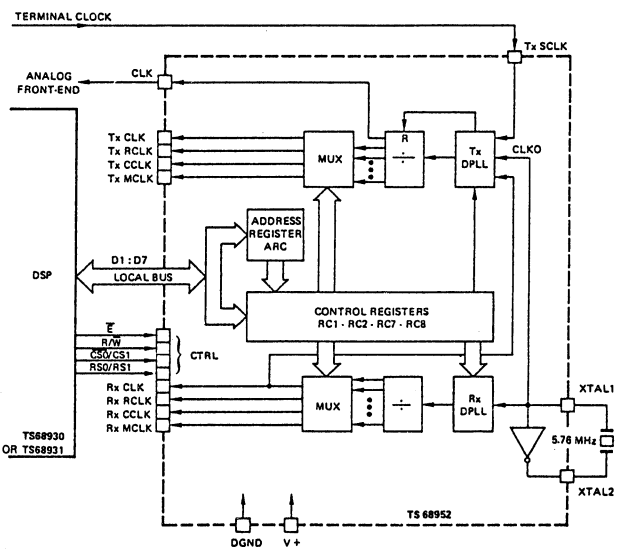


P SUFFIX
PLASTIC PACKAGE

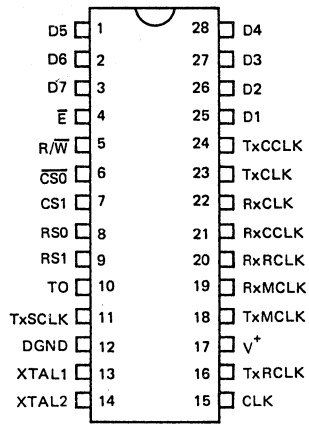
ALSO AVAILABLE
C SUFFIX
CERAMIC PACKAGE

J SUFFIX
CERDIP PACKAGE

BLOCK DIAGRAM



PIN ASSIGNMENT



PIN DESCRIPTION

Name	No.	Description
D5-D7	1-3	Data bus inputs to internal registers
$\overline{E}$	4	Enable input. Data are strobed on the positive transitions of this input
R/$\overline{W}$	5	Read/Write selection input. Internal registers can be written when R/W = 0. Reading mode is only used for Rx analog front-end chip
$\overline{CS0}$-CS1	6-7	Chip Select inputs. The chip set is selected when $\overline{CS0}$ = 0 and CS1 = 1
RS0-RS1	8-9	Register Select inputs. Used to select address or control registers
TO	10	Test Output. Must be left open
TxSCLK	11	Transmit Synchronizing Clock input. Normally tied to an external terminal clock. When this pin is tied to a permanent logical level, transmit DPLL free-runs or can be synchronized to the receive clock system.
DGND	12	Digital ground = 0 V. All digital signals are referenced to this pin
XTAL1	13	Crystal oscillator or pulse generator input
XTAL2	14	Crystal oscillator output
CLK	15	1.44 MHz Clock output. Useful for Tx and Rx analog front-end chips
TxRCLK	16	Transmit baud Rate Clock output
V^+	17	Positive power supply voltage = + 5 V ± 5 %
TxMCLK	18	Transmit Multiplexing Clock output
RxMCLK	19	Receive Multiplexing Clock output
RxRCLK	20	Receive baud Rate Clock output
RxCCLK	21	Receive Conversion Clock output
RxCLK	22	Receive bit rate Clock output
TxCLK	23	Transmit bit rate Clock output
TxCCLK	24	Transmit Conversion Clock output
D1-D4	25-28	Data bus inputs to internal registers (D0 is not used)

FUNCTIONAL DESCRIPTION

The TS68952 is a purely digital circuit that synthesises all the frequencies requested to implement synchronous voice-grade MODEMs from 1200 bps to 19200 bps. It consists of two clock generators using Digital Phase Locked Loops (DPLLs). Frequency programming and DPLL updating can be obtained through four control registers accessed by indirect or cyclical addressing.

This circuit is a part of a three chip Modem Analog Front-End that also includes the TS68950 transmitting analog interface and the TS68951 receiving analog interface.

POWER-UP INITIAL CONDITIONS

Following power-up, the eight transmit and receive clock outputs are undefined and may deliver any frequencies. Control registers RC1 and RC2 must be properly programmed to obtain the wanted operation.

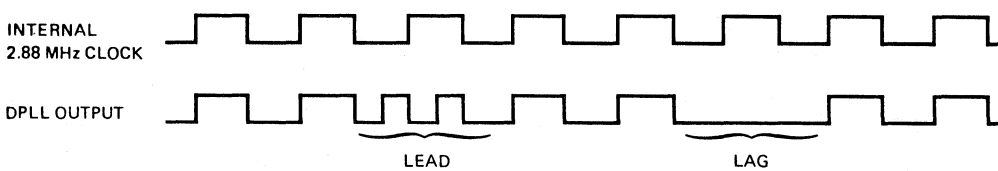


FIGURE 1 – DPLL LEAD AND LAG

CLOCK GENERATION

Master clock is obtained from either a crystal tied between XTAL1 and XTAL2 pins or an external signal connected to the XTAL1 pin; in this case, the XTAL2 pin should be left open. Clock frequency nominal value is 5.76 MHz, but 5.12 MHz and 5.40 MHz frequencies are also specified for particular applications.
The different transmit (Tx) and receive (Rx) clocks are obtained by frequency division in several counters and output selection through digital multiplexers. They can be synchronized on external signal via two independent digital phase locked loops (DPLL).

TRANSMIT DPLL

As shown on figure 1, the TxDPLL operates by adding or subtracting pulses to a 2.88 MHz internal clock, with a reference frequency that is a submultiple of the programmed "rate clock" frequency. This corresponds to phase leads or phase lags of about 350 ns duration, more precisely, two master clock periods.
The Tx DPLL can be synchronized on an external terminal clock tied to TxSCLK pin or on the receive bit clock RxCLK internally generated from the RxDPLL. It can also free-run without any phase shift, when the TxSCLK input is tied to a fixed logical level.

TRANSMIT CLOCKS

The TS68952 delivers four synchronous Tx clocks:

- a bit clock, TxCLK, whose frequency equals the bit rate of the MODEM,
- a baud clock, TxRCLK, whose frequency equals the baud rate of the MODEM,
- a conversion clock, TxCCLK, that gives the sampling frequency of the Tx converter,
- a multiplexing clock, TxMCLK, usable when several terminals are multiplexed on a single physical link.

The frequencies of these four clocks are programmable through RC1 and RC2 control registers. Their cyclical ratio is exactly 1 : 2, except for the 16.8 kHz frequency whose cyclical ratio is slightly modulated around 1 : 2, and their relative phase locking is ensured without user intervention, by periodic reset of the counters.

Immediate phasing of these clocks on the synchronizing external TxSCLK or internal RxCLK clock can be obtained through bit 7 of RC8 register. The content of this register is automatically cleared after phasing completion.

The TS68952 also delivers, on pin CLK, a 1.44 MHz clock that is synchronous with the Tx clock system and will be used as the main clock of the TS68950/51 analog interface circuits.

RECEIVE DPLL

RxDPLL phase shifts are performed by addition and subtraction of pulses from an internal 1.44 MHz clock under the control of RC8 register. Two modes of operation are provided:

- a coarse phase lag whose amplitude has been loaded into RC7 register, can be controlled by one bit of RC8 register. This mode is useful for a fast synchronization of the RxDPLL. The phase lag is obtained by suppressing a variable number of pulses at the input of the counters,
- a fine phase shift with lead or lag amplitude equal to two master clock periods, can be controlled by two bits of RC8. This mode corresponds to normal operation. The phase shifts are obtained by addition or suppression of pulses as indicated in figure 1.

RC8 register is automatically cleared when the programmed phase shift is completed. Simultaneous programming of Tx and Rx control bits of this register has to be avoided.

RECEIVE CLOCKS

The TS68952 delivers four Rx clocks with the same nominal frequency values as their Tx counterparts:

- a bit clock RxCLK,
- a baud clock RxRCLK,
- a conversion clock RxCCLK,
- a multiplexing clock RxMCLK.

The Rx and Tx output clocks are plesiochronous.

BIT CLOCK FREQUENCY PROGRAMMING (Tx AND Rx)

RC1 REGISTER							OUTPUT FREQUENCY (kHz)		
D7	D6	D5	D4	D3	D2	D1			
HB4	HB3	HB2	HB1	HR3	HR2	HR1	F_Q = 5.76 MHz	F_Q = 5.40 MHz	F_Q = 5.12 MHz
0	0	0	0				19.2		
0	0	0	1				16.8		
0	0	1	0				14.4		
0	0	1	1				12.0		
0	1	0	0				9.6		
0	1	0	1				7.2		6.4
0	1	1	0				6.4		
0	1	1	1				6.0		
1	0	0	0				4.8		
1	0	0	1				3.2	3.0	
1	0	1	0				2.4		
1	0	1	1				1.2		
1	1	0	0				0.6		
1	1	0	1				0.6		
1	1	1	0				0.6		
1	1	1	1				0.6		

F_Q = crystal oscillator frequency

RATE CLOCK FREQUENCY PROGRAMMING (Tx AND Rx)

RC1 REGISTER							OUTPUT FREQUENCY (kHz)		
D7	D6	D5	D4	D3	D2	D1			
HB4	HB3	HB2	HB1	HR3	HR2	HR1	F_Q = 5.76 MHz	F_Q = 5.40 MHz	F_Q = 5.12 MHz
				0	0	0	2.4		2.133
				0	0	1	2.0*		
				0	1	0	1.6**	1.5	
				0	1	1	1.2		
				1	0	0	0.6		
				1	0	1	0.6		
				1	1	0	0.6		
				1	1	1	0.6		

Note: Phase shift frequency of Tx DPLL is 600 Hz except for (*) 1000 Hz and for (**) 2000 Hz.

CONVERSION CLOCK FREQUENCY PROGRAMMING (Tx AND Rx)

RC2 REGISTER							OUTPUT FREQUENCY (kHz)		
D7	D6	D5	D4	D3	D2	D1			
HM3	HM2	HM1	HS2	HS1	HTHR	—	F_Q = 5.76 MHz	F_Q = 5.40 MHz	F_Q = 5.12 MHz
			0	0			9.6	9.0	8.533
			0	1			8.0	7.5	
			1	0			7.2		
			1	1			7.2		

MULTIPLEXING CLOCK FREQUENCY PROGRAMMING (Tx AND Rx)

RC2 REGISTER							OUTPUT FREQUENCY (kHz)
D7	D6	D5	D4	D3	D2	D1	
HM3	HM2	HM1	HS2	HS1	HTHR	—	F_Q = 5.76 MHz
0	0	0					1440
0	0	1					288
0	1	0					12
0	1	1					9.6
1	0	0					7.2
1	0	1					4.8
1	1	0					2.4
1	1	1					1.2

Tx SYNCHRONIZATION SIGNAL PROGRAMMING

RC2 REGISTER							SYNCHRONIZATION SIGNAL
D7	D6	D5	D4	D3	D2	D1	
HM3	HM2	HM1	HS2	HS1	HTHR	—	
					0		RxCLK
					1		TxSCLK (note 1)

Note: 1 - TxDPLL free-runs if there is no transition on this input.

Tx CLOCK GENERAL RESET

RC8 REGISTER (notes 2,3)							RESETTING TRANSITION
D7	D6	D5	D4	D3	D2	D1	
MPE	SPR	AVRE	VAL	INIT	—	—	
1	0	0	0	0			Next negative-going transition on synchronization clock

Note: 2 - RC8 register is cleared after the programmed control operation is completed.

Note: 3 - INIT bit is only used for test purpose

Rx CLOCK PHASE SHIFT PROGRAMMING

RC8 REGISTER (note 2)							
D7	D6	D5	D4	D3	D2	D1	
MPE	SPR	AVRE	VAL	INIT	—	—	ACTION ON Rx DPLL
0	1	0	0	0			Phase lag of programmed amplitude
0	0	0	1	0			Phase lag of two main clock periods
0	0	1	1	0			Phase lead of two main clock periods

Rx CLOCK PHASE SHIFT AMPLITUDE PROGRAMMING

RC7 REGISTER							PHASE SHIFT IN DEGREES		
D7	D6	D5	D4	D3	D2	D1			
SP5	SP4	SP3	SP2	SP1	—	—	1200 bauds*	1600 bauds	NUMBER OF MASTER CLOCK PULSES SUPPRESSED
0	0	0	0	0			1.5	2	20
0	0	0	0	1			3	4	40
0	0	0	1	0			4.5	6	60
0	0	0	1	1			6	8	80
0	0	1	0	0			7.5	10	100
0	0	1	0	1			9	12	120
0	0	1	1	0			10.5	14	140
0	0	1	1	1			12	16	160
0	1	0	0	0			13.5	18	180
0	1	0	0	1			15	20	200
0	1	0	1	0			16.5	22	220
0	1	0	1	1			18	24	240
0	1	1	0	0			19.5	26	260
0	1	1	0	1			21	28	280
0	1	1	1	0			22.5	30	300
0	1	1	1	1			24	32	320
1	0	0	0	0			22.5	30	300
1	0	0	0	1			45	60	600
1	0	0	1	0			67.5	90	900
1	0	0	1	1			90	120	1200
1	0	1	0	0			112.5	150	1500
1	0	1	0	1			135	180	1800
1	0	1	1	0			157.5	210	2100
1	0	1	1	1			180	240	2400
1	1	0	0	0			202.5	270	2700
1	1	0	0	1			225	300	3000
1	1	0	1	0			247.5	330	3300
1	1	0	1	1			270	360	3600
1	1	1	0	0			292.5		3900
1	1	1	0	1			315		4200
1	1	1	1	0			337.5		4500
1	1	1	1	1			360		4800

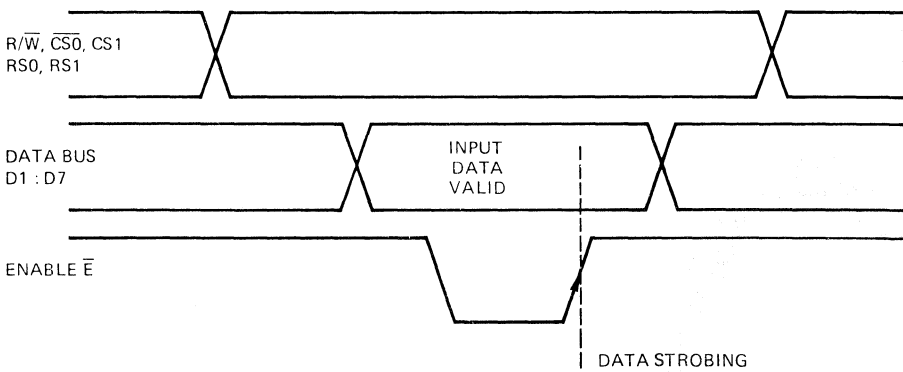
(*) 2400 bauds: multiply by two. 600 bauds: divide by two.

DATA BUS CONTROL

Six signals control the access from the bus to the internal registers according to the table and the timing diagram given below. Control registers are written using an indirect addressing mode where the internal address is stored in the 3 bit ARC register. After each write operation to a control register, the ARC register value is automatically increased by one. This allows cyclical addressing of the eight registers of the MODEM chip set.

R/$\overline{W}$	$\overline{CS0}$	$\overline{CS1}$	RS0	RS1	$\overline{E}$	ACCESSED REGISTER
0	0	1	1	0	↓	Address register ARC
0	0	1	1	1	↓	Control register whose address is in ARC

BUS TIMING DIAGRAM



DATA FORMAT

DATA LOADED IN ARC			
D7	D6	D5	
ARC3	ARC2	ARC1	ADDRESSED REGISTER
0	0	0	RC1
0	0	1	RC2
1	1	0	RC7
1	1	1	RC8

MAXIMUM RATINGS

RATING	MIN.	MAX.
V^+ supply voltage to DGND ground	- 0.3 V	7 V
Voltage at any input or output	DGND - 0.3 V	$V^+ + 0.3$ V
Current at any output	- 20 mA	20 mA
Power dissipation		500 mW
Operating temperature range	0 °C	70 °C
Storage temperature range	- 65 °C	+ 150 °C

OPERATING RANGE

Ambient temperature	V^+	DGND
$0\ °C \leqslant t_{amb} \leqslant +\ 70\ °C$	$+ 5.0\ V \pm 5\ \%$	0 V

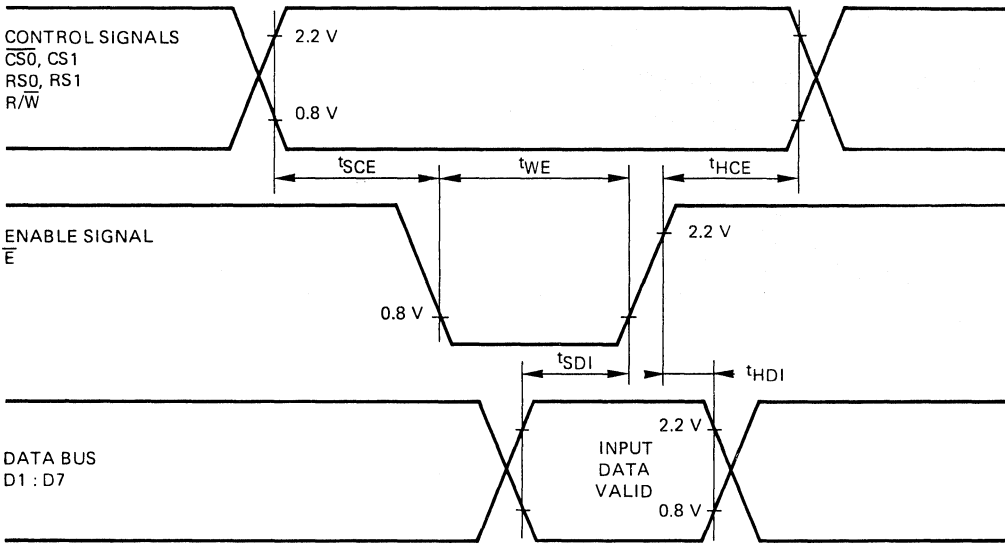
ELECTRICAL OPERATING CHARACTERISTICS

Unless otherwise noted, electrical characteristics are specified over the operating range. Typical values are given for $V^+ = 5.0$ V and $t_{amb} = 25$ °C.

CHARACTERISTIC	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Power dissipation						
Positive supply current	I^+				5.0	mA
Digital interface						
Input low level voltage	V_{IL}				0.8 V	V
Input high level voltage	V_{IH}		2.2			V
Input low level current	I_{IL}	$DGND \leqslant V_I \leqslant V_{IL\ max}$	- 10		10	μA
Input high level current	I_{IH}	$V_{IH\ min} \leqslant V_I \leqslant V^+$	- 10		10	μA
Output low level current	V_{OL}	$I_O = 2.5$ mA			0.4	V
Output high level current	V_{OH}	$I_O = -\ 2.5$ mA	2.4			V
Crystal oscillator interface						
Input low level voltage	V_{IL}				1.5	V
Input high level voltage	V_{IH}		3.5			V
Input low level current	I_{IL}	$DGND \leqslant V_I \leqslant V_{IL\ max}$	- 15			μA
Input high level current	I_{IH}	$V_{IH\ min} \leqslant V_I \leqslant V^+$			15	μA

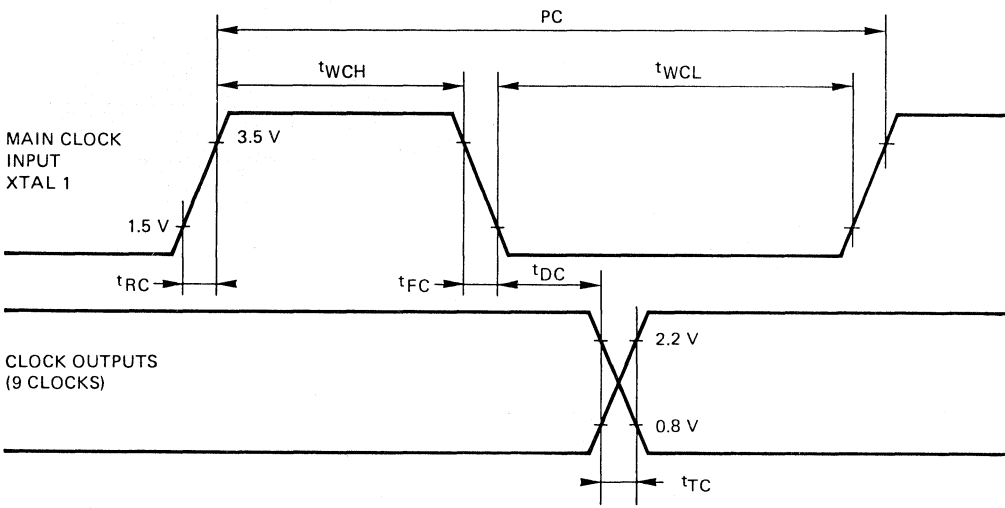
TIMING CHARACTERISTICS

CHARACTERISTIC	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Data bus access						
Control signals set-up time	t_{SCE}	$\overline{CS0}$, CS1, RS0, RS1, R/$\overline{W}$ to $\overline{E}$	40			ns
Control signals hold time	t_{HCE}	$\overline{CS0}$, CS1, RS0, RS1, R/$\overline{W}$ to $\overline{E}$	10			ns
Data-in set-up time	t_{SDI}	D1 : D7 to $\overline{E}$	120			ns
Data-in hold time	t_{HDI}	D1 : D7 to $\overline{E}$	10			ns
Enable signal low level width	t_{WE}	$\overline{E}$		180		ns

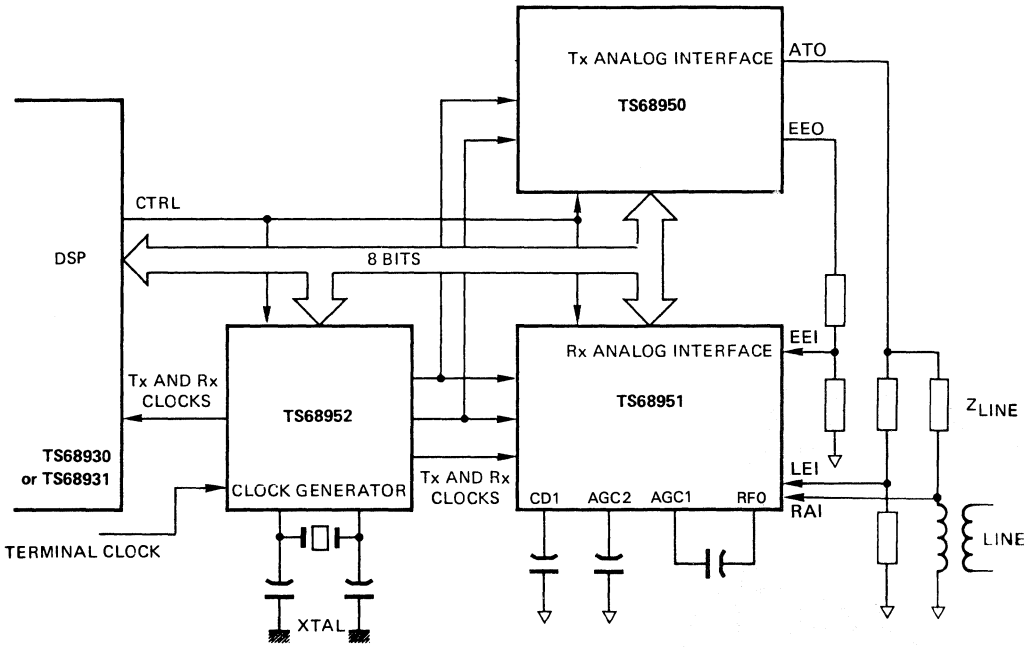


TIMING CHARACTERISTICS (continued)

CHARACTERISTIC	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Clock wave forms						
Main clock period	PC	XTAL1 input	150	173.6		ns
Main clock low level width	t_{WCL}	XTAL1 input	50			ns
Main clock high level width	t_{WCH}	XTAL1 input	50			ns
Main clock rise time	t_{RC}	XTAL1 input			50	ns
Main clock fall time	t_{FC}	XTAL1 input			50	ns
Clock output delay time	t_{DC}	All clock outputs CL = 50 pF			500	ns
Clock output transition time	t_{TC}	All clock outputs CL = 50 pF			100	ns



TYPICAL APPLICATION



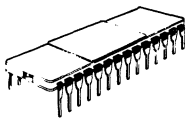
MODEM ANALOG FRONT-END CHIP SET

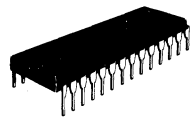
NOTE: Digital ground

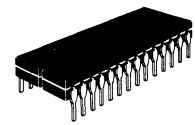
Analog ground

PHYSICAL DIMENSIONS

CB-132





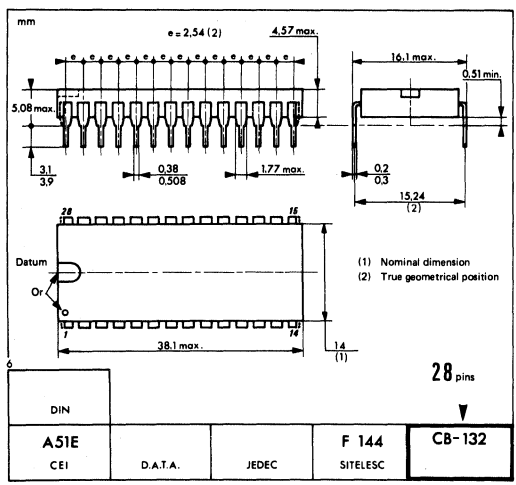


ALSO AVAILABLE

C SUFFIX
CERAMIC PACKAGE

P SUFFIX
PLASTIC PACKAGE

J SUFFIX
CERDIP PACKAGE



CHAPTER 4 - SUBSCRIBER LINE CARD COMPONENTS

THOMSON COMPONENTS MOSTEK

TS5070 • TS5071

MONOLITHIC PROGRAMMABLE CODEC/FILTER COMBO 2ND GENERATION

ADVANCE INFORMATION

COMMUNICATIONS PRODUCTS

ADVANCE INFORMATION

The TS5070 series are second-generation combined PCM CODEC and Filter devices optimized for digital switching applications on subscriber and trunk line cards. Using advanced switched capacitor techniques, COMBO IIG combines transmit bandpass and receive lowpass channel filters with a companding PCM encoder and decoder. The devices are A-law and μ-law selectable and employ a conventional serial PCM interface capable of being clocked up to 4.096 MHz. A number of programmable functions may be controlled via a serial control port.

Channel gains are programmable over a 25.4 dB range in each direction, and a programmable filter is included to enable Hybrid Balancing to be adjusted to suit a wide range of loop impedance conditions. Both transformer and active SLIC interface circuits with real or complex termination impedances can be balanced by this filter, with cancellation in excess of 30 dB being readily achievable when measured across the passband against standard test termination networks.

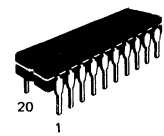
To enable COMBO IIG to interface to the SLIC control leads, a number of programmable latches are included; each may be configured as either an input or an output. The TS5070 provides 6 latches and the TS5071 5 latches.

- Complete CODEC and FILTER system including:
  - Transmit and receive PCM channel filters
  - μ-law or A-law companding coder and decoder
  - Receive power amplifier drives 300 Ω
  - 4.096 MHz serial PCM data (max)
- Programmable Functions:
  - Transmit gain: 25.4 dB range, 0.1 dB steps
  - Receive gain: 25.4 dB range, 0.1 dB steps
  - Hybrid balance cancellation filter
  - Time-slot assignment: up to 64 slots/frame
  - 2 port assignment (TS5070)
  - 6 interface latches (TS5070)
  - A or μ-law
  - Analog loopback
  - Digital loopback
- Direct interface to solid-state SLICs
- Simplifies transformer SLIC, single winding secondary
- Standard serial control interface
- 70 mW operating power (typ)
- 5 mW standby power (typ)
- Meets or exceeds all CCITT and LSSGR specifications
- TTL and CMOS compatible digital interfaces
- Second source of TP3070, TP3071

CMOS

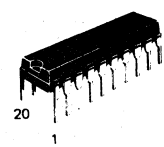
CASES

J20A



J SUFFIX
CERDIP PACKAGE

CB-194

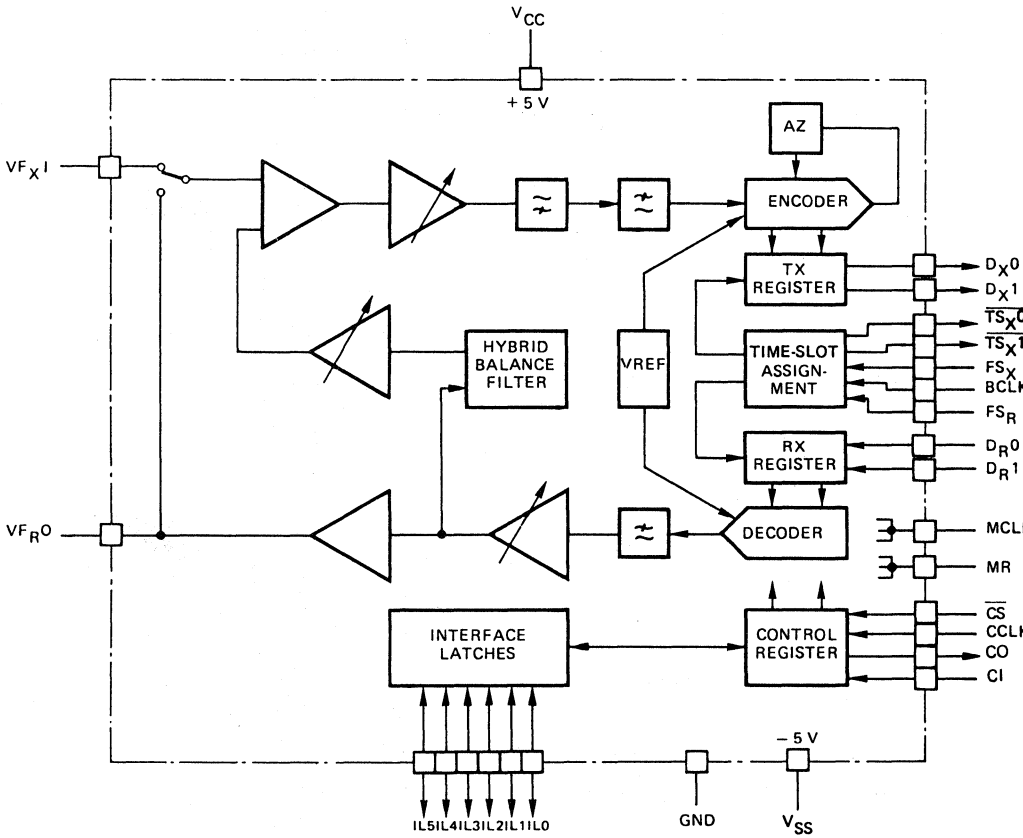


P SUFFIX
PLASTIC PACKAGE

CB-520

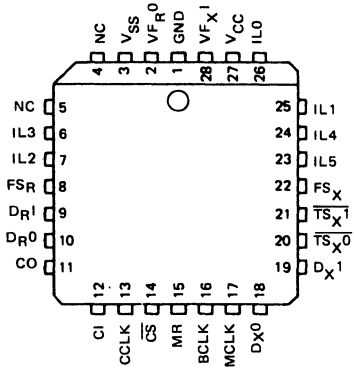
FN SUFFIX
PLCC PACKAGE

BLOCK DIAGRAM

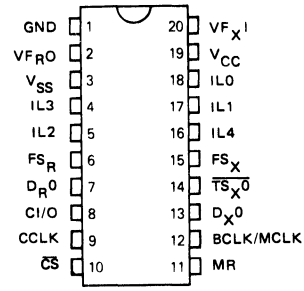


PIN ASSIGNMENTS

TS5070



TS5071



PIN DESCRIPTION

POWER SUPPLY, CLOCK

Name	Pin Type	TS 5070	TS5071	Function	Description
V_{CC}	S	27	19	Positive power supply	+ 5 V ± 5 %
V_{SS}	S	3	3	Negative power supply	− 5 V ± 5 %
GND	S	1	1	Ground	All analog and digital signals are referenced to this pin.
BCLK	I	16	12	Bit clock	Bit clock input used to shift PCM data into and out of the D_R and D_X pins. BCLK may vary from 64 kHz to 4.096 MHz in 8 kHz increments, and must be synchronous with MCLK.
MCLK	I	17	12	Master clock	Master clock input used by the switched capacitor filters and the encoder and decoder sequencing logic. Must be 512 kHz , 1.536/1.544 MHz, 2.048 MHz or 4.096 MHz and synchronous with BCLK.

TRANSMIT SECTION

FS_X	I	22	15	Transmit frame sync.	Normally a pulse or squarewave waveform with an 8 kHz repetition rate is applied to this input to define the start of the transmit time slot assigned to this device (non-delayed frame mode). or the start of the transmit frame (delayed frame mode using the internal time-slot assignment counter).
VF_XI	I	28	20	Transmit analog	This in a high-impedance input. Voice frequency signals present on this input are encoded as an A-law or μ-law PCM bit stream and shifted out on the selected D_X pin.
D_X0 D_X1	O O	18 19	13 –	Transmit Data	D_X1 is available on the TS5070 only, D_X0 is available on all devices. These Transmit Data TRI-STATE ® outputs remain in the high impedance state except during the assigned transmit time slot on the assigned port, during which the transmit PCM data byte is shifted out on the rising edges of BCLK.
$\overline{TS}_X0$ $\overline{TS}_X1$	O O	20 21	14 –	Transmit time slot	$\overline{TS}_X1$ is available on the TS5070 only. $\overline{TS}_X0$ is available on all devices. Normally these open-drain outputs are floating in a high impedance state except when a time-slot is active on one of the $D_X$outputs, when the appropriate $\overline{TS}_X$ output pulls low to enable a backplane line-driver.

RECEIVE SECTION

Name	Pin type	TS5070	TS5071	Function	Description
FS_R	I	8	6	Receive frame sync.	Normally a pulse or squarewave waveform with an 8 kHz repetition rate is applied to this input to define the start of the receive time slot assigned to this device (non-delayed frame mode), or the start of the receive frame (delayed frame mode using the internal time-slot assignment counter).
VF_RO	O	2	2	Receive analog	The Receive analog power amplifier output, capable of driving load impedances as low as 300 Ω (depending on the peak overload level required). PCM data received on the assigned D_R pin is decoded and appears at this output as voice frequency signals.
D_R0 D_R1	I I	10 9	7 –	Receive Data	D_R1 is available on the TS5070 only: D_R0 is available on all devices. These receive data input(s) are inactive except during the assigned receive time slot of the assigned port when the receive PCM data is shifted in on the falling edges of BCLK.

INTERFACE, CONTROL, RESET

IL5 IL4 IL3 IL2 IL1 IL0	I/O I/O I/O I/O I/O I/O	23 24 6 7 25 26	– 16 4 5 17 18	Interface Latches	IL5 through IL0 are available on the TS5070 IL4 through IL0 are available on the TS5071 Each Interface Latch I/O pin may be individually programmed as an input or an output determined by the state of the corresponding bit in the Latch Direction Register (LDR). For pins configured as inputs, the logic state sensed on each input is latched into the Interface Latch Register (ILR) whenever control data is written to COMBO IIG, while $\overline{CS}$ is low, and the information is shifted out on the CO (or CI/O) pin. When configured as outputs, control data written into the ILR appears at the corresponding IL pins.
CCLK	I	13	9	Control clock	This clock shifts serial control information into or out from CI/O when the $\overline{CS}$ input is low, depending on the current instruction CCLK may be asynchronous with the other system clocks.
CI/O	I/O	–	8	Control Data input/output	This is the Control Data I/O pin which is provided on the TS5071. Serial control information is shifted into or out from COMBO IIG on this pin when $\overline{CS}$ is low. The direction of the data is determined by the current instruction as defined in Table I.
CI CO	I O	12 11	– –	Control Data input Control Data output	These are separate controls, availables only on the TS5070. They can be wired together if required.
$\overline{CS}$	I	14	10	Chip select	When this pin is low, control information can be written into or out from COMBO IIG via the CI/O pin (or CI and CO).
MR	I	15	11	Master Reset	This logic input must be pulled low for normal operation of COMBO IIG. When pulled momentarily high, at least 1μ sec, all programmable registers in the device are reset to the states specified under "Power-On Initialization".

FUNCTIONAL DESCRIPTION

POWER-ON INITIALIZATION

When power is first applied, power-on reset circuitry initializes the COMBO IIG and puts it into the power-down state. The gain control registers for the transmit and receive gain sections are programmed for minimum gain, the hybrid balance circuit is turned off, the power amp is disabled and the device is in the non-delayed timing mode. The Latch Direction Register (LDR) is pre-set with all IL pins programmed as inputs, placing the SLIC interface pins in a high impedance state. The CI/O pin is set as an input ready for the first control byte of the initialization sequence.

A reset to these same initial conditions may also be forced by driving the MR pin momentarily high. This may be done either when powered-up or down. For normal operation this pin must be pulled low.

The desired modes for all programmable functions may be initialized via the control port prior to a Power-up command.

POWER-DOWN STATE

Following a period of activity in the powered-up state the power-down state may be re-entered by writing a Power-Down instruction into the serial control port as indicated in Table I. The power down instruction may be included within any other instruction code. It is recommended that the chip be powered down before executing any instructions. In the power-down state, all non-essential circuitry is de-activated and the D_X0 (and D_X1) outputs are in the high impedance TRI-STATE condition.

The coefficients stored in the Hybrid Balance circuit and the Gain Control registers, the data in the LDR and ILR, and all control bits remain unchanged in the power-down state unless changed by writing new data via the serial control port, which remains active. The outputs of the Interface Latches also remain active, maintaining the ability to monitor and control the SLIC.

TRANSMIT FILTER AND ENCODER

The Transmit section input, VF_XI, is a high impedance summing input which is used as the differencing point for the internal hybrid balance cancellation signal. No external components are necessary to set the gain. Following this circuit is a programmable gain/attenuation amplifier which is controlled by the contents of the Transmit Gain Register (see Programmable Functions section). An active pre-filter then precedes the 3rd order high-pass and 5th order low-pass switched capacitor filters. The A/D converter has a compressing characteristic according to the standard CCITT A or μ255 coding laws, which must be selected by a control instruction during initialization (see Tables I and II). A precision on-chip voltage reference ensures accurate and highly stable transmission levels. Any offset voltage arising in the gain-set amplifier, the filters or the comparator is canceled by an internal auto-zero circuit.

Each encode cycle begins immediately following the assigned Transmit time-slot. The total signal delay referenced to the start of the time-slot is approximately 165 μs (due to the Transmit Filter) plus 125 μs (due to encoding delay), which totals 290 μs. Data is shifted out on D_X0 or D_X1 during the selected time slot on eight rising edges of BCLK.

DECODER AND RECEIVE FILTER

PCM data is shifted into the Decoder's Receive PCM Register via the D_R0 or D_R1 pin during the selected time-slot on the 8 falling edges of BCLK. The Decoder consists of an expanding DAC with either A or μ255 law decoding characteristic, which is selected by the same control instruction used to select the Encode law during initialization. Following the Decoder is a 5th order low-pass switched capacitor filter with integral Sin x/x correction for the 8 kHz sample and hold. A programmable gain amplifier, which must be set by writing to the Receive Gain Register, is included, and finally a Post-Filter/Power Amplifier capable of driving a 300 Ω load to $\pm$ 3.5 V, a 600 Ω load to $\pm$ 3.8 V or a 15 kΩ load to $\pm$ 4.0 V at peak overload.

A decode cycle begins immediately after each receive time-slot, and 10 μs later the Decoder DAC output is updated. The total signal delay is 10 μs plus 120 μs (filter delay) plus 62.5 μs (1/2 frame) which gives approximately 190 μs.

PCM INTERFACE

The FS_X and FS_R frame sync inputs determine the beginning of the 8-bit transmit and receive time-slots respectively. They may have any duration from a single cycle of BCLK to a square wave. Two different relationships may be established between the frame sync inputs and the actual time-slots on the PCM busses by setting bit 3 in the Control Register (see Table II). Non-delayed data mode is similar to long-frame timing on the ETC 5050/60 series of devices: time-slots being nominally coincident with the rising edge of the appropriate FS input. The alternative is to use Delayed Data mode which is similar to short-frame sync timing , in which each FS input must be high at least a half-cycle of BCLK earlier than the time - slot. The Time-Slot Assignment circuit on the device can only be used with Delayed Data timing. When using Time -Slot Assignment, the beginning of the first time-slot in a frame is identified by the appropriate FS input. The actual transmit and receive time-slots are then determined by the internal Time-Slot Assignment counters.

Transmit and Receive frames and time-slots may be skewed from each other by any number of BCLK cycles During each assigned Transmit time-slot, the selected $D_X0/1$ output shifts data out from the PCM register on the rising edges of BCLK. $\overline{TS}_X0$ (or $\overline{TS}_X1$ as appropriate) also pulls low for the first 7 1/2 bit times of the time-slot to control the TRI-STATE Enable of a backplane line-driver. Serial PCM data is shifted into the selected $D_R0/1$ input during each assigned Receive time-slot on the falling edges of BCLK. D_X0 or D_X1 and D_R0 or D_R1 are selectable on the TS5070 only.

SERIAL CONTROL PORT

Control information and data are written into or read-back from COMBO IIG via the serial control port consisting of the control clock CCLK; the serial data input/output. CI/O, (or separate input, CI, and output, CO, on the TS5070 only); and the Chip Select input, $\overline{CS}$. All control instructions require 2 bytes, as listed in Table I, with the exception of a single byte power-up/down command.

To shift control data into COMBO IIG, CCLK must be pulsed high 8 times while $\overline{CS}$ is low. Data on the CI/O (or CI) input is shifted into the serial input register on the falling edge of each CCLK pulse. After all data is shifted in, the contents of the input shift register are decoded, and may indicate that a 2nd byte of control data will follow. This second byte may either be defined by a second byte-wide $\overline{CS}$ pulse or may follow the first contiguously, i. e. it is not mandatory for $\overline{CS}$ to return high in between the first and second control bytes. At the end of CCLK8 in the 2nd control byte the data is loaded into the appropriate programmable register. $\overline{CS}$ may remain low continuously when programming successive registers, if desired. However, $\overline{CS}$ should be set high when no data transfers are in progress.

To readback interface Latch data or status information

from COMBO IIG, the first byte of the appropriate instruction is strobed in during the first $\overline{CS}$ pulse, as defined in Table I. $\overline{CS}$ must then be taken low for a further 8 CCLK cycles, during which the data is shifted onto the CO or CI/O pin on the rising edges of CCLK. When CS is high the CO or CI/O pin is in the high-impedance TRI-STATE, enabling the CI/O pins of many devices to be multiplexed together.

Thus, to summarize, 2-byte READ and WRITE instructions may use either two 8-bit wide $\overline{CS}$ pulses or a single 16-bit wide $\overline{CS}$ pulse.

Function	Byte 1 (Note 1)								Byte 2 (Note 1)							
	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Single Byte Power-Up/Down	P	X	X	X	X	X	0	X	None							
Write Control Register	P	0	0	0	0	0	1	X	See Table II							
Read-Back Control Register	P	0	0	0	0	1	1	X	See Table II							
Write to Interface Latch Register	P	0	0	0	1	0	1	X	See Table V							
Read Interface Latch Register	P	0	0	0	1	1	1	X	See Table V							
Write Latch Direction Register	P	0	0	1	0	0	1	X	See Table IV							
Read Latch Direction Register	P	0	0	1	0	1	1	X	See Table IV							
Write Receive Gain Register	P	0	1	0	0	0	1	X	See Table VIII							
Read Receive Gain Register	P	0	1	0	0	1	1	X	See Table VIII							
Write Transmit Gain Register	P	0	1	0	1	0	1	X	See Table VII							
Read Transmit Gain Register	P	0	1	0	1	1	1	X	See Table VII							
Write Receive Time-Slot/Port	P	1	0	0	1	0	1	X	See Table VI							
Read-Back Receive Time-Slot/Port	P	1	0	0	1	1	1	X	See Table VI							
Write Transmit Time-Slot/Port	P	1	0	1	0	0	1	X	See Table VI							
Read-Back Transmit Time-Slot/Port	P	1	0	1	0	1	1	X	See Table VI							

Note 1 : Bit 7 of bytes 1 and 2 is always the first bit clocked into or out from the CI, CO or CI/CO pin. X = don't care.
Note 2 : "P" is the power-up/down control bit, see "Power-up" section ("0" =Power Up "1" =Power Down)
Note 3 : 3 additional registers are provided for the Hybrid Balance Filter, see page 9.

TABLE I - Programmable Register Instructions

PROGRAMMABLE FUNCTIONS

POWER-UP/DOWN CONTROL

Following power-on initialization, power-up and power-down control may be accomplished by writing any of the control instructions listed in Table I into COMBO IIG with the "P" bit set to "0" for power-up or "1" for power-down. Normally it is recommended that all programmable functions be initially programmed while the device is powered down. Power state control can then be included with the last programming instruction or the separate single-byte instruction. Any of the programmable registers may also be modified while the device is powered-up or down be setting the "P" bit as indicated. When the power up or down control is entered as a single byte instruction, Bit one (1) must be reset to a 0.

When a power-up command is given, all de-activated circuits are activated, but the TRI-STATE PCM output(s), D_X0 (and D_X1), will remain in the high impedance state until the second FS_X pulse after power-up.

CONTROL REGISTER INSTRUCTION

The first byte of a READ or WRITE instruction to the Control Register is as shown in Table I. The second byte functions are detailed in Table II.

MASTER CLOCK FREQUENCY SELECTION

A Master clock must be provided to COMBO IIG for operation of the filter and coding/decoding functions. The MCLK frequency must be either 512 kHz, 1.536 MHz, 1.544 MHz, 2.048 MHz, or 4.096 MHz and must be synchronous with BCLK. Bits F_1 and F_0 (see Table II) must be set during initialization to select the correct internal divider.

CODING LAW SELECTION

Bits "MA" and "IA" in Table II permit the selection of μ255 coding or A-law coding, with or without even bit inversion.

ANALOG LOOPBACK

Analog Loopback mode is entered by setting the "AL" and "DL" bits in the Control Register as shown in Table II. In the analog loopback mode, the Transmit input VF_XI is isolated from the input pin and internally connected to the VF_RO output, forming a loop from the Receive PCM Register back to the Transmit PCM Register. The VF_RO pin remains active, and the programmed settings of the Transmit and Receive gains remain unchanged, thus care must be taken to ensure that overload levels are not exceeded anywhere in the loop.

DIGITAL LOOPBACK

Digital Loopback mode is entered by setting the "AL" and "DL" bits in the Control Register as shown in Table II. This mode provides another stage of path verification by enabling data written into the Receive PCM Register to be read back from that register in any Transmit time-

Bit Number								Function
7	6	5	4	3	2	1	0	
F_1	F_0	MA	IA	DN	DL	AL	PP	
0 0 1 1	0 1 0 1							MCLK = 512 kHz MCLK = 1.536 or 1.544 MHz MCLK = 2.048 MHz* MCLK = 4.096 MHz
		0 1 1	X 0 1					Select μ - 255 law* A-law, Including Even Bit Inversion A-law, No Even Bit Inversion
				0 1				Delayed Data Timing Non-Delayed Data Timing *
					0 1 0	0 X 1		Normal Operation * Digital Loopback Analog Loopback
							0 1	Power Amp Enabled in PDN Power Amp Disabled in PDN *

* = State at power-on initialization.

TABLE II - Control Register Byte 2 Functions

	μ255 law MSB LSB	True A-law with even bit inversion MSB LSB	A-law without even bit inversion MSB LSB
V_{IN} = + Full Scale	1 0 0 0 0 0 0 0	1 0 1 0 1 0 1 0	1 1 1 1 1 1 1 1
V_{IN} = 0V	1 1 1 1 1 1 1 1 0 1 1 1 1 1 1 1	1 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1	1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
V_{IN} = − Full Scale	0 0 0 0 0 0 0 0	0 0 1 0 1 0 1 0	0 1 1 1 1 1 1 1

Note 1 : The MSB is always the first PCM bit shifted in or out of COMBO IIG

TABLE III - Coding Law Conventions

Byte 2 Bit Number							
7	6	5	4	3	2	1	0
L_0	L_1	L_2	L_3	L_4	L_5	X	X

L_n Bit	IL Direction
0	Input
1	Output

X = don't care.

TABLE IV - Byte 2 Functions of Latch Direction Register

slot at $D_X0/1$. No PCM decoding or encoding takes place in this mode, VF_RO maintains a low impedance idle output.

INTERFACE LATCH DIRECTIONS

Immediately following power-on, all Interface Latches assume they are inputs, and therefore all IL pins are in a high impedance state. Each IL pin may be individually programmed as a logic input or output by writing the appropriate instruction to the LDR, see Tables I and IV.

Bits L_5–L_0 must be set by writing the specified instruction to the LDR with the L bits in the second byte set as specified in Table IV.

INTERFACE LATCH STATES

Interface Latches configured as outputs assume the state determined by the appropriate data bit in the 2-byte instruction written to the Interface Latch Register (ILR) as shown in Tables I and V. Latches configured as inputs will sense the state applied by an external source, such as the Off-Hook detect output of a SLIC. All bits of the ILR, i.e. sensed inputs and the programmed state of outputs, can be read back in the 2nd byte of a READ from the ILR.

It is recommended that, during initialization, the state of IL pins to be configured as outputs should first be programmed, followed immediately by the Latch Direction Register.

Bit Number							
7	6	5	4	3	2	1	0
D_0	D_1	D_2	D_3	D_4	D_5	X	X

TABLE V - Interface Latch Data Bit Order

TIME-SLOT ASSIGNMENT

COMBO IIG can operate in either fixed time-slot or time-slot assignment mode for selecting the Transmit and Receive PCM time-slots. Following power-on, the device is automatically in Non-Delayed Timing mode, in which the time-slot always begins with the leading (rising) edge of frame sync inputs FS_X and FS_R Time-Slot Assignment may only be used with Delayed Data timing : see Figure 5. FS_X and FS_R may have any phase relation ship with each other in BCLK period movements.

Alternatively, the internal time-slot assignment counters and comparators can be used to access any time-slot in a frame, using the frame sync inputs as marker pulses for the beginning of transmit and receive time-slot 0. In this mode, a frame may consist of up to 64 time-slots of 8 bits each. A time-slot is assigned by a 2-byte instruction as shown in Tables I and VI. The last 6 bits of the second byte indicate the selected time-slot from 0-63 using straight binary notation. A new assignment becomes active on the second frame following the end of the Chip-Select for the second control byte. The "EN" bit allows the PCM inputs, $D_R0/1$, or outputs, $D_X0/1$, as appropriate, to be enabled or disabled.

Time-Slot Assignment mode requires that the FS_X and FS_R pulses must conform to the delayed timing format shown in Figure 5.

Bit Number								Function
7 EN	6 PS (Note 1)	5 T_5 (Note 2)	4 T_4	3 T_3	2 T_2	1 T_1	0 T_0	
0	0	X	X	X	X	X	X	Disable D_X0 Output (Transmit Instruction) Disable D_R0 Input (Receive Instruction)
0	1	X	X	X	X	X	X	Disable D_X1 Output (Transmit Instruction) Disable D_R1 Input (Receive Instruction)
1	0	Assign One Binary Coded Time-Slot from 0-63 Assign One Binary Coded Time-Slot from 0-63						Enable D_X0 Output (Transmit Instruction) Enable D_R0 Input (Receive Instruction)
1	1	Assign One Binary Coded Time-Slot from 0-63 Assign One Binary Coded Time-Slot from 0-63						Enable D_X1 Output (Transmit Instruction) Enable D_R1 Input (Receive Instruction)

Note 1: The "PS" bit MUST always be set to 0 for the TS5071
Note 2: T5 is the MSB of the Time-slot assignment.

TABLE VI - Time-Slot and Port Assignment instruction

PORT SELECTION

On the TS5070 only, an additional capability is available : 2 Transmit serial PCM ports, D_X0 and D_X1, and 2 Receive serial PCM ports, D_R0 and D_R1, are provided to enable two-way space switching to be implemented. Port selections for transmit and receive are made within the appropriate time-slot assignment instruction using the "PS" bit in the second byte. Port Selection may only be used in Delayed Data timing mode.

On the TS5071, only ports D_X0 and D_R0 are available, therefore the "PS" bit MUST always be set to 0 for these devices.

Tabel VI shows the format for the second byte of both transmit and receive time-slot and port assignment instructions.

TRANSMIT GAIN INSTRUCTION BYTE 2

The transmit gain can be programmed in 0.1 dB steps by writing to the Transmit Gain Register as defined in Tables I and VII. This corresponds to a range of 0 dBm0 levels at VF_XI between 1.619 Vrms and 0.087 Vrms (equivalent to + 6.4 dBm to − 19.0 dBm in 600 Ω). To calculate the binary code for byte 2 of this instruction for any desired input 0 dBm0 level in Vrms, take the nearest integer to the decimal number given by:

$$200 \times \log_{10} (V/0.08595)$$

and convert to the binary equivalent. Some examples are given in Table VII.

Bit Number 7 6 5 4 3 2 1 0	0 dBm0 Test Level (Vrms) at VF_X1
0 0 0 0 0 0 0 0	No Output
0 0 0 0 0 0 0 1	0.087
0 0 0 0 0 0 1 0	0.088
1 1 1 1 1 1 1 0	1.600
1 1 1 1 1 1 1 1	1.619

TABLE VII - Byte 2 of Transmit Gain Instructions

RECEIVE GAIN INSTRUCTION BYTE 2

The receive gain can be programmed in 0.1 dB steps by writing to the Receive Gain Register as defined in Tables I and VIII. Note the following restrictions on output drive capability:

a) 0 dBm0 levels ≤ 1.96 Vrms at VF_RO may be driven into a load of ≥15 kΩ to GND,
b) 0 dBm0 levels ≤ 1.90 Vrms at VF_RO may be driven into a load of ≥600 Ω to GND,
c) 0 dBm0 levels ≤ 1.70 Vrms at VF_RO may be driven into a load of ≥ 300 Ω to GND.

To calculate the binary code for byte 2 of this instruction for any desired output 0 dBm0 level in Vrms, take the nearest integer to the decimal number given by:

$$200 \times \log_{10} (V/0.1046)$$

and convert to the binary equivalent. Some examples are given in Table VIII.

Bit Number 7	6	5	4	3	2	1	0	0 dBm0 Test Level (Vrms) at VF_RO
0	0	0	0	0	0	0	0	No Output (Low Z to GND)
0	0	0	0	0	0	0	1	0.106
0	0	0	0	0	0	1	0	0.107
1	1	1	1	1	1	1	0	1.95
1	1	1	1	1	1	1	1	1.96

TABLE VIII - Byte 2 of Receive Gain Instructions

HYBRID BALANCE FILTER

The Hybrid Balance Filter on COMBO II is a programmable filter consisting of a second-order Bi-Quad section, Hybal1, followed by a first-order section, Hybal2, and a programmable attenuator. Either of the filter sections can be bypassed if only one is required to achieve good cancellation. A selectable 180 degree inverting stage is included to compensate for interface circuits which also invert the transmit input relative to the receive output signal. The Bi-quad is intended mainly to balance low frequency signals across a transformer SLIC, and the first order section to balance midrange to higher audio frequency signals.

As a Bi-Quad, Hybal1 has a pair of low frequency zeroes and a pair of complex conjugate poles. When configuring the Bi-Quad, matching the phase of the hybrid at low to midband frequencies is most critical. Once the echo path is correctly balanced in phase, the magnitude of the cancellation signal can be corrected by the programmable attenuator.

The Bi-Quad mode of Hybal1 is most suitable for balancing interfaces with transformers having high inductance of 1.5 Henries or more. An alternative configuration for smaller transformers is available by converting Hybal1 to a simple first-order section with a single real low frequency pole and 0 Hz zero. In this mode, the pole frequency may be programmed.

Many line interfaces can be adequately balanced by use of the Hybal1 section only, in which case the Hybal2 filter should be de-selected to bypass it.

Hybal2, the higher frequency first-order section, is provided for balancing an electronic SLIC, and is also helpful with a transformer SLIC in providing additional phase correction for mid and high-band frequencies, typically 1 kHz to 3.4 kHz. Such a correction is particularly useful if the test balance impedance includes a capacitor of 100 nF or less, such as the loaded and non-loaded loop test networks in the United States. Independent placement of the pole and zero location is provided.

Figure 1 shows a simplified diagram of the local echo path for a typical application with a transformer interface. The magnitude and phase of the local echo signal, measured at VF_XI are a function of the termination impedance Z_T, the line transformer and the impedance of the 2W loop, Z_L. If the impedance reflected back into the transformer primary is expressed as Z_L' then the echo path transfer function from VF_RO to VF_XI is :

$$H(w) = Z_L'/(Z_T + Z_L') \qquad (1)$$

PROGRAMMING THE FILTER

On initial power-up the Hybrid Balance filter is disabled. Before the hybrid balance filter can be programmed it is necessary to design the transformer and termination impedance in order to meet system 2W input return loss specifications, which are normally measured against a fixed test impedance (600 or 900 Ω in most countries). Only then can the echo path be modeled and the hybrid balance filter programmed. Hybrid balancing is also measured against a fixed test impedance, specified by each national Telecom administration to provide adequate control of talker and listener echo over the majority of their network connections. This test impedance is Z_L in Figure 1. The echo signal and the degree of transhybrid loss obtained by the programmable filter must be measured from the PCM digital input, D_RO, to the PCM digital output, D_XO, either by digital test signal analysis or by conversion back to analog by a PCM CODEC/Filter.

Three registers must be programmed in COMBO IIG to fully configure the Hybrid Balance Filter as follows:

Register 1:	select/de-select Hybrid Balance Filter invert/non–invert cancellation signal select/de-select Hybal2 filter section attenuator setting
Register 2:	select/de-select Hybal1 filter set Hybal1 to Bi-quad or 1st order pole and zero frequency selection
Register 3:	program pole frequency in Hybal2 filter program zero frequency in Hybal2 filter

Standard filter design techniques may be used to model the echo path (see Equation 1) and design a matching hybrid balance filter configuration. Alternatively, the frequency response of the echo path can be measured and the hybrid balance filter designed to replicate it.

A Hybrid Balance filter design guide and software optimization program are available under license from THOMSON SEMICONDUCTEURS (order TS5077).

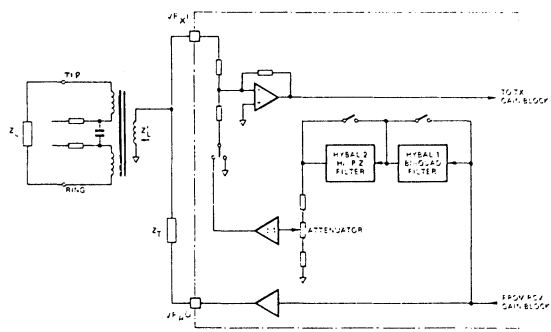


FIGURE 1 - SIMPLIFIED DIAGRAM OF HYBRID BALANCE CIRCUIT

APPLICATIONS INFORMATIONS

Figure 2 shows a typical application of the TS5071 together with a transformer-based SLIC.
Four of the IL latches are configured as outputs to control the relay drivers on the SLIC, while IL4 is an input for the Supervision signal. Figure 3 shows a similar arrangement with a monolithic SLIC.

POWER SUPPLIES

While the pins of the TS5070 COMBO IIG devices are well protected against electrical misuse, it is recommended that the standard CMOS practice of applying GND to the device before any other connections are made should always be followed. In applications where the printed circuit card may be plugged into a hot socket with power and clocks already present, an extra long ground pin on the connector should be used.
To minimize noise sources all ground connections to each device should meet at a common point as close as possible to the GND pin in order to prevent the interaction of ground return currents flowing through a common bus impedance. Power supply decoupling capacitors of 0.1 μF should be connected from this common point to V_{CC} and V_{SS} as close to the device pins as possible.

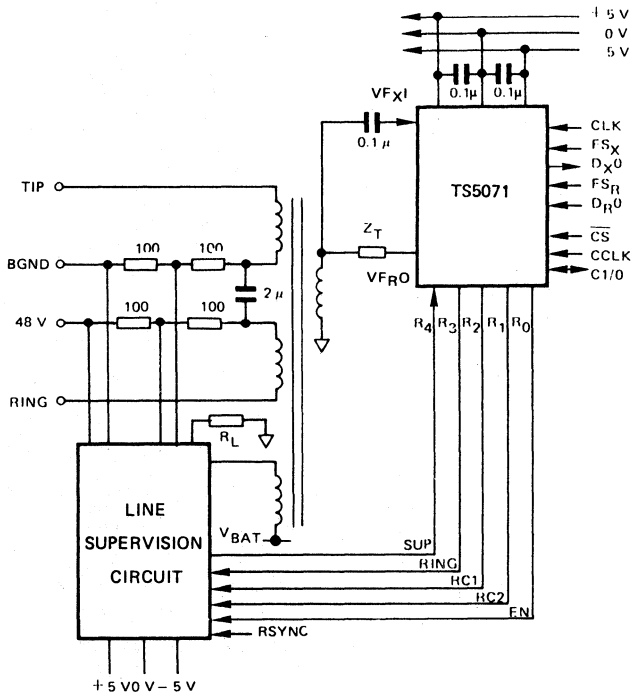


FIGURE 2 - TYPICAL APPLICATION WITH TRANSFORMER SLIC

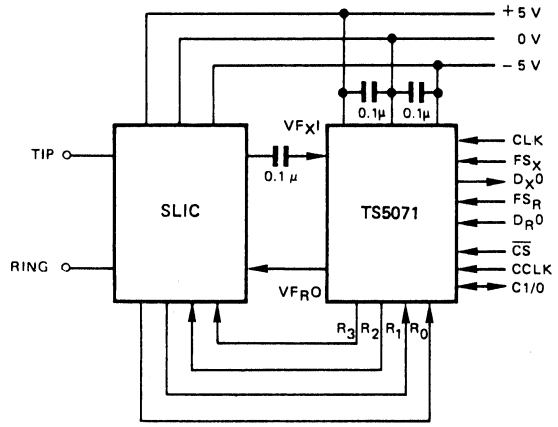


FIGURE 3 - TYPICAL APPLICATION WITH MONOLITHIC SLIC

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
V_{CC} to GND	V_{CC}	+ 7	V
V_{SS} to GND	V_{SS}	– 7	V
Voltage at VF_XI		V_{CC} + 1 to V_{SS} – 1	V
Voltage at any digital input	V_{IN}	V_{CC} + 1 to GND – 1	V
Current at VF_RO		± 100	mA
Current at any digital output	I_O	± 50	mA
Storage temperature range	T_{stg}	– 65, + 150	°C
Lead temperature (soldering, 10 seconds)	T_{lead}	300	°C

ELECTRICAL OPERATING CHARACTERISTICS

Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for V_{CC} = + 5 V ± 5 %; V_{SS} = − 5V ± 5%, T_A = 0°C to 70°C by correlation with 100 % electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. All signals referenced to GND. Typicals specified at V_{CC} = + 5V, V_{SS} = − 5V, T_A = 25°C.
All timing parameters are measured at V_{OH} = 2.0 V and V_{OL} = 0.7 V.
See Definitions and Timing Conventions section for test methods information.

DIGITAL INTERFACE

Characteristic		Symbol	Min	Typ	Max	Unit
Input low voltage	All digital inputs (DC Meas.)	V_{IL}			0.7	V
Input high voltage	All digital inputs (DC Meas.)	V_{IH}	2.0			
Output low voltage	D_X0 and D_X1, IL = 3.2 mA All other Digital outputs, IL = 1 mA	V_{OL}			0.4	V
Output high voltage	D_X0 and D_X1, IL = − 3.2 mA All other Digital outputs except ($\overline{TS}_X$), IL = − 1 mA All digital outputs, I_L = − 100 µA	V_{OH}	2.4 V_{CC} − 0.5			V V
Input low current all digital inputs (GND < V_{IN} < V_{IL})		I_{IL}	− 10		10	µA
Input high current all digital inputs (V_{IH} < V_{IN} < V_{CC})		I_{IH}	− 10		10	µA
Output current in high impedance state (TRI-STATE) D_X0, D_X1, CO and CI/O (as an Output) I_L5 - IL0 as outputs (GND < V_O < V_{CC})		I_{OZ}	− 10		10	µA

ANALOG INTERFACE

Input current VVF_XI (− 3.3 V < VF_XI < 3.3 V)	I_{VFXI}	− 10		10	µA
Input resistance (− 3.3 V < VF_XI < 3.3 V)	R_{VFXI}	390			kΩ
Input Offset Voltage at VF_XI	VOS_X			20	mV
Load resistance (VF_RO) (− 3.5 V < VF_RO < 3.5 V)	RL_{VFRO}	300			Ω
Load capitance CL_{VFRO} from VF_RO to GND $RL_{VFRO} \geq 300\Omega$	CL_{VFRO}			200	pF
Output resistance (steady zero PCM code applied to D_R0 or D_R1)	RO_{VFRO}		1.0	3.0	Ω
Output offset voltage at VF_RO (Alterning ± zero PCM code applied to D_R0 or D_R1, maximum receive Gain)	V_{OSR}	− 200		200	mV

POWER DISSIPATION

Power down current (CCLK, CI/O, CI, CO = 0.4 V, $\overline{CS}$ = 2.4 V Interface latches set as outputs with no load All other inputs active, Power Amp disabled)	$I_{CC}0$			1.5	mA
Power down current (as above)	$-I_{SS}0$			0.3	mA
Power up current (CCLK, CI/O, CI, CO = 0.4, $\overline{CS}$ = 2.4 V No load on Power Amp Interface latches set as outputs with no load)	$I_{CC}1$		7	10	mA
Power up current (as above)	$-I_{SS}1$		7	10	mA

TIMING SPECIFICATIONS

Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for V_{CC} = + 5 V ± 5 %; V_{SS} = − 5V ± 5%, T_A = 0°C to 70°C by correlation with 100 % electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. All signals referenced to GND. Typicals specified at V_{CC} = + 5V, V_{SS} = − 5V, T_A = 25°C.

All timing parameters are measured at V_{OH} = 2.0 V and V_{OL} = 0.7 V.

See Definitions and Timing Conventions section for test methods information.

MASTER CLOCK TIMING

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency of MCLK (Selection of Frequency is Programmable) (See Table III)	f_{MCLK}		**512** 1.536 1.544 2.048 **4.096**		kHz MHz MHz MHz MHz
Period of MCLK High (Measured from V_{IH} to V_{IH}, see Note)	t_{WMH}	**80**			ns
Period of MCLK Low (Measured from V_{IL} to V_{IL},see Note)	t_{WML}	**80**			ns
Rise Time of MCLK (Measured from V_{IL} to V_{IH})	t_{RM}			30	ns
Fall Time of MCLK (Measured from V_{IH} to V_{IL})	t_{FM}			30	ns
HOLD Time, BCLK low to MCLK high (TS5070 Only)	t_{HBM}	**50**			ns

PCM INTERFACE TIMING

Frequency of BCLK (May Vary from 64 kHz to 4.096 MHz in 8 kHz increments)	f_{BCLK}	**64**		**4096**	kHz
Period of BCLK High (Measured from V_{IH} to V_{IH})	t_{WBH}	**80**			ns
Period of BCLK Low (Measured from V_{IL} to V_{IL})	t_{WBL}	**80**			ns
Rise Time of BCLK (Measured from V_{IL} to V_{IH})	t_{RB}			30	ns
Fall Time of BCLK (Measured from V_{IH} to V_{IL})	t_{FB}			30	ns
Hold Time, BCLK Low to $FS_{X/R}$ High or Low	t_{HBF}	**0**			ns
Setup Time , $FS_{X/R}$ High to BCLK Low	t_{SFB}	**30**			ns
Delay Time, BCLK High to Data Valid (Load = 100 pF Plus 2 LSTTL Loads)	t_{DBD}			**80**	ns
Delay Time, BCLK Low to D_X0/1 Disabled (Applies to the later Edge in Non-Delayed Data Mode only)	t_{DBZ}	**15**		**80**	ns
Delay Time, BCLK High to $\overline{TS}_X$ Low if FS_X High, or FS_X High to $\overline{TS}_X$ Low if BCLK High (Load =100pF plus 2 LSTTL Loads)	t_{DBT}			60	ns
TRI-STATE Time, BCLK Low to $\overline{TS}_X$ High if FS_X Low, or BCLK High to $\overline{TS}_X$ High if FS_X High	t_{ZBT}	15		60	ns
Delay Time, $FS_{X/R}$ High to Data Valid (Load = 100 pF Plus 2 LSTTL Loads, Applies if $FS_{X/R}$ Rises Later than BCLK Rising Edge in Non-Delayed Data Mode Only)	t_{DFD}			**80**	ns
Setup Time, D_R0/1 Valid to BCLK Low	t_{SDB}	**30**			ns
Hold Time, BCLK Low to D_R0/1 invalid	t_{HBD}	**10**			ns

NOTE : Applies only to MCLK frequencies ≥ 1.536 MHz. At 512 kHz a 50:50 ± 2% duty cycle must be used

SERIAL CONTROL PORT TIMING

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency of CCLK	f_{CCLK}			2.048	MHz
Period of CCLK High (Measured from V_{IH} to V_{IH})	t_{WCH}	160			ns
Period of CCLK Low (Measured from V_{IL} to V_{IL})	t_{WCL}	160			ns
Rise Time of CCLK (Measured from V_{IL} to V_{IH})	t_{RC}			50	ns
Fall Time of CCLK (Measured from V_{IH} to V_{IL})	t_{FC}			50	ns
Hold Time, CCLK Low to $\overline{CS}$ Low (CCLK1)	t_{HCS}	10			ns
Hold Time, CCLK Low to $\overline{CS}$ High (CCLK8)	t_{HSC}	100			ns
Setup Time, $\overline{CS}$ Transition to CCLK Low	t_{SSC}	50			ns
Setup Time, CI (CI/O) Data in to CCLK Low	t_{SDC}	50			ns
Hold Time, CCLK Low to CI/O Invalid	t_{HCD}	50			ns
Delay Time, CCLK High to CI/O Data Out Valid (Load = 100pF plus 2 LSTTL Loads)	t_{DCD}			50	ns
Delay Time, $\overline{CS}$ Low to CO (CI/O) Valid (Applies Only if Separate $\overline{CS}$ used for Byte 2)	t_{DSD}			50	ns
Delay Time, $\overline{CS}$ High to CO (CI/O) High impedance (Applies only when $\overline{CS}$ High occurs before 9th CCLK High)	t_{DDZ}	15		60	ns
Hold Time, 8th CCLK Low to $\overline{CS}$ High	t_{HSC}	100			ns

INTERFACE LATCH TIMING

Setup Time, IL to CCLK 8 of Byte 1 (Interface Latch Inputs Only)	t_{SLC}	100			ns
Hold Time, IL Valid from 8th CCLK Low (Byte 1)	t_{HCL}	50			ns
Delay Time, CCLK 8 of Byte 2 to IL (Interface Latch Outputs Only C_L = 50 pF)	t_{DCL}			200	ns

MASTER RESET PIN

Duration of Master Reset High	t_{WMR}	1			µs

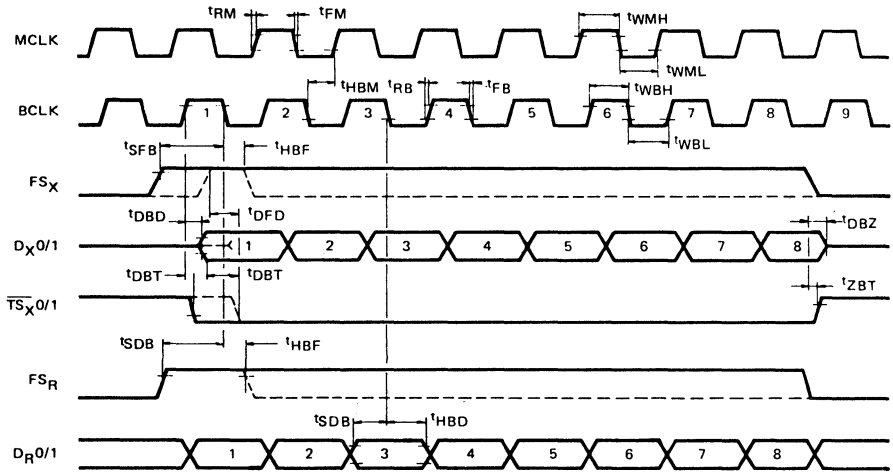


FIGURE 4 – NON DELAYED DATA TIMING

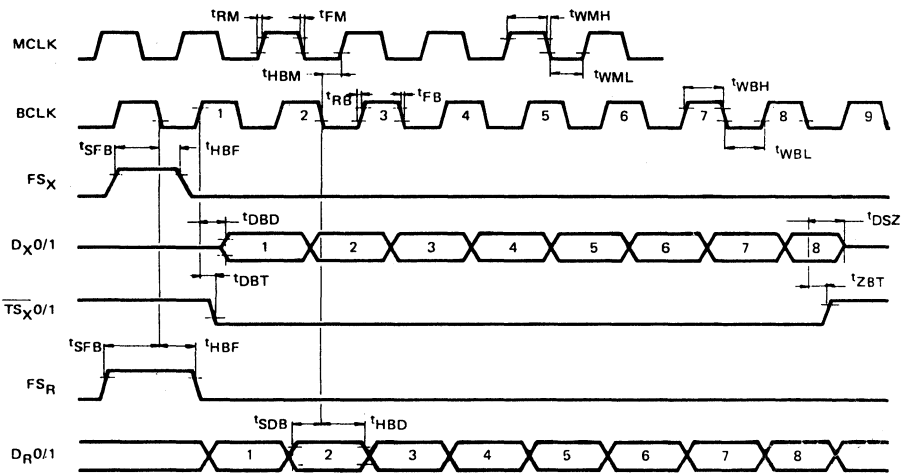


FIGURE 5 - DELAYED DATA TIMING

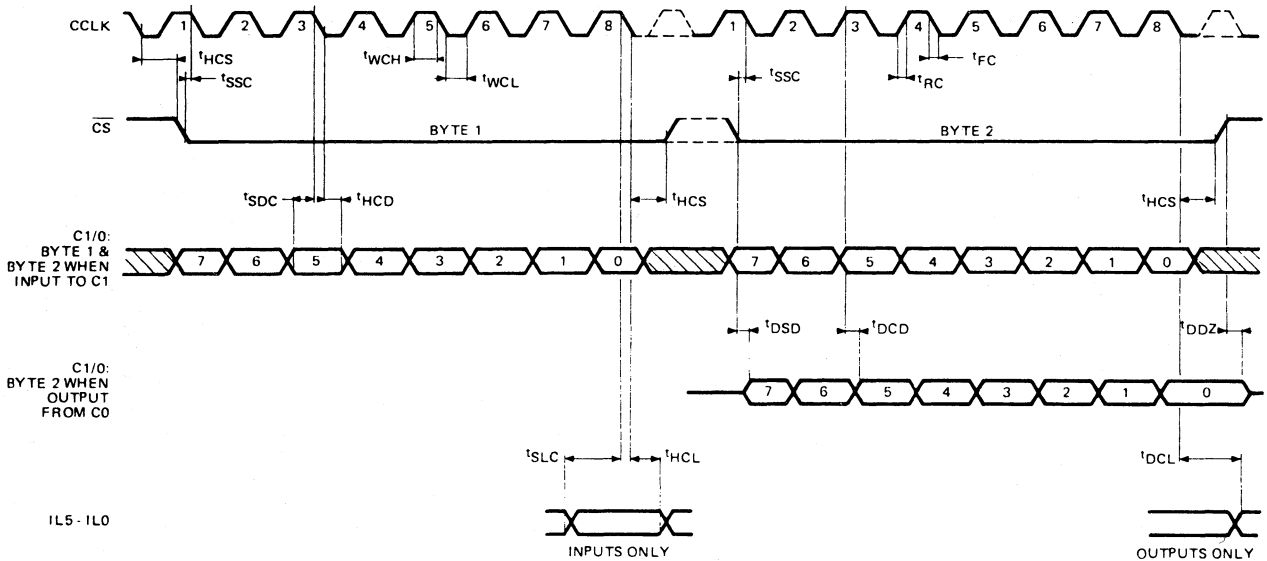


FIGURE 6 - CONTROL PORT TIMING

TRANSMISSION CHARACTERISTICS

Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for V_{CC} = + 5V ± 5 %, V_{SS} = − 5V ± 5 %, T_A = 0°C to 70°C by correlation with 100 % electrical testing at T_A = 25°C. f = 1015.625 Hz, VF_XI = 0 dBm0, D_R0 or D_R1 = 0 dBm PCM code. All other limits are assured by correlation with other production tests and/or product design and characterization. All signals referenced to GND. Typicals specified at V_{CC} = + 5V, V_{SS} = − 5V, T_A = 25°C.

AMPLITUDE RESPONSE

Characteristic	Symbol	Min	Typ	Max	Unit
Absolute levels					
The Maximum 0 dBm0 Levels are:					
VF_XI			1.619		Vrms
VF_RO (15 kΩ Load)			1.963		Vrms
The Minimum 0 dBm0 Levels are:					
VF_XI			87.0		mVms
VF_RO (Any Load > 300 Ω)			106.0		mVms
Maximum Overload					
The Nominal Overload Levels are:	T_{max}				
VF_XI – A-law			2.33		Vrms
μ-law			2.33		Vrms
VF_RO – A-law (600 Ω Load)			2.73		Vrms
μ-law (600 Ω Load)			2.73		Vrms
The Maximum Overload Levels are:					
VF_XI – A-law			2.32		Vrms
μ-law			2.33		Vrms
VF_RO – A-law (150 kΩ Load)			2.82		Vrms
μ-law (150 kΩ Load)			2.83		Vrms
The Minimum Overload Levels are:					
VF_XI - A-law			124.9		mVrms
μ-law			125.3		mVrms
VF_RO – A-law (Any Load > 300 Ω)			152.2		mVrms
μ-law (Any Load > 300 Ω)			152.7		mVrms
Transmit Gain Absolute Accurary	G_{XA}				
Transmit Gain Programmed for Maximum 0 dBm0 Test Level Measure Deviation of Digital Code from Ideal 0 dBm0 PCM Code at $D_x0/1$. T_A = 25°C, V_{CC} = 5V, V_{SS} = − 5V		**− 0.15**		**0.15**	dB
Transmit Gain Variation with Programmed Gain	G_{XAG}				
Measure Transmit Gain Over the Range from Maximum to Minimum Calculate the Deviation from the Programmed Gain Relative to G_{XA} i.e., $G_{XAG} = G_{actual} - G_{prog} - G_{XA}$ T_A = 25°C, V_{CC} = 5V, V_{SS} = − 5 V		**− 0.1**		**0.1**	dB

AMPLITUDE RESPONSE (continued)

Characteristic	Symbol	Min	Typ	Max	Unit
Transmit Gain **Variation with Frequency** Relative to 1015.625 Hz, (Note 4) Minimum Gain $< G_X <$ Maximum Gain $D_{R}0$ (or $D_{R}1$) = 0 dBm0 Code	G_{XAF}				
f = 60 Hz				- 26	dB
f = 200 Hz		- 1.8		- 0.1	dB
f = 300 Hz to 3000 Hz		- 0.15		0.15	dB
f = 3400 Hz		- 0.7		0.0	dB
f = 4000 Hz				14	dB
f ≥ 4600 Hz Measure Response at Alias Frequency from 0 kHz to 4 kHz G_X = 0 dB, VF_XI = 1.619 Vrms $D_{R}0$ or $D_{R}1$ = 0 dBm0 Code (Note 4)				32	dB
f = 62.5 Hz				- 24.9	dB
f = 203.125 Hz		- 1.7		- 0.1	dB
f = 296.875 Hz		- 0.15		0.15	dB
f = 515.625 Hz		- 0.15		0.15	dB
f = 2796.875 Hz		- 0.15		0.15	dB
f = 3015.625 Hz		- 0.15		0.15	dB
f = 3406.250 Hz		- 0.7		0.0	dB
f = 3984.375 Hz				- 13.5	dB
f = 4593.750 Hz, Measure 3406.25 Hz				- 32	dB
f = 5015.625 Hz, Measure 2984.375 Hz				- 32	dB
f = 10015.625 Hz, Measure 2015.625 Hz				- 32	dB
Transmit Gain **Variation with Temperature** Measured Relative to G_{XA}, V_{CC} = 5 V, V_{SS} = - 5V Minimum gain $< G_X <$ Maximum Gain	G_{XAT}	- 0.1		0.1	dB
Transmit Gain **Variation with Supply** V_{CC} = 5 V ± 5%, V_{SS} = - 5 V ± 5% Measured Relative to G_{XA} T_A = 25°C, G_X = Maximum Gain	G_{XAV}	- 0.05		0.05	dB
Transmit Gain **Variation with Signal level** Sinusoidal Test Method Reference Level = 0 dBm0 VF_XI = - 40 dBm0 to + 3 dBm0 VF_XI = - 50 dBm0 to - 40 dBm0 VF_XI = - 55 dBm0 to - 50 dBm0	G_{XAL}	 - 0.2 - 0.4 - 1.2		 0.2 0.4 1.2	 dB dB dB
Receive Gain **Absolute Accurary** Receive Gain Programmed for Maximum 0dBm0 Test Level Apply 0dBm0 PCM Code to $D_{R}0$ or $D_{R}1$ Measure VF_RO T_A = 25°C, V_{CC} = 5V, V_{SS} = - 5V	G_{RA}	- 0.15		0.15	dB
Receive Gain **Variation with Programmed Gain** Measure Receive Gain Over the Range from Maximum to Minimum Setting. Calculate the Deviation from the Programmed Gain Relative to G_{RA} i.e. $G_{RAG} = G_{actual} - G_{prog} - G_{RA}$ T_A = 25°C, V_{CC} = 5V, V_{SS} = - 5V	G_{RAG}	- 0.1		0.1	dB
Receive Gain **Variation with Temperature** Measured Relative to G_{RA} V_{CC} = 5V, V_{SS} = - 5V Minimum Gain $< G_R <$ Maximum Gain	G_{RAT}	- 0.1		0.1	dB

AMPLITUDE RESPONSE (continued)

Characteristic	Symbol	Min	Typ	Max	Unit
Receive Gain **Variation with Supply** Measured Relative to G_{RA} V_{CC} = 5 V ± 5%, V_{SS} = − 5 V ± 5% T_A = 25 °C, G_R = Maximum	G_{RAV}				
		− 0.05		0.05	dB
Receive Gain **Variation with Frequency** Relative to 1015.625 Hz, (Note 4) D_R0 or D_R1 = 0 dBm0 code Minimum Gain < G_R < Maximum Gain	G_{RAF}				
f = 200 Hz		− 0.25		0.15	dB
f = 300 Hz to 3000 Hz		− 0.15		0.15	dB
f = 3400 Hz		− 0.7		0.0	dB
f = 4000 Hz		–		− 14	dB
G_R = 4 dB, D_R0 = 0 dBm0 Code G_X = 0 dBm0, VF_XI = 0 dBm (Note 4)					
f = 203.125 Hz		− 0.25		0.15	dB
f = 296.875 Hz		− 0.15		0.15	dB
f = 515.625 Hz		− 0.15		0.15	dB
f = 2796.875 Hz		− 0.15		0.15	dB
f = 3015.625 Hz		− 0.15		0.15	dB
f = 3406.250 Hz		− 0.7		0.0	dB
f = 3984.375 Hz				− 13.5	dB
Receive Gain **Variation with Signal level** Sinusoidal Test Method Reference Level = 0 dBm0	G_{RAL}				
D_R0 = − 40 dBm0 to + 3 dBm0		− 0.2		0.2	dB
D_R0 = − 50 dBm0 to − 40 dBm0		− 0.4		0.4	dB
D_R0 = − 55 dBm0 to − 50 dBm0		− 1.2		1.2	dB

ENVELOPE DELAY DISTORTION WITH FREQUENCY

Characteristic	Symbol	Min	Typ	Max	Unit
Tx Delay, Absolute f = 1600 Hz	D_{XA}			315	μs
Tx Delay, Relative	D_{XR}				
f = 500 - 600 Hz				220	μs
f = 600 - 800 Hz				145	μs
f = 800 - 1000 Hz				75	μs
f = 1000 - 1600 Hz				40	μs
f = 1600 - 2600 Hz				75	μs
f = 2600 - 2800 Hz				105	μs
f = 2800 - 3000 Hz				155	μs
Rx Delay, Absolute f = 1600 Hz	D_{RA}			200	μs
Rx Delay, Relative	D_{RR}				
f = 500 - 1000 Hz		− 40			μs
f = 1000 - 1600 Hz		− 30			μs
f = 1600 - 2600 Hz				90	μs
f = 2600 - 2800 Hz				125	μs
f = 2800 - 3000 Hz				175	μs

NOISE

Characteristic	Symbol	Min	Typ	Max	Unit
Transmit Noise, C Message Weighted μ-law Selected (Note 1) All "1"s in Gain Register	N_{XC}		12	**15**	dBrnC0
Transmit Noise, P Message Weighted A-law Selected (Note 1) All "1"s in Gain Register	N_{XP}		74	**– 67**	dBm0p
Receive Noise, C Message Weighted μ-law Selected PCM Code is Alternating Positive	N_{RC}		8	**11**	dBrnC0
Receive Noise, P Message Weighted A-law Selected PCM Code Equals Postive Zero	N_{RP}		82	**– 79**	dBm0p
Noise, Single Frequency f = 0 kHz to 100 kHz, Loop Around Measurement, VF_XI = 0 Vrms	N_{RS}			53	dBm0
Positive Power Supply Rejection **Transmit** V_{CC} = 5.0 V_{DC} + 100 mVrms f = 0 kHz - 50 kHz (Note 2)	$PPSR_X$	**30**			dBC
Negative Power Supply Rejection **Transmit** V_{SS} = – 5.0 V_{DC} + 100 mVrms f = 0 kHz - 50 kHz (Note 2)	$NPSR_X$	**30**			dBC
Positive Power Supply Rejection **Receive** PCM Code Equals Positive Zero V_{CC} = 5.0 V_{DC} + 100 mVrms Measure VF_RO f = 0 Hz - 4000 Hz f = 4 kHz - 25 kHz f = 25 kHz - 50 kHz	$PPSR_R$	 **30** **40** **36**			 dBC dB dB
Negative Power Supply Rejection **Receive** PCM Code Equals Positive Zero V_{SS} = – 5.0 V_{DC} + 100 mVrms Measure VF_RO f = 0 Hz - 4000 Hz f = 4 kHz - 25 kHz f = 25 kHz - 50 kHz	$NPSR_R$	 **30** **40** **36**			 dBC dB dB
Spurious Out-of Band Signals **at the Channel Output** 0 dBm0, 300 Hz to 3400 Hz input PCM Code Applied at D_R0 (or D_R1) 4600 Hz - 7600 Hz 7600 Hz - 8400 Hz 8400 Hz - 100 000 Hz	SOS			 **– 30** **– 40** **– 30**	 dB dB dB

DISTORTION

Characteristic	Symbol	Min	Typ	Max	Unit
Signal to Total Distortion **Transmit or Receive** Half-Channel, μ-law Selected Sinusoidal Test Method	STD_X STD_R				
Level = 3.0 dBm0		**33**			dBC
= 0 dBm0 to − 30 dBm0		**36**			dBC
= − 40 dBm0 XMT		**29**			dBC
RCV		**30**			dBC
= − 45 dBm0 XMT		**25**			dBC
Single Frequency Distortion **Transmit**	SFD_X			**− 46**	dB
Single Frequency Distortion **Receive**	SFD_R			**− 46**	dB
Intermodulation Distortion Transmit or Receive Two Frequencies in the Range 300 Hz - 3400 Hz	IMD			**− 41**	dB

CROSSTALK

Transmit to Receive Crosstalk, 0 dBm0 Transmit Level f = 300 Hz - 3400 Hz D_R = Steady PCM Code	CT_{X-R}		− 90	**− 75**	dB
Receive to Transmit Crosstalk 0 dBm0 Receive Level f = 300 Hz - 3400 Hz, (Note 2)	CT_{R-X}		− 90	**− 70**	dB

Note 1 : Measured by extrapolation from distortion test result at − 50 dBm0

Note 2 : $PPSR_X$, $NPSR_X$, and CT_{R-X} are measured with a − 50 dBm0 activation signal applied to VF_XI.

Note 3 : A signal is Valid if it is above V_{IH} or below V_{IL} and invalid if it is between V_{IL} and V_{IH}. For the purposes of the specification the following conditions apply :

a) All input signals are defined as V_{IL} = 0.4 V, V_{IH} = 2 7V, $t_R < 10$ ns, $t_F < 10$ ns

b) t_R is measured from V_{IL} to V_{IH}, t_F is measured from V_{IH} to V_{IL}

c) Delay Times are measured from the input signal Valid to the output signal Valid

d) Setup Times are measured from the data input Valid to the clock input Invalid

e) Hold Times are measured from the clock signal Valid to the data input Invalid

f) Pulse widths are measured from V_{IL} to V_{IL} or from V_{IH} to V_{IH}

Note 4 : A multi-tone test technique is used.

DEFINITIONS

V_{IH} — V_{IH} is the D.C. input level above which an input level is guaranteed to appear as a logical one. This parameter is to be measured by performing a functional test at reduced clock speeds and nominal timing. (i.e. not minimum setup and hold times or output strobes), with the high level of all driving signals set to V_{IH} and maximum supply voltages applied to the device.

V_{IL} — V_{IL} is the D.C. input level below which an input level is guaranteed to appear as a logical zero the device. This parameter is measured in the same manner as V_{IH} but with all driving signal low levels set to VIL and minimum supply voltages applied to the device.

V_{OH} — V_{OH} is the minimum D.C. output level to which an output placed in a logical one state will converge when loaded at the maximum specified load current.

V_{OL} — V_{OL} is the maximum D.C. output level to which an output placed in a logical zero state will converge when loaded at the maximum specified load current.

Threshold Region — The threshold region is the range of input voltages between V_{IL} and V_{IH}.

Valid Signal — A signal is Valid if it is in one of the valid logic states. (i.e. above V_{IH} or below V_{IL}). In timing specifications, a signal is deemed valid at the instant it enters a valid state.

Invalid signal — A signal is invalid if it is not in a valid logic state, i.e., when it is in the threshold region between V_{IL} and V_{IH}. In timing specifications, a signal is deemed Invalid at the instant it enters the threshold region.

TIMING CONVENTIONS

For the purposes of this timing specification the following conventions apply.

Input Signals — All input signals may be characterized as: $V_L = 0.4$ V, $V_H = 2.4$ V, $t_R < 10$ ns, $t_F < 10$ ns.

Period — The period of the clock signal is designated as tp_{xx} where $_{xx}$ represents the mnemonic of the clock signal being specified.

Rise Time — Rise times are designated as t_{Ryy}, where yy represents a mnemonic of the signal whose rise time is being specified, t_{Ryy} is measured from V_{IL} to V_{IH}.

Fall Time — Fall times are designated as t_{Fyy}, where yy represents a mnemonic of the signal whose fall time is being specified, t_{Fyy} is measured from V_{IH} to V_{IL}.

Pulse Width High — The high pulse width is designated as t_{WzzH}, where zz represents the mnemonic of the input or output signal whose pulse width is being specified. High pulse widths are measured from V_{IH} to V_{IH}.

Pulse Width Low — The low pulse width is designated as t_{WzzL} where zz represents the mnemonic of the input or output signal whose pulse width is being specified. Low pulse widths are measured from V_{IL} to V_{IL}.

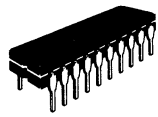
Setup Time — Setup times are designated as t_{Swwxx} where ww represents the mnemonic of the input signal whose setup time is being specified relative to a clock or strobe input represented by mnemonic xx. Setup times are measured from the ww Valid to xx Invalid.

Hold Time — Hold times are designated as T_{Hwwxx} where ww represents the mnemonic of the input signal whose hold time is being specified relative to a clock or strobe input represented by the mnemonic xx. Hold times are measured from xx Valid to ww Invalid.

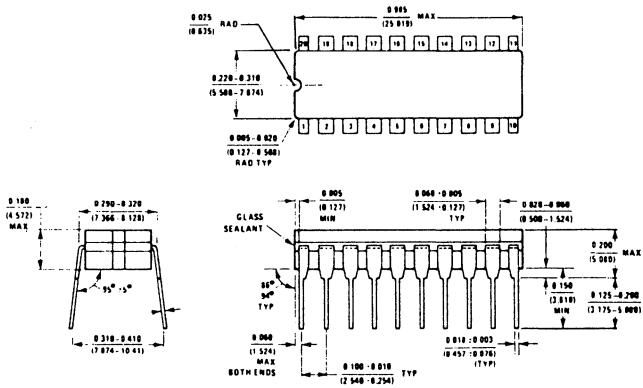
Delay Time — Delay times are designated as T_{Dxxyy} (IHIL), where xx represents the mnemonic of the input reference signal and yy represents the mnemonic of the output signal whose timing is being specified relative to xx. The mnemonic may optionally be terminated by an H or L to specify the high going or low going transition of the output signal. Maximum delay times are measured from xx Valid to yy Valid. Minimum delay times are measured from xx Valid to yy Invalid. This parameter is tested under the load conditions specified in the Conditions column of the Timing Specifications section of this datasheet.

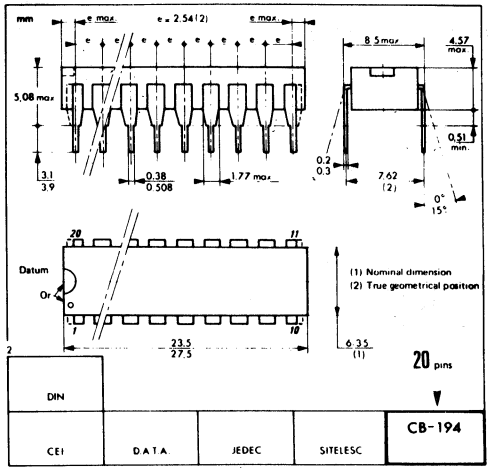
PHYSICAL DIMENSIONS

J20A

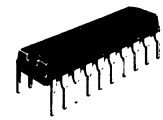


J SUFFIX
CERDIP PACKAGE

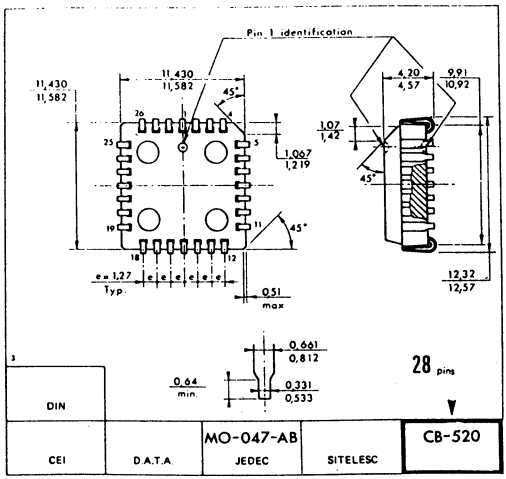




CB-194



P SUFFIX
PLASTIC PACKAGE



CB-520

FN SUFFIX
PLCC PACKAGE

MONOLITHIC SERIAL INTERFACE CODEC/FILTER

The ETC5057/ETC5054 family consists of A-law and μ-law monolithic PCM CODEC/filters utilizing the A/D and D/A conversion architecture shown in Figure 1, and a serial PCM interface. The devices are fabricated using double-poly CMOS process.

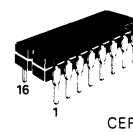
The encode portion of each device consists of an input gain adjust amplifier, an active RC pre-filter which eliminates very high frequency noise prior to entering a switched-capacitor band-pass filter that rejects signals below 200 Hz and above 3400 Hz. Also included are auto-zero circuitry and a companding coder which samples the filtered signal and encodes it in the companded A-law or μ-law PCM format. The decode portion of each device consists of an expanding decoder, which reconstructs the analog signal from the companded A-law or μ- law code, a low-pass filter which corrects for the sin x/x response of the decoder output and rejects signals above 3400 Hz and is followed by a single-ended power amplifier capable of driving low impedance loads. The devices require two 1.536 MHz, 1.544 MHz, or 2.048 MHz transmit and receive master clocks, which may be asynchronous, transmit and receive bit clocks which may vary from 64 kHz to 2.048 MHz, and transmit and receive frame sync pulses. The timing of the frame sync pulses and PCM data is compatible with both indrustry standard formats.

- Complete CODEC and filtering system (COMBO) including:
  - Transmit high-pass and low-pass filtering
  - Receive low-pass filter with sin x/x correction
  - Active RC noise filters
  - A-law or μ-law compatible COder and DECoder
  - Internal precision voltage reference
  - Serial I/O interface
  - Internal auto-zero circuitry
- A-law, 16-pins - ETC5057
- μ-law without signaling, 16-pins - ETC5054
- Meets or exceeds all D3/D4 and CCITT specifications
- ± 5V operation
- Low operating power - typically 60 mW
- Power-down standby - typically 3 mW
- TTL or CMOS compatible digital interfaces
- Maximizes line interface card circuit density
- Second source of TP3057, TP3054.

CMOS

MONOLITHIC SERIAL INTERFACE CODEC/FILTER

CASE J16A



J SUFFIX
CERDIP PACKAGE

PIN ASSIGNMENT

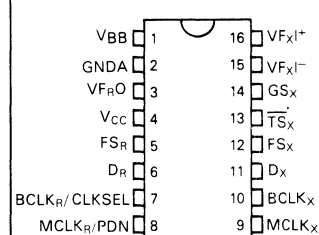
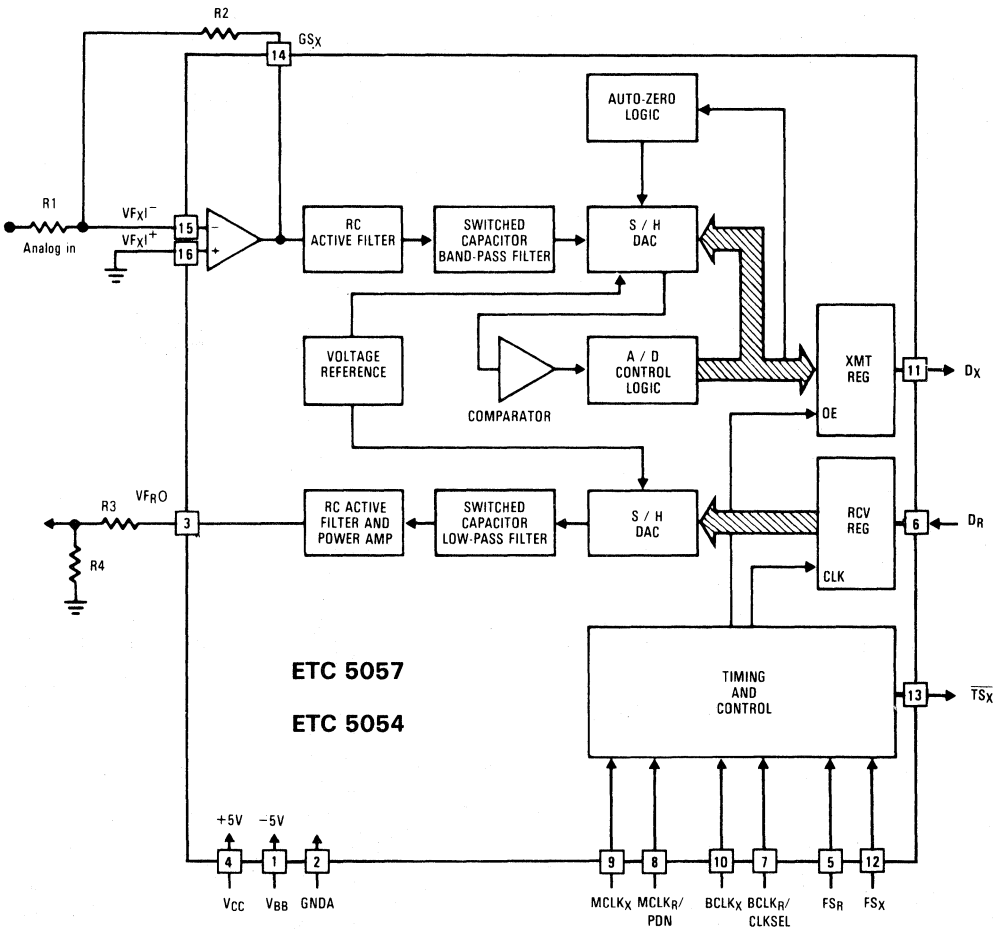


FIGURE 1 - BLOCK DIAGRAM



PIN DESCRIPTION

NAME	PIN TYPE *	N°	FUNCTION	DESCRIPTION
V_{BB}	S	1	Negative power supply	$V_{BB} = -5V \pm 5\%$.
GNDA	GND	2	Analog ground	All signals are referenced to this pin.
VF_RO	O	3	Receive filter output	Analog output of the receive filter
V_{CC}	S	4	Positive power supply	$V_{CC} = +5V \pm 5\%$.
FS_R	I	5	Receive frame sync pulse	Enables $BCLK_R$ to shift PCM data into D_R.FS_R is an 8 kHz pulse train. See Figures 2,3 and 4 for timing details.
D_R	I	6	Receive data input	PCM data is shifted into D_R following the FS_R leading edge.
$BCLK_R$/CLKSEL	I	7	Shift-in clock	Shifts data into D_R after the FS_R leading edge. May vary from 64 kHz to 2.048 MHz. Alternatively, may be a logic input which selects either 1.536 MHz/1.544 MHz or 2.048 MHz for master clock in synchronous mode and $BCLK_X$ is used for both transmit and receive directions (see Table 1).
$MCLK_R$/PDN	I	8	Receive master clock	Must be 1.536 MHz, 1.544 MHz or 2.048 MHz. May be asynchronous with $MCLK_X$, but should be synchronous with $MCLK_X$ for best performance. When $MCLK_R$ is connected continuously low, $MCLK_X$ is selected for all internal timing. When $MCLK_R$ is connected continuously high, the device is powered down.
$MCLK_X$	I	9	Transmit master clock	Must be 1.536 MHz, 1.544 MHz ro 2.048 MHz. May be asynchronous with $MCLK_R$.
FS_X	I	12	Transmit frame sync pulse	Enables $BCLK_X$ to shift out the PCM data on D_X.FS_X is an 8 kHz pulse train. See Figures 2,3 and 4 for timing details.
$BCLK_X$	I	10	Shift-out clock	Shifts out the PCM data on D_X. May vary from 64 kHz to 2.048 MHz, but must be synchronous with $MCLK_X$.
D_X	O	11	Transmit data output	The TRI-STATE® PCM data output which is enabled by FS_X.
$\overline{TS_X}$	O	13	Transmit time slot	Open drain output which pulses low during the encoder time slot. Must be grounded if not used.
GS_X	O	14	Gain set	Analog output of the transmit input amplifier. Used to set gain externally.
VF_XI^-	I	15	Inverting amplifier input	Inverting input of the transmit input amplifier.
VF_XI^+	I	16	Non-inverting amplifier input	Non-inverting input of the transmit input amplifier.

*I : Input, O : Output, S : Power supply

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FUNCTIONAL DESCRIPTION

POWER-UP

When power is first applied, power-on reset circuitry initializes the COMBO and places it into the power-down mode. All non-essential circuits are deactivated and the D_X and VF_RO outputs are put in high impedance states. To power-up the device, a logical low level or clock must be applied to the $MCLK_R$/PDN pin and FS_X and/or FS_R pulses must be present. Thus, 2 power-down control modes are available. The first is to pull the $MCLK_R$/PDN pin high ; the alternative is to hold both FS_X and FS_R inputs continuously low. The device will power-down approximately 2 ms after the last FS_X or FS_R pulse. Power-up will occur on the first FS_X or FS_R pulse. The TRI-STATE PCM data output, D_X, will remain in the high impedance state until the second FS_X pulse.

SYNCHRONOUS OPERATION

For synchronous operation, the same master clock and bit clock should be used for both the transmit and receive directions. In this mode, a clock must be applied to $MCLK_X$ and the $MCLK_R$/ PDN pin can be used as a power-down control. A low level on $MCLK_R$/PDN powers up the device and a high level powers down the device. In either case, $MCLK_X$ will be selected as the master clock for both the transmit and receive circuits. A bit clock must also be applied to $BCLK_X$ and the $BCLK_R$/CLKSEL can be used to select the proper internal divider for a master clock of 1.536 MHz, 1.544 MHz or 2.048 MHz. For 1.544 MHz operation, the device automatically compensates for the 193rd clock pulse each frame.
With a fixed level on the $BCLK_R$/CLKSEL pin, $BCLK_X$ will be selected as the bit clock for both the transmit and receive directions. Table 1 indicates the frequencies of operation which can be selected, depending on the state of $BCLK_R$/CLKSEL. In this synchronous mode, the bit clock, $BCLK_X$, may be from 64 kHz to 2.048 MHz, but must be synchronous with $MCLK_X$.

TABLE 1 - SELECTION OF MASTER CLOCK FREQUENCIES

$BCLK_R$/CLKSEL	Master clock frequency selected	
	ETC 5057	ETC 5054
Clocked	2.048 MHz	1.536 MHz or 1.544 MHz
0	1.536 MHz or 1.544 MHz	2.048 MHz
1 (or open circuit)	2.048 MHz	1.536 MHz or 1.544 MHz

Each FS_X pulse begins the encoding cycle and the PCM data from the previous encode cycle is shifted out of the enabled D_X output on the positive edge of $BCLK_X$. After 8 bit clock periods, the TRI-STATE D_X output is returned to a high impedance state. With an FS_R pulse, PCM data is latched via the D_R input on the negative edge of $BCLK_X$(or $BCLK_R$ if running). FS_X and FS_R must be synchronous with $MCLK_{X/R}$.

ASYNCHRONOUS OPERATION

For asynchronous operation, separate transmit and receive clocks may be applied. $MCLK_X$ and $MCLK_R$ must be 2.048 MHz for the ETC5057, or 1.536 MHz, 1.544 MHz for the ETC5054, and need not be synchronous. For best transmission performance, however, $MCLK_R$ should be synchronous with $MCLK_X$, which is easily achieved by applying only static logic levels to the $MCLK_R$/ PDN pin. This will automatically connect $MCLK_X$ to all internal $MCLK_R$ functions (see Pin Description). For 1.544 MHz operation, the device automatically compensates for the 193rd clock pulse each frame. FS_X starts each encoding cycle and must be synchronous with $MCLK_X$ and $BCLK_X$. FS_R starts each decoding cycle and must be synchronous with $BCLK_R$. $BCLK_R$ must be a clock, the logic levels shown in Table 1 are not valid in asynchronous mode. $BCLK_X$ and $BCLK_R$ may operate from 64 kHz to 2.048 MHz.

SHORT FRAME SYNC OPERATION

The COMBO can utilize either a short frame sync pulse or a long frame sync pulse. Upon power initialization, the device assumes a short frame mode. In this mode, both frame sync pulses, FS_X and FS_R, must be one bit clock period long, with timing relationships specified in Figure 3. With FS_X high during a falling edge of $BCLK_X$, the next rising edge of $BCLK_X$ enables the D_X TRI-STATE output buffer, which will output the sign bit. The following seven rising edges clock out the remaining seven bits, and the next falling edge disables the D_X output. With FS_R high during a falling edge of $BCLK_R$ ($BCLK_X$ in synchronous mode), the next falling edge of $BCLK_R$ latches in the sign bit. The following seven falling edges latch in the seven remaining bits. Both devices may utilize the short frame sync pulse in synchronous or asynchronous operating mode.

LONG FRAME SYNC OPERATION

To use the long frame mode, both the frame sync pulses, FS_X and FS_R, must be three or more bit clock periods long, with timing relationships specified in Figure 4. Based on the transmit frame sync. FS_X, the COMBO will sense whether short or long frame sync pulses are being used. For 64 kHz operation, the frame sync pulse must be kept low for a minimum of 160 ns (See Fig. 2). The D_X TRI-STATE output buffer is enabled with the rising edge of FS_X or the rising edge of

$BCLK_X$, whichever comes later, and the first bit clocked out is the sign bit. The following seven $BCLK_X$ rising edges clock out the remaining seven bits. The D_X output is disabled by the falling $BCLK_X$ edge following the eighth rising edge, or by FS_X going low, whichever comes later. A rising edge on the receive frame sync pulse, FS_R, will cause the PCM data at D_R to be latched in on the next eight falling edges of $BCLK_R$ ($BCLK_X$ in synchronous mode). Both devices may utilize the long frame sync pulse in synchronous or asynchronous mode.

TRANSMIT SECTION

The transmit section input is an operational amplifier with provision for gain adjustment using two external resistors, see Figure 5. The low noise and wide bandwidth allow gains in excess of 20 dB across the audio passband to be realized. The op amp drives a unity-gain filter consisting of RC active pre-filter, followed by an eighth order switched-capacitor bandpass filter clocked at 256 kHz. The output of this filter directly drives the encoder sample-and-hold circuit. The A/D is of companding type according to A-law (ETC5057) or μ law (ETC5054) coding conventions. A precision voltage reference is trimmed in manufacturing to provide an input overload (t_{MAX}) of nominally 2.5V peak (see table of Transmission Characteristics). The FS_X frame sync pulse controls the sampling of the filter output, and then the successive-approximation encoding cycle begins. The 8-bit code is then loaded into a buffer and shifted out through D_X at the next FS_X pulse. The total encoding delay will be approximately 165 μ s (due to the transmit filter) plus 125 μ s (due to encoding delay), which totals 290 μ s. Any offset voltage due to the filters or comparator is cancelled by sign bit integration.

RECEIVE SECTION

The receive section consists of an expanding DAC which drives a fifth order switched-capacitor low pass filter clocked at 256 kHz. The decoder is A-law (ETC5057) or μ -law (ETC5054) and the 5th order low pass filter corrects for the sin x/x attenuation due to the 8 kHz sample and hold. The filter is then followed by a 2nd order RC active post-filter and power amplifier capable of driving a 600 Ω load to a level of 7.2 dBm. The receive section is unity-gain. Upon the occurence of FS_R, the data at the D_R input is clocked in on the falling edge of the next eight $BCLK_R$ ($BCLK_X$) periods. At the end of the decoder time slot, the decoding cycle begins, and 10 μ s later the decoder DAC output is updated. The total decoder delay is ~10 μ s (decoder update) plus 110 μ s (filter delay) plus 62.5 μ s (1/2 frame), which gives approximately 180 μ s.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
V_{CC} to GNDA	V_{CC}	7	V
V_{BB} to GNDA	V_{BB}	−7	V
Voltage at any analog input or output	V_{IN}, V_{OUT}	V_{CC} +0.3 to V_{BB} −0.3	V
Voltage at any digital input or output		V_{CC} +0.3 to GNDA −0.3	V
Operating temperature range	T_{oper}	−25 to +125	°C
Storage temperature range	T_{stg}	−65 to +150	°C
Lead temperature (soldering, 10 seconds)		300	°C

ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 5%, V_{BB} = −5V ± 5%, GNDA = 0V, T_A = 0°C to 70°C (Unless otherwise noted); typical characteristics specified at V_{CC} = 5.0V, V_{BB} = − 5.0V, T_A = 25°C; all signals are referenced to GNDA.

DIGITAL INTERFACE

Characteristic	Symbol	Min	Typ	Max	Unit
Input low voltage	V_{IL}	–	–	0.6	V
Input high voltage	V_{IH}	2.2	–	–	V
Output low voltage	V_{OL}				V
I_L=3.2mA D_X		–	–	0.4	
I_L=3.2mA, open drain $\overline{TS_X}$		–	–	0.4	
Output high voltage	V_{OH}				V
I_H=−3.2mA D_X		2.4	–	–	
Input low current (GNDA ≤ V_{IN} ≤ V_{IL}, all digital inputs)	I_{IL}	−10	–	10	μA
Input high current (V_{IH} ≤ V_{IN} ≤ V_{CC})	I_{IH}	−10	–	10	μA
Output current in hight impedance state (TRI-STATE)	I_{OZ}				μA
(GNDA ≤ V_O ≤ V_{CC}) D_X		−10	–	10	

ANALOG INTERFACE WITH TRANSMIT INPUT AMPLIFIER (ALL DEVICES)

Input leakage current (−2.5V ≤ V ≤ +2.5V) VF_XI^+ or VF_XI^-	I_IXA	−200	–	200	nA
Input resistance (−2.5V ≤ V ≤ +2.5V) VF_XI^+ or VF_XI^-	R_IXA	10	–	–	MΩ
Output resistance (closed loop, unity gain)	R_OXA	–	1	3	Ω
Load resistance GS_X	R_LXA	10	–	–	kΩ
Load capacitance GS_X	C_LXA	–	–	50	pF
Output dynamic range (R_L ≥ 10kΩ) GS_X	V_OXA	± 2.8	–	–	V
Voltage gain (VF_XI^+ to GS_X)	A_VXA	5000	–	–	V/V
Unity gain bandwidth	F_UXA	1	2	–	MHz
Offset voltage	$V_{OS}XA$	−20	–	20	mV
Common-mode voltage	$V_{CM}XA$	−2.5	–	2.5	V
Common-mode rejection ratio	CMRRXA	60	–	–	dB
Power supply rejection ratio	PSRRXA	60	–	–	dB

ANALOG INTERFACE WITH RECEIVE FILTER (ALL DEVICES)

Output resistance VF_RO	R_ORF	–	1	3	Ω
Load resistance (VF_RO = ± 2.5V)	R_LRF	600	–	–	Ω
Load capacitance	C_LRF	–	–	500	pF
Output DC offset voltage	VOS_RO	−200	–	200	mV

POWER DISSIPATION (ALL DEVICES)

Power-down current	$I_{CC}0$	–	0.5	1.5	mA
Power-down current	$I_{BB}0$	–	0.05	0.3	mA
Active current	$I_{CC}1$	–	6.0	9.0	mA
Active current	$I_{BB}1$	–	6.0	9.0	mA

TIMING SPECIFICATIONS

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency of master clocks Depends on the device used and the $BCLK_R$/CLKSEL Pin $MCLK_X$ and $MCLK_R$	$1/t_{PM}$	– – –	1.536 1.544 2.048	– – –	MHz
Width of master clock high $MCLK_X$ and $MCLK_R$	t_{WMH}	160	–	–	ns
Width of master clock low $MCLK_X$ and $MCLK_R$	t_{WML}	160	–	–	ns
Rise time of master clock $MCLK_X$ and $MCLK_R$	t_{RM}	–	–	50	ns
Fall time of master clock $MCLK_X$ and $MCLK_R$	t_{FM}	–	–	50	ns
Period of bit clock	t_{PB}	485	488	15.725	ns
Width of bit clock high (V_{IH}=2.2V)	t_{WBH}	160	–	–	ns
Width of bit clock low (V_{IL}=0.6V)	t_{WBL}	160	–	–	ns
Rise time of bit clock (t_{PB}=488ns)	t_{RB}	–	–	50	ns
Fall time of bit clock (t_{PB}=488ns)	t_{FB}	–	–	50	ns
Set-up time from $BCLK_X$ high to $MCLK_X$ falling edge. (First bit clock after the leading edge of FS_X)	t_{SBFM}	100	–	–	ns
Holding time from bit clock low to the frame sync (long frame only)	t_{HBF}	0	–	–	ns
Set-up time from frame sync to bit clock low (long frame only)	t_{SFB}	80	–	–	ns
Hold time from 3rd period of bit clock low to frame sync (long frame only) FS_X or FS_R	t_{HBFI}	100	–	–	ns
Delay time to valid data from FS_X or $BCLK_X$, whichever comes later and delay time from FS_X to data output disabled (C_L=0 pF to 150 pF)	t_{DZF}	20	–	165	ns
Delay time from $BCLK_X$ high to data valid (Load=150 pF plus 2 LSTTL loads)	t_{DBD}	0	–	180	ns
Delay time from $BCLK_X$ low to data output disabled	t_{DZC}	50	–	165	ns
Set-up time from D_R valid to $BCLK_{R/X}$ low	t_{SDB}	50	–	–	ns
Hold time from $BCLK_{R/X}$ low to D_R invalid	t_{HBD}	50	–	–	ns
Holding time from bit clock high to frame sync (short frame only)	t_{HOLD}	0	–	–	ns
Set-up time from $FS_{X/R}$ to $BCLK_{X/R}$ low (short frame sync pulse) - Note 1	t_{SF}	50	–	–	ns
Hold time from $BCLK_{X/R}$ low to $FS_{X/R}$ low (short frame sync pulse) - Note 1	t_{HF}	100	–	–	
Delay time to TS_X low (load=150 pF plus 2 LSTTL loads)	t_{XDP}	–	–	140	ns
Minimum width of the frame sync pulse (low level) (64k bit/s operating mode)	t_{WFL}	160	–	–	ns

Note 1 : For short frame sync timing, FS_X and FS_R must go high while their respective bit clocks are high.

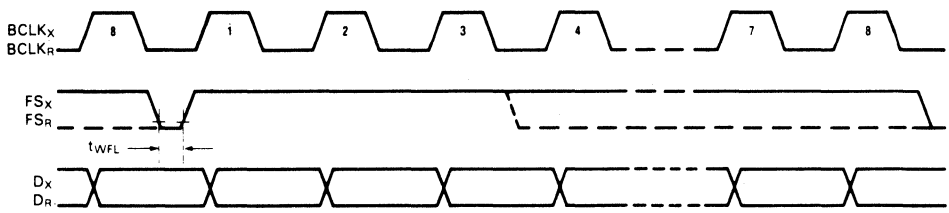


FIGURE 2 - 64 k bits/s TIMING DIAGRAM (See next page for complete timing)

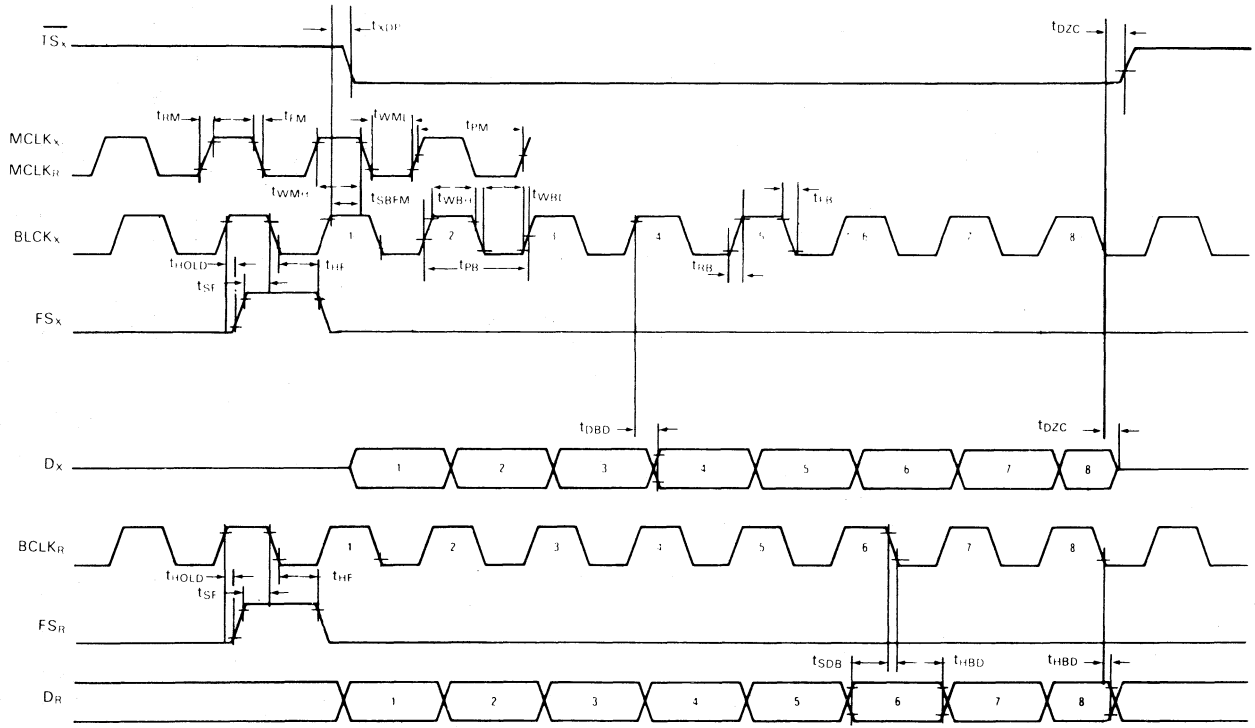


FIGURE 3 - SHORT FRAME SYNC TIMING

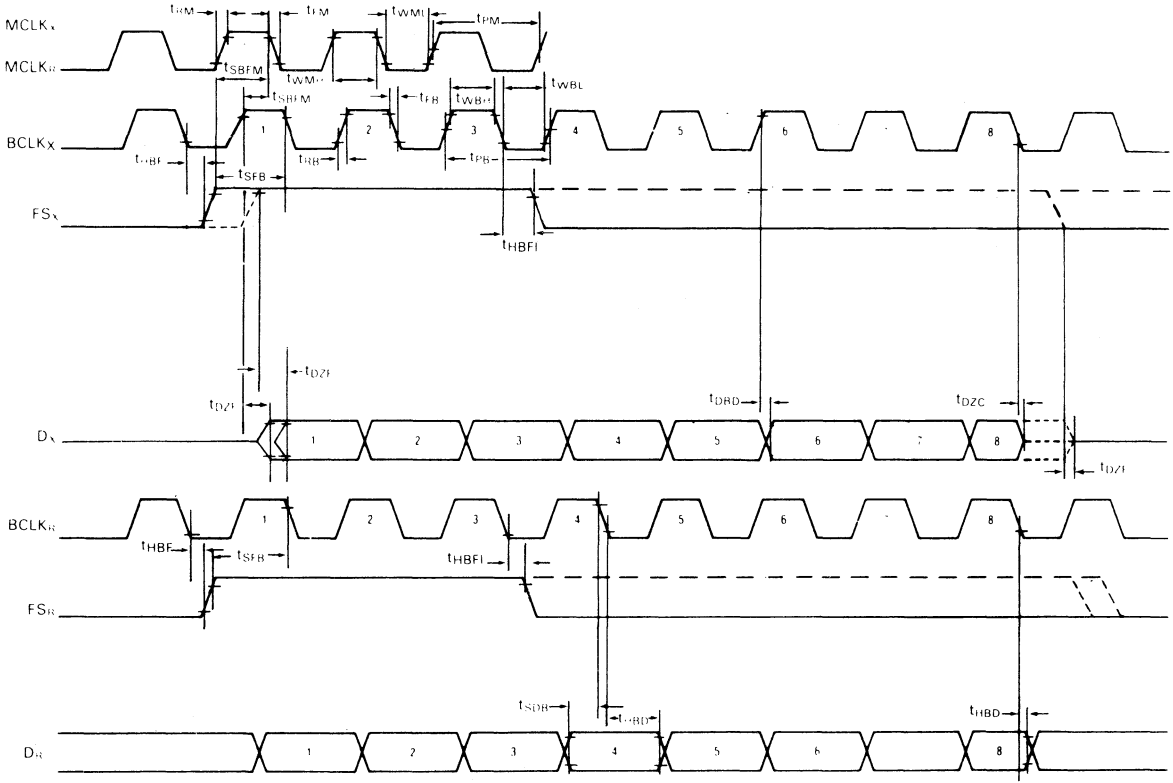


FIGURE 4 - LONG FRAME SYNC TIMING

TRANSMISSION CHARACTERISTICS

(All devices) $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$, $V_{BB} = -5V \pm 5\%$, GNDA = 0V, f = 1.02 kHz, V_{IN} = 0 dBm0 transmit input amplifier connected for unity-gain non-inverting. (Unless otherwise specified)

AMPLITUDE RESPONSE

Characteristic	Symbol	Min	Typ	Max	Unit
Absolute levels - Nominal 0 dBm0 level is 4 dBm (600Ω) 0 dBm0 ETC 5057, ETC 5054		–	1.2276	–	Vrms
Max overload level 3.14 dBm0 ETC 5057 3.17 dBm0 ETC 5054	t_{MAX}	– –	2.492 2.501	– –	V_{PK}
Transmit gain, absolute ($T_A = 25°C$, $V_{CC} = 5V$, $V_{BB} = -5V$) Input at GS_X = 0 dBm0 at 1020 Hz	G_{XA}	−0.15	–	0.15	dB
Transmit gain, relative to G_{XA} f = 16Hz f = 50Hz f = 60Hz f = 180Hz f = 200Hz f = 300Hz-3000 Hz f = 3300Hz f = 3400Hz f = 4000Hz f = 4600Hz and up,measure reponse from 0Hz to 4000Hz	G_{XR}	 – – – −2.8 −1.8 −0.15 −0.35 −0.7 – –	 – – – – – – – – – –	 −40 −30 −26 −0.2 −0.1 0.15 0.05 0 −14 −32	dB
Absolute transmit gain variation with temperature ($T_A = 0°C$ to $+80°C$)	G_{XAT}	–	–	± 0.1	dB
Absolute transmit gain variation with supply voltage ($V_{CC} = 5V \pm 5\%$, $V_{BB} = -5V \pm 5\%$)	G_{XAV}	–	–	± 0.05	dB
Transmit gain variations with level Sinusoidal test method reference level = −10dBm0 VF_XI^+ = −40dBm0 to +3dBm0 VF_XI^+ = −50dBm0 to −40dBm0 VF_XI^+ = −55dBm0 to −50dBm0	G_{XRL}	 −0.2 −0.4 −1.2	 – – –	 0.2 0.4 1.2	dB
Receive gain, absolute ($T_A = 25°C$, $V_{CC} = 5V$, $V_{BB} = -5V$) Input = digital code sequence for 0dBm0 signal at 1020Hz	G_{RA}	−0.15	–	0.15	dB
Receive gain, relative to G_{RA} f = 0Hz to 3000 Hz f = 3300Hz f = 3400Hz f = 4000Hz	G_{RR}	 −0.15 −0.35 −0.7 –	 – – – –	 0.15 0.05 0 −14	dB
Absolute receive gain variation with temperature ($T_A = 0°C$ to $+80°C$)	G_{RAT}	–	–	± 0.1	dB
Absolute receive gain variation with supply voltage ($V_{CC} = 5V \pm 5\%$, $V_{BB} = -5V \pm 5\%$)	G_{RAV}	–	–	± 0.05	dB
Receive gain variations with level Sinusoidal test method;reference input PCM code corresponds to an ideally encoded −10dBm0 signal PCM level = −40dBm0 to +3dBm0 PCM level = −50dBm0 to −40dBm0 PCM level = −55dBm0 to −50dBm0	G_{RRL}	 −0.2 −0.4 −1.2	 – – –	 0.2 0.4 1.2	dB
Receive output drive level ($R_L = 600\Omega$)	V_{RO}	−2.5	–	2.5	V

TRANSMISSION CHARACTERISTICS

(All devices) T_A = 0°C to +70°C, V_{CC} = 5V ± 5%, V_{BB} = −5V ± 5%, GNDA = 0V, f = 1.02 kHz, V_{IN} = 0 dBm0, transmit input amplifier connected for unity-gain non-inverting. (Unless otherwise specified)

ENVELOPE DELAY DISTORTION WITH FREQUENCY

Characteristic	Symbol	Min	Typ	Max	Unit
Transmit delay, absolute (f = 1600Hz)	D_{XA}	–	290	315	μs
Transmit delay, relative to D_{XA}	D_{XR}				μs
f = 500Hz-600Hz		–	195	220	
f = 600Hz-800Hz		–	120	145	
f = 800Hz-1000 Hz		–	50	75	
f = 1000Hz-1600Hz		–	20	40	
f = 1600Hz-2600Hz		–	55	75	
f = 2600Hz-2800Hz		–	80	105	
f = 2800Hz-3000Hz		–	130	155	
Receive delay, absolute (f = 1600Hz)	D_{RA}	–	180	200	μs
Receive delay, relative to D_{RA}	D_{RR}				μs
f = 500Hz-1000Hz		−40	−25	–	
f = 1000Hz-1600Hz		−30	−20	–	
f = 1600Hz-2600Hz		–	70	90	
f = 2600Hz-2800Hz		–	100	125	
f = 2800Hz-3000Hz		–	145	175	

NOISE

Transmit noise, P message weighted (ETC 5057, VF_XI^+ = 0V)	N_{XP}	–	−74	−69 (Note 1)	dBm0p
Receive noise, P message weighted (ETC 5057, PCM code equals positive zero)	N_{RP}	–	−82	−79	dBm0p
Transmit noise, C message weighted (ETC 5054, VF_XI^+ = 0V)	N_{XC}	–	12	15	dBrnC0
Receive noise, C message weighted ETC 5054, PCM code equals alternating positive and negative zero	N_{RC}	–	8	11	dBrnC0
Noise, single frequency f = 0kHz to 100kHz, loop around measurement, VF_XI^+ = 0Vrms	N_{RS}	–	–	−53	dBm0
Positive power supply rejection, transmit VF_XI^+ = 0Vrms, V_{CC} = 5.0V_{DC}+100mVrms, f = 0kHz-50kHz	$PPSR_X$	40	–	–	dBp
Negative power supply rejection, transmit VF_XI^+ = 0Vrms V_{BB} = −5.0V_{DC}+100mVrms f = 0kHz-50kHz	$NPSR_X$	40	–	–	dBp
Positive power supply rejection, receive (PCM code equals positive zero, V_{CC} = 5.0V_{DC}+100mVrms)	$PPSR_R$				
f = 0Hz-4000Hz		40	–	–	dBp
f = 4kHz-25kHz		40	–	–	dB
f = 25kHz-50kHz		36	–	–	dB
Negative power supply rejection, receive (PCM code equals positive zero, V_{BB} = −5.0V_{DC}+100mVrms)	$NPSR_R$				
f = 0Hz-4000Hz		40	–	–	dBp
f = 4kHz-25kHz		40	–	–	dB
f = 25kHz-50kHz		36	–	–	dB

TRANSMISSION CHARACTERISTICS (Continued)
(All devices) T_A = 0°C to +70°C, V_{CC} = 5V ± 5%, V_{BB} = −5V ± 5%, GNDA = 0V, f = 1.02 kHz, V_{IN} = 0 dBm0, transmit input amplifier connected for unity-gain non-inverting. (Unless otherwise specified)

Characteristic		Symbol	Min	Typ	Max	Unit
Spurious out-of-band signals at the channel output Loop around measurement, 0 dBm0, 300Hz-3400Hz input applied to VF_XI^+, measure individual image signals at VF_RO		SOS	–	–	−30	dB
4600Hz-7600Hz			–	–	−32	
7600Hz-8400Hz			–	–	−40	
8400Hz-100,000Hz			–	–	−32	
DISTORTION						
Signal to total distortion (sinusoidal test method)		STD_X or STD_R				dBp
Transmit or receive half-channel						
Level = 3.0dBm0			33	–	–	
= 0dBm0 to −30dBm0			36	–	–	
= −40dBm0	XMT		29	–	–	
	RCV		30	–	–	
= −55dBm0	XMT		14	–	–	
	RCV		15	–	–	
Single frequency distortion, transmit		SFD_X	–	–	−46	dB
Single frequency distortion, receive		SFD_R	–	–	−46	dB
Intermodulation distortion Loop around measurement, VF_XI^+ = −4dBm0 to −21dBm0, two frequencies in the range 300Hz-3400Hz		IMD	–	–	−41	dB
CROSSTALK						
Transmit to receive crosstalk, 0dBm0 transmit level f = 300Hz-3400Hz, D_R = steady PCM code		CT_{X-R}	–	−90	−75	dB
Receive to transmit crosstalk, 0dBm0 receive level f = 300Hz-3400Hz, VF_XI = 0V		CT_{R-X}	–	−90	−70 (Note 2)	dB

Note 1 : Theoretical worst-case for a perfectly zeroed encoder with alternating sign bit, due to the decoding law.
Note 2 : CT_{R-X} is measured with a −40 dBm0 activating signal applied at VF_XI^+

ENCODING FORMAT AT D_X OUTPUT

	A-Law (includes even bit inversion)	μLaw
V_{IN}(at GS_X) = +Full-scale	1 0 1 0 1 0 1 0	1 0 0 0 0 0 0 0
V_{IN}(at GS_X) = 0V	1 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1	1 1 1 1 1 1 1 1 0 1 1 1 1 1 1 1
V_{IN}(at GS_X) = −Full-scale	0 0 1 0 1 0 1 0	0 0 0 0 0 0 0 0

APPLICATIONS INFORMATION

POWER SUPPLIES

While the pins ot the ETC5050 family are well protected against electrical misuse, it is recommended that the standard CMOS practice be followed, ensuring that ground is connected to the device before any other connections are made. In applications where the printed circuit board may be plugged into a "hot" socket with power and clocks already present, an extra long ground pin in the connector is useful.

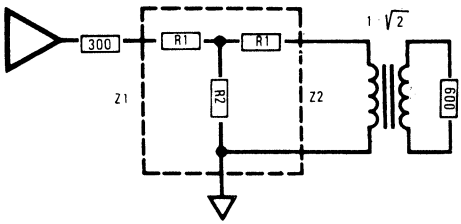
All ground connections to each device should meet at a common point as close as possible to the GNDA pin. This minimizes the interaction of ground return currents flowing through a common bus impedance. 0.1 μF supply decoupling capacitors should be connected from this common ground point to V_{CC} and V_{BB}.

For best performance, the ground point of beach /FILTER on a card should be connected to a common card This common ground point should be decoupled to V_{CC} and V_{BB} with 10 μF capacitors.

RECEIVE GAIN ADJUSTMENT

For applications where a ETC5050 family CODEC/filter receive output must drive a 600 Ω load, but a peak swing lower then ±2.5V is required, the receive gain can be easily adjusted by inserting a matched T- pad or π-pad at the output. Table II lists the required resistor values for 600 Ω terminations. As these are generally non-standard values, the equations can be used to compute the attenuation of the closest pratical set of resistors. It may be necessary to use unequal values for the R1 or R4 arms of the attenuators to achieve a precise attenuation. Generally it is tolerable to allow a small deviation of the input impedance from nominal while still maintaining a good return loss. For example a 30 dB return loss against 600 Ω is obtained if the output impedance of the attenuator is in the range 282 Ω to 319 Ω (assuming a perfect transformer).

T-PAD ATTENUATOR



$$R1 = Z1\left(\frac{N^2+1}{N^2-1}\right) - 2\sqrt{Z1.Z2}\left(\frac{N}{N^2-1}\right)$$

$$R2 = 2\sqrt{Z1.Z2}\left(\frac{N}{N^2-1}\right)$$

Where : $N = \sqrt{\frac{\text{POWER IN}}{\text{POWER OUT}}}$

and

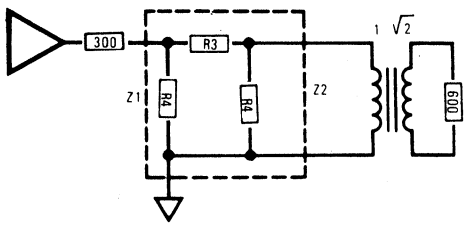
$$S = \sqrt{\frac{Z1}{Z2}}$$

$$\text{Also} : Z = \sqrt{Z_{SC}.Z_{OC}}$$

Where Z_{SC} = impedance with short circuit termination

and Z_{OC} = impedance with open circuit termination

π - PAD ATTENUATOR



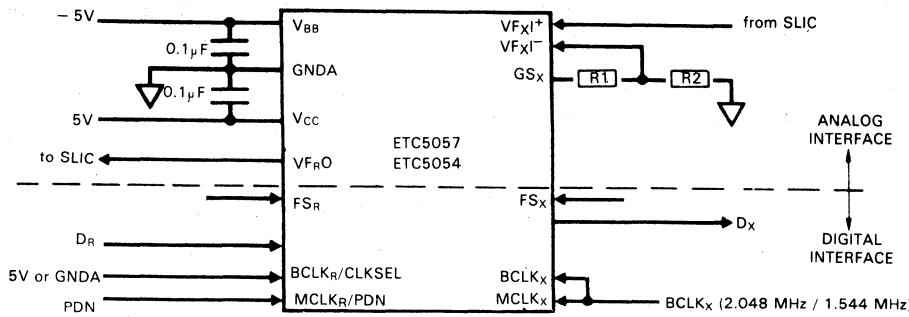
$$R3 = \sqrt{\frac{Z1.Z2}{2}}\left(\frac{N^2-1}{N}\right)$$

$$R4 = Z1\left(\frac{N^2-1}{N^2-2NS+1}\right)$$

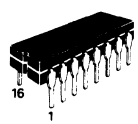
TABLE II. ATTENUATOR TABLES FOR Z1 = Z2 = 300 Ω (ALL VALUES IN Ω)

dB	R1	R2	R3	R4
0.1	1.7	26k	3.5	52k
0.2	3.5	13k	6.9	26k
0.3	5.2	8.7k	10.4	17.4k
0.4	6.9	6.5k	13.8	13k
0.5	8.5	5.2k	17.3	10.5k
0.6	10.4	4.4k	21.3	8.7k
0.7	12.1	3.7k	24.2	7.5k
0.8	13.8	3.3k	27.7	6.5k
0.9	15.5	2.9k	31.1	5.8k
1.0	17.3	2.6k	34.6	5.2k
2	34.4	1.3k	70	2.6k
3	51.3	850	107	1.8k
4	68	650	144	1.3k
5	84	494	183	1.1k
6	100	402	224	900
7	115	380	269	785
8	379	284	317	698
9	143	244	370	630
10	156	211	427	527
11	168	184	490	535
12	180	161	550	500
13	190	142	635	473
14	200	125	720	450
15	210	110	816	430
16	218	98	924	413
18	233	77	1.17k	386
20	246	61	1.5k	366

FIGURE 5 - TYPICAL SYNCHRONOUS APPLICATION

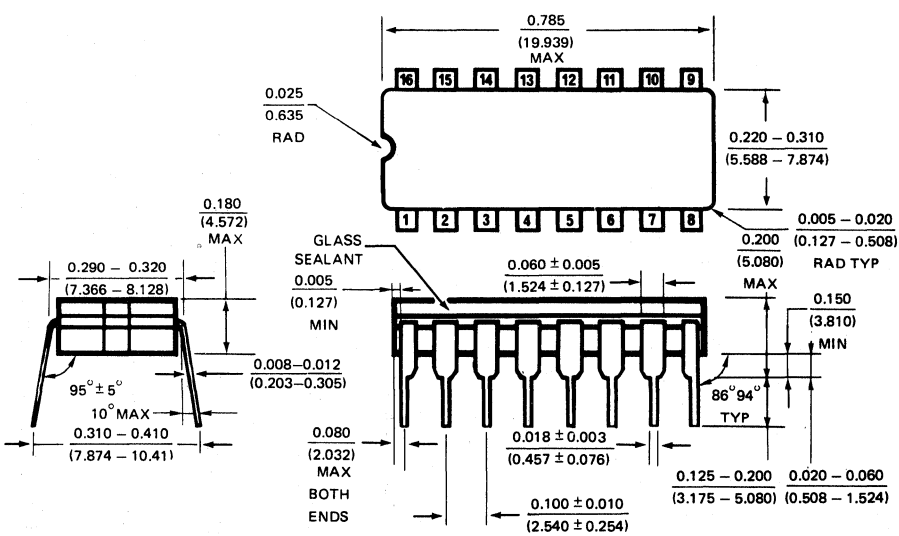


Note 1 : XMIT gain = $20 \times \log\left(\frac{R1 + R2}{R2}\right)$ $(R1 + R2) > 10k\Omega$



CASE J16A

J SUFFIX
CERDIP PACKAGE



PHYSICAL DIMENSIONS

MONOLITHIC SERIAL INTERFACE CODEC/FILTER WITH RECEIVE POWER AMPLIFIER

The ETC5064 (μ-law) and ETC5067 (A-law) are monolithic PCM CODEC/FILTERS utilizing the A/D and D/A conversion architecture shown in Figure 1, and a serial PCM interface. The devices are fabricated using National's advanced double-poly CMOS process (microCMOS).

Similar to the ETC5050 family, these devices feature an additional Receive Power Amplifier to provide push-pull balanced output drive capacity. The receive gain can be adjusted by means of two external resistors for an output level of up to ±6.6 V across a balanced 600 Ω load.

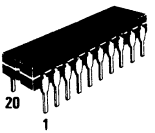
Also included is an Analog Loopback switch and $\overline{TS_X}$ output.

- Complete CODEC and filtering system including :
  - Transmit high-pass and low-pass filtering.
  - Receive low-pass filter with sin x/x correction.
  - Active RC noise filters.
  - μ-law or A-law compatible COder and DECoder.
  - Internal precision voltage reference.
  - Serial I/O interface.
  - Internal auto-zero circuitry.
  - Receive push-pull power amplifiers.
- μ-law ETC5064
- A-law ETC5067
- Meets or exceeds all D3/D4 and CCITT specifications.
- ±5 V operation.
- Low operating power - typically 70 mW
- Power-down standby mode - typically 3 mW
- Automatic power-down.
- TTL or CMOS compatible digital interfaces.
- Maximizes line interface card circuit density.

CMOS

MONOLITHIC SERIAL INTERFACE CODEC/FILTER WITH RECEIVE POWER AMPLIFIER

CASE J20A



20 Lead Cavity
J SUFFIX
CERDIP PACKAGE

PIN ASSIGNMENT

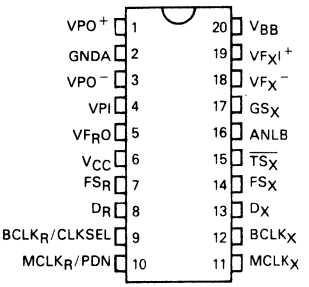
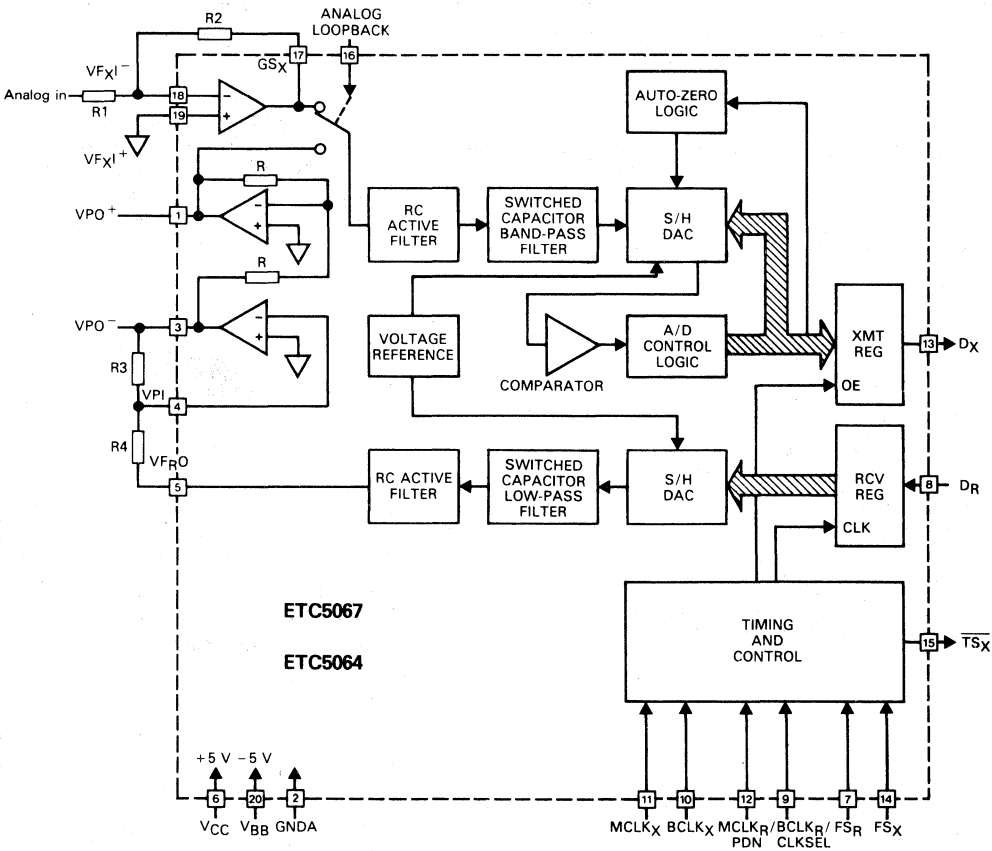


FIGURE 1 - BLOCK DIAGRAM



PIN DESCRIPTION

NAME	PIN TYPE *	N°	DESCRIPTION
VPO^+	O	1	The non-inverted output of the receive power amplifier.
GNDA	GND	2	Analog ground. All signals are referenced to this pin.
VPO^-	O	3	The inverted output of the receive power amplifier.
VPI	I	4	Inverting input to the receive power amplifier. Also powers down both amplifiers when connected to V_{BB}
VF_RO	O	5	Analog output of the receive filter.
V_{CC}	S	6	Positive power supply pin. $V_{CC} = +5\ V\ \pm 5\%$.
FS_R	I	7	Receive frame sync pulse which enables $BCLK_R$ to shift PCM data into D_R. FS_R is an 8 kHz pulse train. See Figures 2 and 3 for timing details.
D_R	I	8	Receive data input. PCM data is shifted into D_R following the FS_R leading edge.
$BCLK_R$/CLKSEL	I	9	The bit clock which shifts data into D_R after the FS_R leading edge. May vary from 64 kHz to 2.048 MHz. Alternatively, may be a logic input which selects either 1.536 MHz/1.544 MHz or 2.048 MHz for master clock in synchronous mode and $BCLK_X$ is used for both transmit and receive directions (see Table I).
$MCLK_R$/PDN	I	10	Receive master clock. Must be 1.536 MHz, 1.544 MHz or 2.048 MHz. May be synchronous with $MCLK_X$, but should be synchronous with $MCLK_X$ for best performance. When $MCLK_R$ is connected continuously low, $MCLK_X$ is selected for all internal timing. When $MCLK_R$ is connected continuously high, the device is powered down.
$MCLK_X$	I	11	Transmit master clock. Must be 1.536 MHz, 1.544 MHz or 2.048 MHz. May be asynchronous with $MCLK_R$
$BCLK_X$	I	12	The bit clock which shifts out the PCM data on D_X. May vary from 64 kHz to 2.048 MHz, but must be synchronous with $MCLK_X$
D_X	O	13	The TRI-STATE® PCM data output which is enabled by FS_X
FS_X	I	14	Transmit frame sync pulse input which enables $BCLK_X$ to shift out the PCM data on D_X. FS_X is an 8 kHz pulse train, see Figures 2 and 3 for timing details.
$\overline{TS_X}$	O	15	Open drain output which pulses low during the encoder time slot. Must to be grounded if not used
ANLB	I	16	Analog Loopback control input. Must be set to logic '0' for normal operation. When pulled to logic '1', the transmit filter input is disconnected form the output of the transmit preamplifier and connected to the VPO^+ output of the receive power amplifier.
GS_X	O	17	Analog output of the transmit input amplifier. Used to externally set gain.
VF_XI^-	I	18	Inverting input of the transmit input amplifier.
VF_XI^+	I	19	Non-inverting input of the transmit input amplifier.
V_{BB}	S	20	Negative power supply pin. $V_{BB} = -5\ V\ \pm 5\%$.

* I : Input, O : Output, S : Power supply.
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FUNCTIONAL DESCRIPTION

POWER-UP

When power is first applied, power-on reset circuitry initializes the COMBO and places it into the power-down mode. All non-essential circuits are deactivated and the D_X and VF_RO outputs are put in high impedance states. To power-up the device, a logical low level or clock must be applied to the $MCLK_R$/PDN pin and FS_X and/or FS_R pulses must be present. Thus, 2 power-down control modes are available. The first is to pull the $MCLK_R$/PDN pin high ; the alternative is to hold both FS_X and FS_R inputs continuously low. The device will power-down approximately 2 ms after the last FS_X or FS_R pulse. Power-up will occur on the first FS_X or FS_R pulse. The TRI-STATE PCM data output, D_X, will remain in the high impedance state until the second FS_X pulse.

SYNCHRONOUS OPERATION

For synchronous operation, the same master clock and bit clock should be used for both the transmit and receive directions. In this mode, a clock must be applied to $MCLK_X$ and the $MCLK_R$/ PDN pin can be used as a power-down control. A low level on $MCLK_R$/PDN powers up the device and a high level powers down the device. In either case, $MCLK_X$ will be selected as the master clock for both the transmit and receive circuits. A bit clock must also be applied to $BCLK_X$ and the $BCLK_R$/CLKSEL can be used to select the proper internal divider for a master clock of 1.536 MHz, 1.544 MHz or 2.048 MHz. For 1.544 MHz operation, the device automatically compensates for the 193rd clock pulse each frame.
With a fixed level on the $BCLK_R$/CLKSEL pin, $BCLK_X$ will be selected as the bit clock for both the transmit and receive directions. Table 1 indicates the frequencies of operation which can be selected, depending on the state of $BCLK_R$/CLKSEL. In this synchronous mode, the bit clock, $BCLK_X$, may be from 64 kHz to 2.048 MHz, but must be synchronous with $MCLK_X$.

TABLE 1 - SELECTION OF MASTER CLOCK FREQUENCIES

$BCLK_R$/CLKSEL	Master clock frequency selected	
	ETC5067	ETC5064
Clocked	2.048 MHz	1.536 MHz or 1.544 MHz
0	1.536 MHz or 1.544 MHz	2.048 MHz
1 (or open circuit)	2.048 MHz	1.536 MHz or 1.544 MHz

Each FS_X pulse begins the encoding cycle and the PCM data from the previous encode cycle is shifted out of the enabled D_X output on the positive edge of $BCLK_X$. After 8 bit clock periods, the TRI-STATE D_X output is returned to a high impedance state. With an FS_R pulse, PCM data is latched via the D_R input on the negative edge of $BCLK_X$(or $BCLK_R$ if running). FS_X and FS_R must be synchronous with $MCLK_X/_R$.

ASYNCHRONOUS OPERATION

For asynchronous operation, separate transmit and receive clocks may be applied. $MCLK_X$ and $MCLK_R$ must be 2.048 MHz for the ETC5067 , or 1.536 MHz, 1.544 MHz for the ETC5064 , and need not be synchronous. For best transmission performance, however, $MCLK_R$ should be synchronous with $MCLK_X$, which is easily achieved by applying only static logic levels to the $MCLK_R$/ PDN pin. This will automatically connect $MCLK_X$ to all internal $MCLK_R$ functions (see Pin Description). For 1.544 MHz operation, the device automatically compensates for the 193rd clock pulse each frame. FS_X starts each encoding cycle and must be synchronous with $MCLK_X$ and $BCLK_X$. FS_R starts each decoding cycle and must be synchronous with $BCLK_R$. $BCLK_R$ must be a clock, the logic levels shown in Table 1 are not valid in asynchronous mode. $BCLK_X$ and $BCLK_R$ may operate from 64 kHz to 2.048 MHz.

SHORT FRAME SYNC OPERATION

The COMBO can utilize either a short frame sync pulse or a long frame sync pulse. Upon power initialization, the device assumes a short frame mode. In this mode, both frame sync pulses, FS_X and FS_R, must be one bit clock period long, with timing relationships specified in Figure 3. With FS_X high during a falling edge of $BCLK_X$, the next rising edge of $BCLK_X$ enables the D_X TRI-STATE output buffer, which will output the sign bit. The following seven rising edges clock out the remaining seven bits, and the next falling edge disables the D_X output. With FS_R high during a falling edge of $BCLK_R$ ($BCLK_X$ in synchronous mode), the next falling edge of $BCLK_R$ latches in the sign bit. The following seven falling edges latch in the seven remaining bits. Both devices may utilize the short frame sync pulse in synchronous or asynchronous operating mode.

LONG FRAME SYNC OPERATION

To use the long frame mode, both the frame sync pulses, FS_X and FS_R, must be three or more bit clock periods long, with timing relationships specified in Figure 4. Based on the transmit frame sync. FS_X, the COMBO will sense whether short or long frame sync pulses are being used. For 64 kHz operation, the frame sync pulse must be kept low for a minimum of 160 ns (See Fig. 2). The D_X TRI-STATE output buffer is enabled with the rising edge of FS_X or the rising edge of

$BCLK_X$, whichever comes later, and the first bit clocked out is the sign bit. The following seven $BCLK_X$ rising edges clock out the remaining seven bits. The D_X output is disabled by the falling $BCLK_X$ edge following the eighth rising edge, or by FS_X going low, whichever comes later. A rising edge on the receive frame sync pulse, FS_R, will cause the PCM data at D_R to be latched in on the next eight falling edges of $BCLK_R$ ($BCLK_X$ in synchronous mode). Both devices may utilize the long frame sync pulse in synchronous or asynchronous mode.

TRANSMIT SECTION

The transmit section input is an operational amplifier with provision for gain adjustment using two external resistors, see Figure 5. The low noise and wide bandwidth allow gains in excess of 20 dB across the audio passband to be realized. The op amp drives a unity-gain filter consisting of RC active pre-filter, followed by an eighth order switched-capacitor bandpass filter clocked at 256 kHz. The output of this filter directly drives the encoder sample-and-hold circuit. The A/D is of companding type according to A-law (ETC5067) or μ law (ETC5064) coding conventions. A precision voltage reference is trimmed in manufacturing to provide an input overload (t_{MAX}) of nominally 2.5V peak (see table of Transmission Characteristics). The FS_X frame sync pulse controls the sampling of the filter output, and then the successive-approximation encoding cycle begins. The 8-bit code is then loaded into a buffer and shifted out through D_X at the next FS_X pulse. The total encoding delay will be approximately 165 μ s (due to the transmit filter) plus 125 μ s (due to encoding delay), which totals 290 μ s. Any offset voltage due to the filters or comparator is cancelled by sign bit integration.

RECEIVE SECTION

The receive section consists of an expanding DAC which drives a fifth order switched-capacitor low pass filter clocked at 256 kHz. The decoder is A-law (ETC5067) or μ -law (ETC5064) and the 5th order low pass filter corrects for the sin x/x attenuation due to the 8 kHz sample and hold. The filter is then followed by a 2nd order RC active post-filter and power amplifier capable of driving a 600 Ω load to a level of 7.2 dBm. The receive section is unity-gain. Upon the occurence of FS_R, the data at the D_R input is clocked in on the falling edge of the next eight $BCLK_R$ ($BCLK_X$) periods. At the end of the decoder time slot, the decoding cycle begins, and 10 μ s later the decoder DAC output is updated. The total decoder delay is ~10 μ s (decoder update) plus 110 μ s (filter delay) plus 62.5 μ s (1/2 frame), which gives approximately 180 μ s.

RECEIVE POWER AMPLIFIERS

Two inverting mode power amplifiers are provided for directly driving a matched line interface transformer. The gain of the first power amplifier can be adjusted to boost the $\pm$2.5 V peak output signal from the receive filter up $\pm$3.3 V peak into an unbalanced 300 Ω load, or $\pm$ 4.0 V into an unbalanced 15 kΩ load. The second power amplifier is internally connected in unity-gain inverting mode to give 6 dB of signal gain for balanced loads.

Maximum power transfer to a 600 Ω subscriber line termination is obtained by differentially driving a balanced transformer with a $\sqrt{2}$:1 turns ratio, as shown in Figure 2. A total peak power of 15.6 dBm can be delivered to the load plus termination.

Both power amplifiers can be powered down independently from the PDN input by connecting the VPI input to V_{BB}, saving approximately 12 mW of power.

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
V_{CC} to GNDA	V_{CC}	7	V
V_{BB} to GNDA	V_{BB}	−7	V
Voltage at any analog input or output	V_{IN}, V_{OUT}	V_{CC} +0.3 to V_{BB} −0.3	V
Voltage at any digital input or output		V_{CC} +0.3 to GNDA −0.3	V
Operating temperature range	T_{oper}	−25 to +125	°C
Storage temperature range	T_{stg}	−65 to +150	°C
Lead temperature (soldering, 10 seconds)		300	°C

ELECTRICAL CHARACTERISTICS

$V_{CC} = 5.0V \pm 5\%$, $V_{BB} = -5V \pm 5\%$, GNDA = 0V, $T_A = 0°C$ to $70°C$ (Unless otherwise noted); typical characteristics specified at $V_{CC} = 5.0V$, $V_{BB} = -5.0V$, $T_A = 25°C$; all signals are referenced to GNDA.

DIGITAL INTERFACE

Characteristic	Symbol	Min	Typ	Max	Unit
Input low voltage	V_{IL}	–	–	0.6	V
Input high voltage	V_{IH}	2.2	–	–	V
Output low voltage I_L=3.2mA D_X I_L=3.2mA, open drain $\overline{TS_X}$	V_{OL}	– –	– –	0.4 0.4	V
Output high voltage I_H=–3.2mA D_X	V_{OH}	2.4	–	–	V
Input low current (GNDA $\leq V_{IN} \leq V_{IL}$, all digital inputs)	I_{IL}	–10	–	10	μA
Input high current ($V_{IH} \leq V_{IN} \leq V_{CC}$)	I_{IH}	–10	–	10	μA
Output current in hight impedance state (TRI-STATE) (GNDA $\leq V_O \leq V_{CC}$) D_X	I_{OZ}	–10	–	10	μA

ANALOG INTERFACE WITH TRANSMIT INPUT AMPLIFIER (ALL DEVICES)

Input leakage current (–2.5V $\leq$ V $\leq$ +2.5V) VF_XI^+ or VF_XI^-	I_IXA	–200	–	200	nA
Input resistance (–2.5V $\leq$ V $\leq$ +2.5V) VF_XI^+ or VF_XI^-	R_IXA	10	–	–	MΩ
Output resistance (closed loop, unity gain)	R_OXA	–	1	3	Ω
Load resistance GS_X	R_LXA	10	–	–	kΩ
Load capacitance GS_X	C_LXA	–	–	50	pF
Output dynamic range ($R_L \geq 10k\Omega$) GS_X	V_OXA	± 2.8	–	–	V
Voltage gain (VF_XI^+ to GS_X)	A_VXA	5000	–	–	V/V
Unity gain bandwidth	F_UXA	.1	2	–	MHz
Offset voltage	$V_{OS}XA$	–20	–	20	mV
Common-mode voltage	$V_{CM}XA$	–2.5	–	2.5	V
Common-mode rejection ratio	CMRRXA	60	–	–	dB
Power supply rejection ratio	PSRRXA	60	–	–	dB

ANALOG INTERFACE WITH RECEIVE FILTER (ALL DEVICES)

Output resistance VF_RO	R_ORF	–	1	3	Ω
Load resistance (VF_RO= ± 2.5V)	R_LRF	10	–	–	kΩ
Load capacitance	C_LRF	–	–	25	PF
Output DC offset voltage	VOS_RO	–200	–	200	MV

ANALOG INTERFACE WITH POWER AMPLIFIERS (All devices)

Input leakage current (–1.0 V $\leq$ VPI $\leq$ 1.0 V)	IPI	–100	–	100	nA
Input resistance (–1.0 V $\leq$ VPI $\leq$ 1.0 V)	RIPI	10	–	–	MΩ
Input offset voltage	VIOS	–25	–	25	mV
Output resistance (inverting unity-gain at VPO^+ or VPO^-)	ROP	–	1	–	Ω
Unity-gain bandwidth, open loop (VPO^-)	F_C	–	400	–	kHz
Load capacitance (VPO^+ or VPO^- to GNDA) $R_L \geq 1500\ \Omega$ $R_L = 600\ \Omega$ $R_L = 300\ \Omega$	C_LP	– – –	– – –	100 500 1000	pF
Gain VPO^- to VPO^+ to GNDA, level at VPO^- = 1.77 Vrms (+3 dBmO)	GAp^+		–1	–	V/V
Power supply rejection of V_{CC} or V_{BB} (VPO^- connected to VPI) 0 kHz - 4 kHz 0 kHz - 50 kHz	$PSRR_P$	60 36	– –	– –	dB

POWER DISSIPATION (ALL DEVICES)

Power-down current	$I_{CC}0$	–	0.5	1.5	mA
Power-down current	$I_{BB}0$	–	0.05	0.3	mA
Active current	$I_{CC}1$	–	7.0	10.0	mA
Active current	$I_{BB}1$	–	7.0	10.0	mA

TIMING SPECIFICATIONS

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency of master clocks Depends on the device used and the $BCLK_R$/CLKSEL Pin $MCLK_X$ and $MCLK_R$	$1/t_{PM}$	– – –	1.536 1.544 2.048	– – –	MHz
Width of master clock high $MCLK_X$ and $MCLK_R$	t_{WMH}	160	–	–	ns
Width of master clock low $MCLK_X$ and $MCLK_R$	t_{WML}	160	–	–	ns
Rise time of master clock $MCLK_X$ and $MCLK_R$	t_{RM}	–	–	50	ns
Fall time of master clock $MCLK_X$ and $MCLK_R$	t_{FM}	–	–	50	ns
Period of bit clock	t_{PB}	485	488	15.725	ns
Width of bit clock high (V_{IH}=2.2V)	t_{WBH}	160	–	–	ns
Width of bit clock low (V_{IL}=0.6V)	t_{WBL}	160	–	–	ns
Rise time of bit clock (t_{PB}=488ns)	t_{RB}	–	–	50	ns
Fall time of bit clock (t_{PB}=488ns)	t_{FB}	–	–	50	ns
Set-up time from $BCLK_X$ high to $MCLK_X$ falling edge. (First bit clock after the leading edge of FS_X)	t_{SBFM}	100	–	–	ns
Holding time from bit clock low to the frame sync (long frame only)	t_{HBF}	0	–	–	ns
Set-up time from frame sync to bit clock low (long frame only)	t_{SFB}	80	–	–	ns
Hold time from 3rd period of bit clock low to frame sync (long frame only) FS_X or FS_R	t_{HBFI}	100	–	–	ns
Delay time to valid data from FS_X or $BCLK_X$, whichever comes later and delay time from FS_X to data output disabled (C_L=0 pF to 150 pF)	t_{DZF}	20	–	165	ns
Delay time from $BCLK_X$ high to data valid (Load=150 pF plus 2 LSTTL loads)	t_{DBD}	0	–	150	ns
Delay time from $BCLK_X$ low to data output disabled	t_{DZC}	50	–	165	ns
Set-up time from D_R valid to $BCLK_{R/X}$ low	t_{SDB}	50	–	–	ns
Hold time from $BCLK_{R/X}$ low to D_R invalid	t_{HBD}	50	–	–	ns
Holding time from bit clock high to frame sync (short frame only)	t_{HOLD}	0	–	–	ns
Set-up time from $FS_{X/R}$ to $BCLK_{X/R}$ low (short frame sync pulse) - Note 1	t_{SF}	50	–	–	ns
Hold time from $BCLK_{X/R}$ low to $FS_{X/R}$ low (short frame sync pulse) - Note 1	t_{HF}	100	–	–	ns
Delay time to TS_X low (load=150 pF plus 2 LSTTL loads)	t_{XDP}	–	–	140	ns
Minimum width of the frame sync pulse (low level) (64k bit/s operating mode)	t_{WFL}	160	–	–	ns

Note 1 : For short frame sync timing, FS_X and FS_R must go high while their respective bit clocks are high.

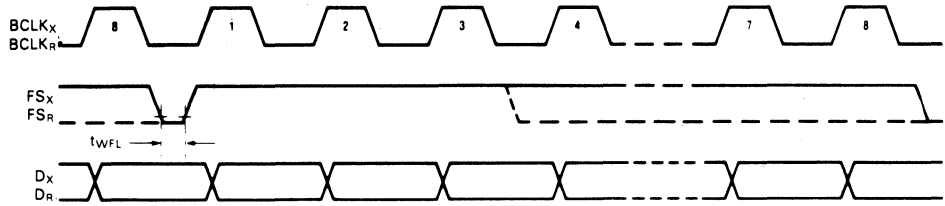


FIGURE 2 - 64 k bits/s TIMING DIAGRAM (See next page for complete timing)

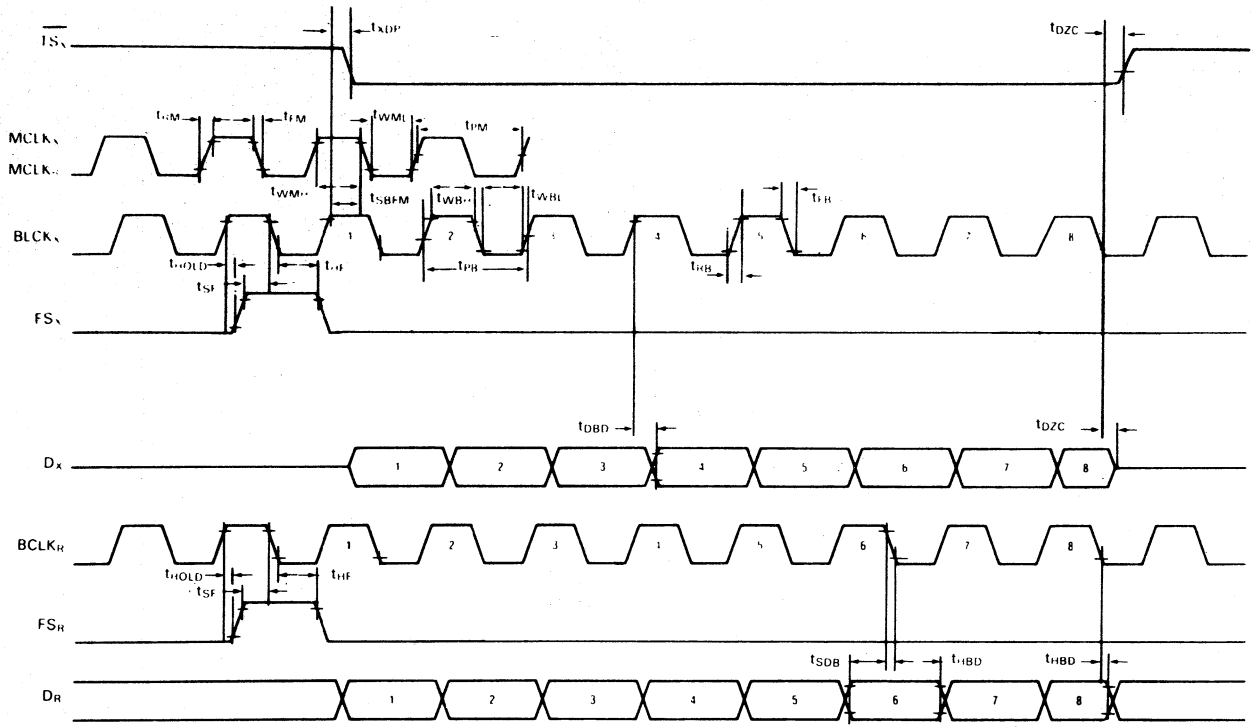


FIGURE 3 - SHORT FRAME SYNC TIMING

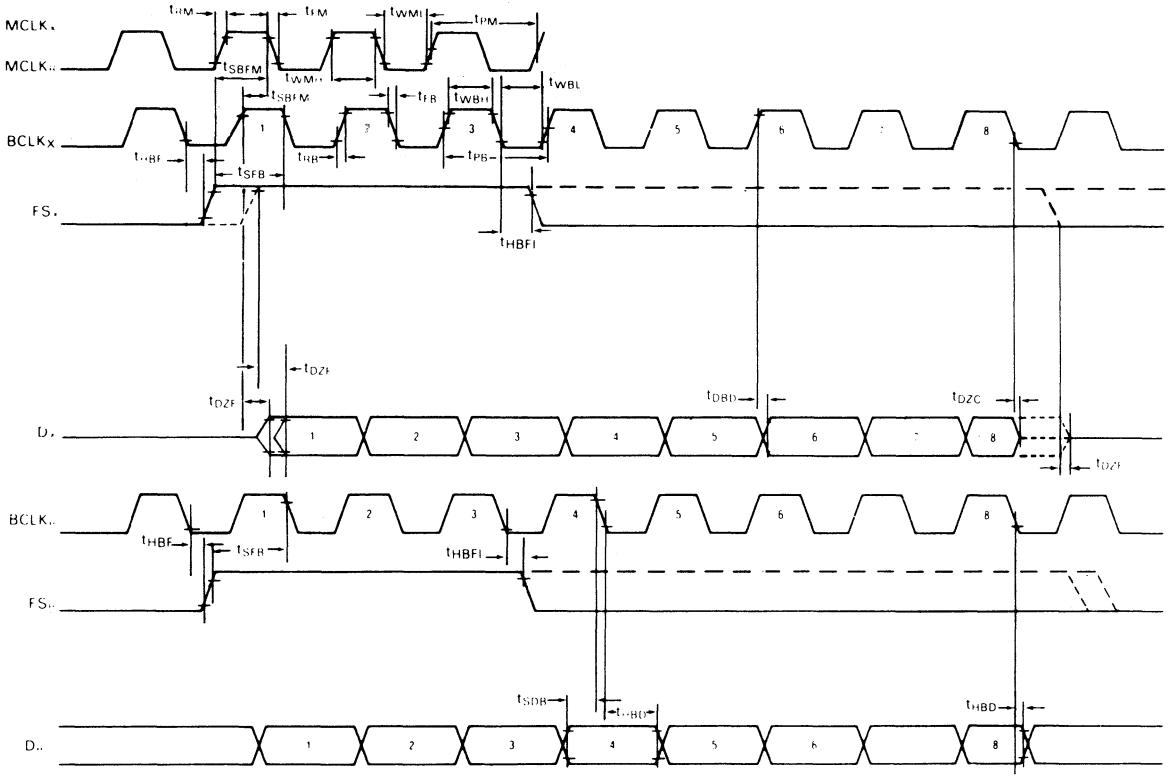


FIGURE 4 - LONG FRAME SYNC TIMING

TRANSMISSION CHARACTERISTICS

(All devices) T_A = 0°C to 70°C, V_{CC} = 5V ± 5%, V_{BB} = −5V ± 5%, GNDA = 0V, f = 1.02 kHz, V_{IN} = 0 dBm0 transmit input amplifier connected for unity-gain non-inverting. (Unless otherwise specified)

AMPLITUDE RESPONSE

Characteristic	Symbol	Min	Typ	Max	Unit
Absolute levels - Nominal 0 dBm0 level is 4 dBm (600Ω) 0 dBm0 ETC5067, ETC5064		–	1.2276	–	Vrms
Max overload level 3.14 dBm0 ETC5067 3.17 dBm0 ETC5064	t_{MAX}	– –	2.492 2.501	– –	V_{PK}
Transmit gain, absolute (T_A = 25°C, V_{CC} = 5V, V_{BB} = −5V) Input at GS_X = 0 dBm0 at 1020 Hz	G_{XA}	−0.15	–	0.15	dB
Transmit gain, relative to G_{XA} f = 16Hz f = 50Hz f = 60Hz f = 180Hz f = 200Hz f = 300Hz-3000 Hz f = 3300Hz f = 3400Hz f = 4000Hz f = 4600Hz and up,measure reponse from 0Hz to 4000Hz	G_{XR}	 – – – −2.8 −1.8 −0.15 −0.35 −0.7 – –	 – – – – – – – – – –	 −40 −30 −26 −0.2 −0.1 0.15 0.05 0 −14 −32	dB
Absolute transmit gain variation with temperature (T_A = 0°C to +70°C)	G_{XAT}	–	–	± 0.1	dB
Absolute transmit gain variation with supply voltage (V_{CC} = 5V ± 5%, V_{BB} = −5V ± 5%)	G_{XAV}	–	–	± 0.05	dB
Transmit gain variations with level Sinusoidal test method reference level = −10dBm0 VF_XI^+ = −40dBm0 to +3dBm0 VF_XI^+ = −50dBm0 to −40dBm0 VF_XI^+ = −55dBm0 to −50dBm0	G_{XRL}	 −0.2 −0.4 −1.2	 – – –	 0.2 0.4 1.2	dB
Receive gain, absolute (T_A = 25°C, V_{CC} = 5V, V_{BB} = −5V) Input = digital code sequence for 0dBm0 signal at 1020Hz	G_{RA}	−0.15	–	0.15	dB
Receive gain, relative to G_{RA} f = 0Hz to 3000 Hz f = 3300Hz f = 3400Hz f = 4000Hz	G_{RR}	 −0.15 −0.35 −0.7 –	 – – – –	 0.15 0.05 0 −14	dB
Absolute receive gain variation with temperature (T_A = 0°C to +70°C)	G_{RAT}	–	–	± 0.1	dB
Absolute receive gain variation with supply voltage (V_{CC} = 5V± 5%, V_{BB} = −5V± 5%)	G_{RAV}	–	–	± 0.05	dB
Receive gain variations with level Sinusoidal test method;reference input PCM code corresponds to an ideally encoded −10dBm0 signal PCM level = −40dBm0 to +3dBm0 PCM level = −50dBm0 to −40dBm0 PCM level = −55dBm0 to −50dBm0	G_{RRL}	 −0.2 −0.4 −1.2	 – – –	 0.2 0.4 1.2	dB
Receive filter output at VF_RO R_L = 10 kΩ	V_{RO}	−2.5	–	2.5	V

TRANSMISSION CHARACTERISTICS

(All devices) $T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 5\%$, $V_{BB} = -5V \pm 5\%$, GNDA = 0V, f = 1.02 kHz, V_{IN} = 0 dBm0, transmit input amplifier connected for unity-gain non-inverting. (Unless otherwise specified)

ENVELOPE DELAY DISTORTION WITH FREQUENCY

Characteristic	Symbol	Min	Typ	Max	Unit
Transmit delay, absolute (f = 1600Hz)	D_{XA}	–	290	315	μs
Transmit delay, relative to D_{XA}	D_{XR}				μs
f = 500Hz-600Hz		–	195	220	
f = 600Hz-800Hz		–	120	145	
f = 800Hz-1000 Hz		–	50	75	
f = 1000Hz-1600Hz		–	20	40	
f = 1600Hz-2600Hz		–	55	75	
f = 2600Hz-2800Hz		–	80	105	
f = 2800Hz-3000Hz		–	130	155	
Receive delay, absolute (f = 1600Hz)	D_{RA}	–	180	200	μs
Receive delay, relative to D_{RA}	D_{RR}				μs
f = 500Hz-1000Hz		−40	−25	–	
f = 1000Hz-1600Hz		−30	−20	–	
f = 1600Hz-2600Hz		–	70	90	
f = 2600Hz-2800Hz		–	100	125	
f = 2800Hz-3000Hz		–	145	175	

NOISE

Transmit noise, P message weighted (ETC5067, $VF_XI^+ = 0V$)	N_{XP}	–	−74	−69 (Note 1)	dBm0p
Receive noise, P message weighted (ETC5067, PCM code equals positive zero)	N_{RP}	–	−82	−79	dBm0p
Transmit noise, C message weighted (ETC5064, $VF_XI^+ = 0V$)	N_{XC}	–	12	15	dBrnC0
Receive noise, C message weighted ETC5064 , PCM code equals alternating positive and negative zero	N_{RC}	–	8	11	dBrnC0
Noise, single frequency f = 0kHz to 100kHz, loop around measurement, $VF_XI^+ = 0Vrms$	N_{RS}	–	–	−53	dBm0
Positive power supply rejection, transmit $VF_XI^+ = 0Vrms$, $V_{CC} = 5.0V_{DC}+100mVrms$, f = 0kHz-50kHz	$PPSR_X$	40	–	–	dBp
Negative power supply rejection, transmit $VF_XI^+ = 0Vrms$, $V_{BB} = -5.0V_{DC}+100mVrms$ f = 0kHz-50kHz	$NPSR_X$	40	–	–	dBp
Positive power supply rejection, receive (PCM code equals positive zero, $V_{CC} = 5.0V_{DC}+100mVrms$)	$PPSR_R$				
f = 0Hz-4000Hz		40	–	–	dBp
f = 4kHz-25kHz		40	–	–	dB
f = 25kHz-50kHz		36	–	–	dB
Negative power supply rejection, receive (PCM code equals positive zero, $V_{BB} = -5.0V_{DC}+100mVrms$)	$NPSR_R$				
f = 0Hz-4000Hz		40	–	–	dBp
f = 4kHz-25kHz		40	–	–	dB
f = 25kHz-50kHz		36	–	–	dB

TRANSMISSION CHARACTERISTICS (Continued)
(All devices) $T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 5\%$, $V_{BB} = -5V \pm 5\%$, GNDA = 0V, f = 1.02 kHz, V_{IN} = 0 dBm0, transmit input amplifier connected for unity-gain non-inverting. (Unless otherwise specified)

Characteristic	Symbol	Min	Typ	Max	Unit
Spurious out-of-band signals at the channel output Loop around measurement, 0 dBm0, 300Hz-3400Hz input applied to VF_XI^+, measure individual image signals at VF_RO	SOS	–	–	-30	dB
4600Hz-7600Hz		–	–	-32	
7600Hz-8400Hz		–	–	-40	
8400Hz-100,000Hz		–	–	-32	
DISTORTION					
Signal to total distortion (sinusoidal test method)	STD_X or				dBp
Transmit or receive half-channel	STD_R				
Level = 3.0dBm0		33	–	–	
= 0dBm0 to −30dBm0		36	–	–	
= −40dBm0 XMT		29	–	–	
RCV		30	–	–	
= −55dBm0 XMT		14	–	–	
RCV		15	–	–	
Single frequency distortion, transmit	SFD_X	–	–	−46	dB
Single frequency distortion, receive	SFD_R	–	–	−46	dB
Intermodulation distortion Loop around measurement, VF_XI^+ = −4dBm0 to −21dBm0, two frequencies in the range 300Hz-3400Hz	IMD	–	–	−41	dB
CROSSTALK					
Transmit to receive crosstalk, 0dBm0 transmit level f = 300Hz-3400Hz, D_R = steady PCM code	CT_{X-R}	–	−90	−75	dB
Receive to transmit crosstalk, 0dBm0 receive level f = 300Hz-3400Hz, VF_XI = 0V	CT_{R-X}	–	−90	−70 (Note 2)	dB
POWER AMPLIFIERS					
Maximum 0 dBm0 level for better than ±0.1 dB linearity over the range 10 dBm0 to +3 dBm0 (balanced load, R_L connected between VPO^+ and VPO^-	V_{OL}				V_{rms}
R_L = 600 Ω		3.3	–	–	
R_L = 1200 Ω		3.5	–	–	
R_L = 30 kΩ		4.0	–	–	
Signal/distortion R_L = 600 Ω, 0 dBm0	S/Dp	50	–	–	dB

Note 1 : Measured by extrapdation from the distortion test result
Note 2 : CTMX is measured with a −40 dBm0 activating signal applied at VF_XI^+

ENCODING FORMAT AT D_X OUTPUT

	A-Law (includes even bit inversion)	μLaw
V_{IN}(at GS_X) = +Full-scale	1 0 1 0 1 0 1 0	1 0 0 0 0 0 0 0
V_{IN}(at GS_X) = 0V	1 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1	1 1 1 1 1 1 1 1 0 1 1 1 1 1 1 1
V_{IN}(at GS_X) = −Full-scale	0 0 1 0 1 0 1 0	0 0 0 0 0 0 0 0

APPLICATIONS INFORMATION

POWER SUPPLIES

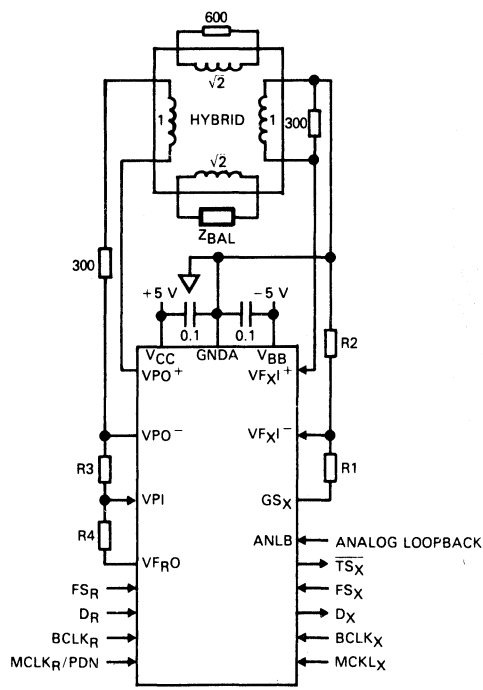
While the pins ot the ETC5060 family are well protected against electrical misuse, it is recommended that the standard CMOS practice be followed, ensuring that ground is connected to the device before any other connections are made. In applications where the printed circuit board may be plugged into a "hot" socket with power and clocks already present, an extra long ground pin in the connector is useful.

All ground connections to each device should meet at a common point as close as possible to the GNDA pin. This minimizes the interaction of ground return currents flowing through a common bus impedance. 0.1 μF supply decoupling capacitors should be connected from this common ground point to V_{CC} and V_{BB}.

For best performance, the ground point of each CODEC/FILTER on a card should be connected to a common card ground in start formation, rather than via a ground bus. This common ground point should be decoupled to V_{CC} and V_{BB} with 10 μF capacitors.

For best performance either, $\overline{TSX}$ should be grounded if not used.

TYPICAL ASYNCHRONOUS APPLICATION

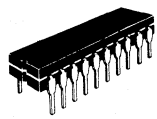


Note 1 : Transmit gain $= 20 \times \log\left(\frac{R1+R2}{R2}\right)$, $(R1+R2) \geq 10\ k\Omega$

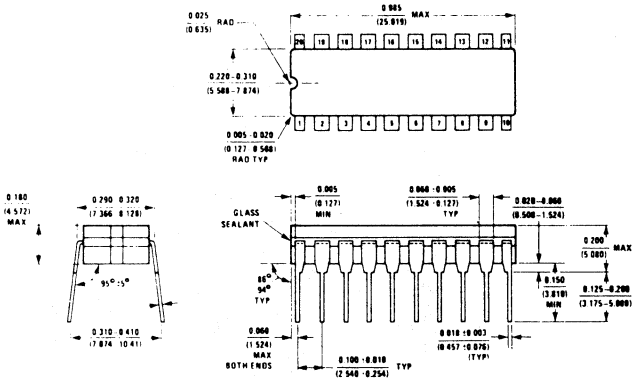
Note 2 : Receive gain $= 20 \times \log\left(\frac{2 \times R3}{R4}\right)$, $R4 \geq 10\ k\Omega$

FIGURE 2

CASE J20A



20 Lead Cavity
J SUFFIX
CERDIP PACKAGE



THOMSON COMPONENTS
MOSTEK

MK5116(J,N)

-255 LAW COMPANDING CODEC

COMMUNICATIONS PRODUCTS

FEATURES

- ☐ ±5-Volt Power Supplies
- ☐ Low Power Dissipation - 30mW (Typ)
- ☐ Follows the μ-255 Companding Law
- ☐ Synchronous or Asynchronous Operation
- ☐ On-chip sample and hold
- ☐ On-Chip Offset Null Circuit Eliminates Long-Term Drift Errors and Need for Trimming
- ☐ Single 16-Pin Package
- ☐ Minimal External Circuity Required
- ☐ Serial Data Output of 64kb/s—2.1 Mb/s at 8kHz Sampling Rate
- ☐ Separate Analog and Digital Grounding Pins Reduce System Noise Problems

DESCRIPTION

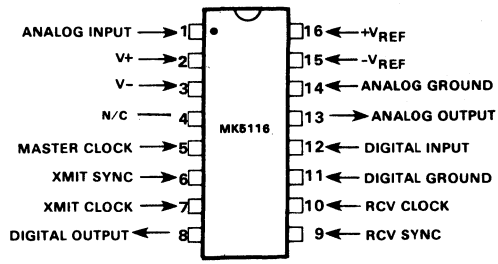
The MK5116 is a monolithic CMOS companding CODEC which contains two sections: (1) An analog-to-digital converter which has a transfer characteristic conforming to the μ-255 companding law and (2) a digital-to-analog converter which also conforms to the μ-255 law.

These two sections form a coder-decoder which is designed to meet the needs of the telecommunications industry for per-channel voice-frequency codecs used in telephone digital switching and transmission systems. Digital input and output are in serial format. Actual transmission and reception of 8-bit data words containing the analog information is done at a 64kb/s-2.1 Mb/s rate with analog signal sampling occurring at an 8kHz rate. A sync pulse input is provided for synchronizing transmission and reception of multi-channel information being multiplexed over a single transmission line.

The pin configuration of the MK5116 is shown in Figure 1.

PIN CONNECTIONS

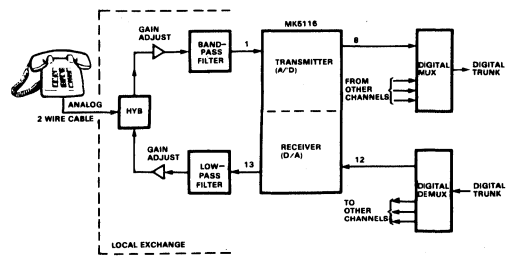
Figure 1



A block diagram of a PCM system using the MK5116 is shown in Figure 2.

PCM SYSTEM BLOCK DIAGRAM

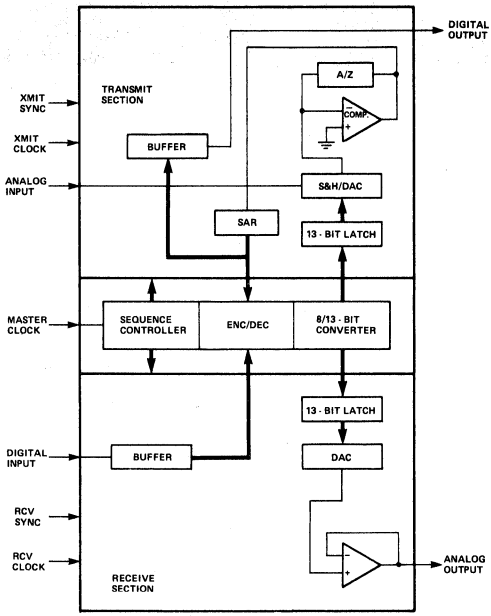
Figure 2



FUNCTIONAL DESCRIPTION: (Refer to Figure 3 for a Block Diagram)

MK5116 BLOCK DIAGRAM

Figure 3



POSITIVE AND NEGATIVE REFERENCE VOLTAGES ($+V_{REF}$ and $-V_{REF}$) Pins 16 and 15

These inputs provide the conversion references for the digital-to-analog converters in the MK5116. $+V_{REF}$ and $-V_{REF}$ must maintain 100ppM/°C regulation over the operating temperature range. Variation of the reference directly affects system gain.

ANALOG INPUT, Pin 1

Voice-frequency analog signals which are bandwidth-limited to 4kHz are input at this pin. Typically, they are then sampled at an 8kHz rate (refer to Figure 4). The analog input must remain between $+V_{REF}$ and $-V_{REF}$ for accurate conversion. The recommended input interface circuit is shown in Figure 9.

MASTER CLOCK, Pin 5

This signal provides the basic timing and control signals required for all internal conversions. It does not have to be synchronized with RCV SYNC, RCV CLOCK, XMIT SYNC, or XMIT CLOCK and is not internally related to them.

XMIT SYNC, Pin 6 (Refer to Figure 10 for the Timing Diagram)

This input is synchronized with XMIT CLOCK. When XMIT SYNC goes high, the digital output is activated, and the A/D conversion begins on the next positive edge of MASTER CLOCK. The conversion by MASTER CLOCK can be asynchronous with XMIT CLOCK. The serial output data is clocked out by the positive edges of XMIT CLOCK. The negative edge of XMIT SYNC causes the digital output to become three-state. XMIT SYNC may remain high longer than 8 XMIT CLOCK cycles, but must go low for at least 1 master clock before the transmission of the next digital word (refer to Figure 12).

XMIT CLOCK, Pin 7 (Refer to Figure 10 for the Timing Diagram)

The on-chip 8-bit output shift register of the MK5116 is unloaded at the clock rate present on this pin. Clock rates of 64kHz-2.1MHz can be used for XMIT CLOCK. The positive edge of the INTERNAL CLOCK transfers the data from the master to the slave of a master-slave flip-flop (refer to the Figure 5). If the positive edge of XMIT SYNC occurs after the positive edge of XMIT CLOCK, XMIT SYNC will determine when the first positive edge of INTERNAL CLOCK will occur. In this event, the hold time for the first clock pulse is measured from the positive edge of XMIT SYNC.

RVC SYNC, Pin 9 (Refer to Figure 11 for the Timing Diagram)

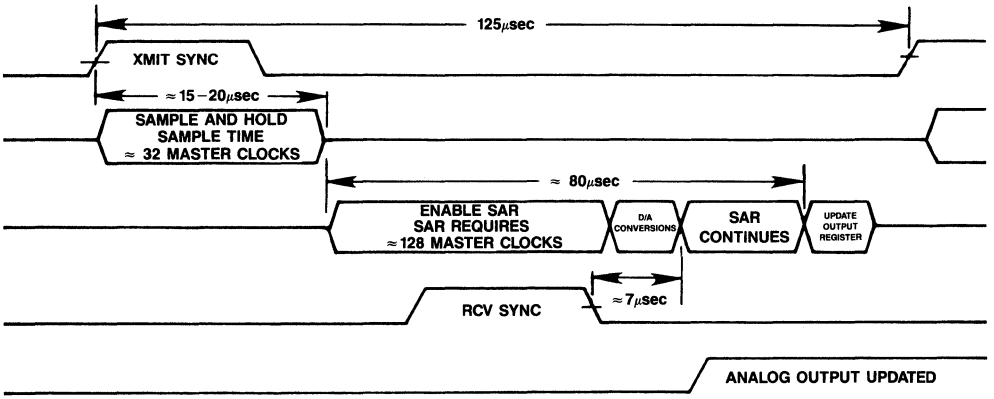
This input is synchronized with RCV CLOCK, and serial data is clocked in by RCV CLOCK. Duration of the RCV SYNC pulse is approximately 8 RCV CLOCK periods. The conversion from digital to analog starts after the negative edge of the RCV SYNC pulse (refer to Figure 4). The negative edge of RCV SYNC should occur before the 9th positive clock edge to insure that only eight bits are clocked in. RCV SYNC must stay low for 17 MASTER CLOCKS (min.) before the next digital word is to be received (refer to Figure 13).

RCV CLOCK, Pin 10 (Refer to Figure 11 for Timing Diagram)

The on-chip 8-bit shift register for the MK5116 is loaded at the clock rate present on this pin. Clock rates of 64kHz-2.1MHz can be used for RCV CLOCK. Valid data should be applied to the digital input before the positive edge of the internal clock (refer to Figure 5). This set up time, t_{RDS}, allows the data to be transferred into the MASTER of a master-slave flip-flop. A hold time, t_{RDH}, is required to complete this transfer. If the rising edge of RCV SYNC occurs after the first rising edge of RCV CLOCK, RCV SYNC will determine when the first positive edge of INTERNAL CLOCK will occur. In this event, the set-up

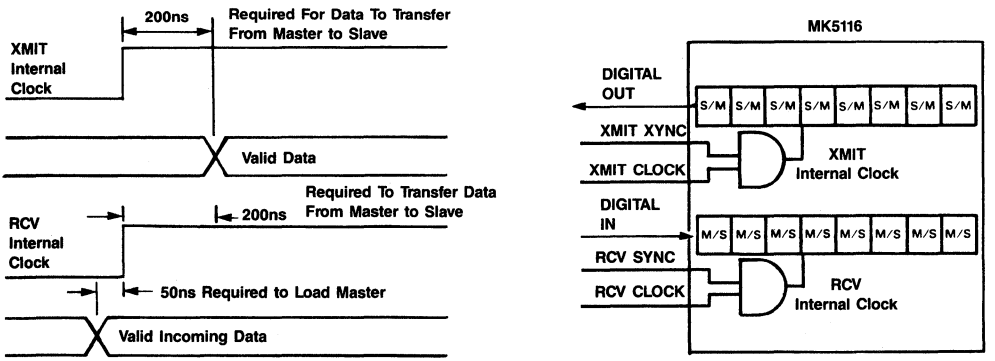
A/D, D/A CONVERSION TIMING

Figure 4



DATA INPUT/OUTPUT TIMING

Figure 5



and hold times for the first clock pulse should be measured from the positive edge of RCV SYNC.

DIGITAL OUTPUT, Pin 8

The MK5116 output register stores the 8-bit encoded sample of the analog input. This 8-bit word is shifted out under control of XMIT SYNC and XMIT CLOCK. When XMIT SYNC is low, the DIGITAL OUTPUT is an open circuit. When XMIT SYNC is high, the state of the DIGITAL OUTPUT is determined by the value of the output bit in the serial shift register. The output is composed of a Sign Bit, 3 Chord Bits, and 4 Step Bits. The Sign Bit indicates the polarity of the analog input while the Chord and Step Bits indicate the magnitude. In the first Chord, the Step Bit has a value of 0.6mV. In the second Chord, the Step Bit has a value of 1.2mV. This doubling of the step value continues for each of the six successive Chords.

Each Chord has a specific value; and the Step Bits, 16 in each Chord, specify the displacement from that value (refer to Table 1). Thus the output, which follows the μ-255 law, has resolution that is proportional to the input level rather than to full scale. This provides the resolution of a 12-bit A/D converter at low input levels and that of a 6-bit converter as the input approaches full scale. The transfer characteristic of the A/D converter (μ-law Encoder) is shown in Figure 6.

DIGITAL INPUT, Pin 12

The MK5116 input register accepts the 8-bit sample of an analog value and loads it under control of RCV SYNC and RCV CLOCK. The timing diagram is shown in Figure 11. When RCV SYNC goes high, the MK5116 uses RCV

DIGITAL OUTPUT CODE μ-LAW

Table 1

	Chord Code	Chord Value	Step Value
1.	000	0.0mV	0.613mV
2.	001	10.11mV	1.226mV
3.	010	30.3mV	2.45mV
4.	011	70.8mV	4.90mV
5.	100	151.7mV	9.81mV
6.	101	313mV	19.61mV
7.	110	637mV	39.2mV
8.	111	1.284V	78.4mV

EXAMPLE:

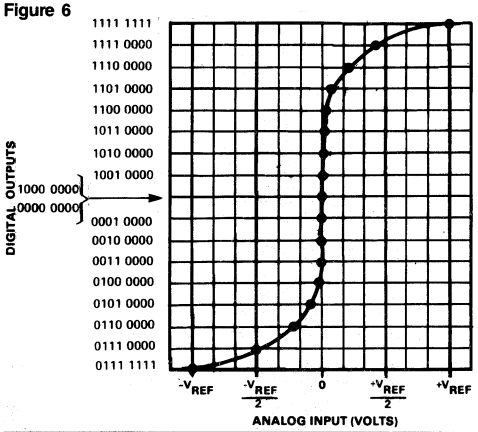
1 011 0010 = + 70.8mV + (2×4.90mV)

Sign Bit Chord Step Bits

If the sign bit were a zero, then both plus signs would be changed to minus signs.

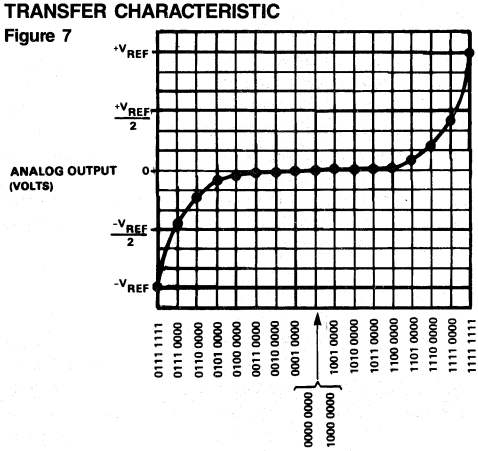
A/D CONVERTER (μ-Law Encoder) TRANSFER CHARACTERISTIC

Figure 6



D/A CONVERTER (μ-Law Decoder) TRANSFER CHARACTERISTIC

Figure 7



CLOCK to clock the serial data into its input register. RCV SYNC goes low to indicate the end of serial input data. The 8 bits of the input data have the same functions described for the DIGITAL OUTPUT. The transfer characteristic of the D/A converter (μ-Law Decoder) is shown in Figure 7.

ANALOG OUTPUT, Pin 13

The analog output is in the form of voltage steps (100% duty cycle) having amplitude equal to the analog sample which was encoded. This waveform is then filtered with an external low-pass filter with sinx/x correction to recreate the sampled voice signal.

OPERATION OF CODEC WITH 64kHz XMIT/RCV CLOCK FREQUENCIES

XMIT/RCV SYNC must not be allowed to remain at a logic "1" state. XMIT SYNC is required to be at a logic "0" state for 1 master-clock period (min.) before the next digital word is transmitted. RCV SYNC is required to be at a logic "0" state for 17 master-clock periods (min.) before the next digital word is received (refer to Figures 12 and 13).

OFFSET NULL

The offset-null feature of the MK5116 eliminates long-term drift errors and conversion errors due to temperature changes by going through an offset-adjustment cycle before every conversion, thus guaranteeing accurate A/D conversion for inputs near ground. There is no offset adjust of the output amplifier because the resultant DC error ($V_{OFFSET0}$) will have no effect, since the output is intended to be AC-coupled to the external filter. The sign is not used to null the analog input. Therefore, for an analog input of 0 volts, the sign bit will be stable.

PERFORMANCE EVALUATION

The equipment connections shown in Figure 8 can be used to evaluate the performance of the MK5116. An analog signal provided by the HP3551A Transmission Test Set is connected to the Analog Input (Pin 1) of the MK5116. The Digital Output of the CODEC is tied back to the Digital Input, and the Analog Output is fed through a low-pass filter to the HP3551A. Remaining pins of the MK5116 are connected as follows:

(1) RCV SYNC is tied to XMIT SYNC
(2) XMIT CLOCK is tied to MASTER CLOCK. The signal is inverted and tied to RCV CLOCK.

The following timing signals are required:

(1) MASTER CLOCK = 1.536 MHz
(2) XMIT SYNC repetition rate = 8kHz
(3) XMIT SYNC width = 8 XMIT CLOCK periods

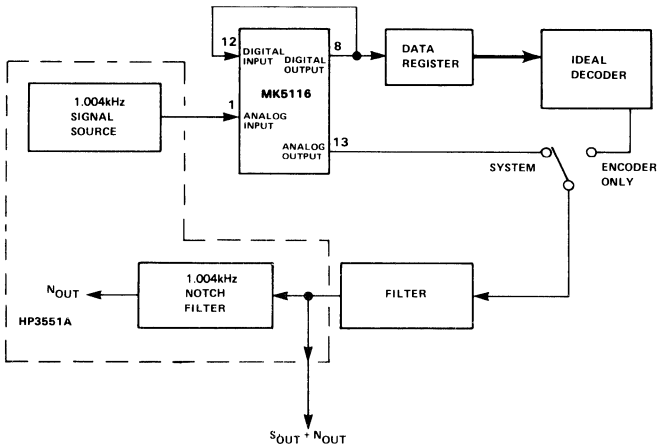
When all the above requirements are met, the setup of

Figure 8 permits the measurement of synchronous system performance over a wide range of analog inputs. The data register and ideal decoder provide a means of checking the encoder portion of the MK5116 independently of the decoder section. To test the system in the asynchronous mode, MASTER CLOCK should be separated from XMIT CLOCK, and MASTER CLOCK should be separated from RCV CLOCK. XMIT and RCV SYNCS are also separated.

Some experimental results obtained with the MK5116 are shown in Figure 14 and Figure 15. In each case, both the measured results and the corresponding D3 Channel Bank specifications are shown. The MK5116 exceeds the requirements for Signal-to-Distortion ratio (Figure 14) and for Gain Tracking (Figure 15).

SYSTEM CHARACTERISTICS TEST CONFIGURATION

Figure 8



NOTE: The ideal decoder consists of a digital decompander and a 13-bit precision DAC.

ABSOLUTE MAXIMUM RATINGS

DC Supply Voltage, V+ . . . . . +6V
DC Supply Voltage, V− . . . . . −6V
Ambient Operating Temperature, T_A . . . . . 0°C to 70°C
Storage Temperature . . . . . −55°C to +125°C
Package Dissipation at 25°C (Derated 9mW/°C when soldered into PCB) 500mW
Digital Input . . . . . $-0.5V \leq V_{IN} \leq V+$
Analog Input . . . . . $V- \leq V_{IN} \leq V+$
$+V_{REF}$ . . . . . $-0.5V \leq +V_{REF} \leq V+$
$-V_{REF}$ . . . . . $V- \leq -V_{REF} \leq +0.5V$

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damages to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may effect device reliability.

ELECTRICAL OPERATING CHARACTERISITCS
POWER SUPPLY REQUIREMENTS

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V+	Positive Supply Voltage	4.75	5.0	5.25	V	
V−	Negative Supply Voltage	−5.25	−5.0	−4.75	V	
$+V_{REF}$	Positive Reference Voltage	2.375	2.5	2.625	V	1
$-V_{REF}$	Negative Reference Voltage	−2.625	−2.5	−2.375	V	1

TEST CONDITIONS: V+ = 5.0V, V− = −5.0V, $+V_{REF}$ = 2.5V, $-V_{REF}$ = −2.5V, T_A = 0°C to 70°C

DC CHARACTERISTICS

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
R_{INAS}	Analog Input Resistance During Sampling		2		kΩ	2
R_{INANS}	Analog Input Resistance Non-Sampling		100		MΩ	
C_{INA}	Analog Input Capacitance		150	250	pF	2
$V_{OFFSET/1}$	Analog Input Offset Voltage		±1	±8	mV	2
R_{OUTA}	Analog Output Resistance		1	10	Ω	
I_{OUTA}	Analog Output Current	0.25	0.5		mA	
$V_{OFFSET/0}$	Analog Output Offset Voltage		+20	±850	mV	
I_{INLOW}	Logic Input Low Current (V_{IN} = 0.8V) Digital Input, Clock Input, Sync Input		±0.1	±10	μA	3
I_{INHIGH}	Logic Input High Current (V_{IN} = 2.4V) Digital Input, Master and RCV Clock Input, RCV Sync Input		±0.1	±10	μA	3
I_{INHIGH_X}	Logic Input High Current (V_{In} = 2.4V) TX Clock, TX Sync		−.25	−0.8	mA	3
C_{DO}	Digital Output Capacitance		8	12	pF	
I_{DOL}	Digital Output Leakage Current		±0.1	±10	μA	
V_{OUTLOW}	Digital Output Low Voltage			0.4	V	4
$V_{OUTHIGH}$	Digital Output High Voltage	3.9			V	4
I+	Positive Supply Current		4	10	mA	5
I−	Negative Supply Current		2	6	mA	5
I_{REF+}	Positive Reference Current		4	20	μA	
I_{REF-}	Negative Reference Current		4	20	μA	

AC CHARACTERISTICS (Refer to Figure 10 and Figure 11)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
F_M	Master Clock Frequency	1.5	1.544	2.1	MHz	
F_R, F_X	XMIT, RCV Clock Frequency	0.064	1.544	2.1	MHz	
PW_{CLK}	Clock Pulse Width (MASTER, XMIT, RCV)	200			ns	
t_{RC}, t_{FC}	Clock Rise, Fall Time (MASTER, XMIT, RCV)			25% of PW_{CLK}	ns	
t_{RS}, t_{FS}	Sync Rise, Fall Time (XMIT, RCV)			25% of PW_{CLK}	ns	
t_{DIR}, t_{DIF}	Data Input Rise, Fall Time			25% of PW_{CLK}	ns	
t_{WSX}, t_{WSR}	Sync Pulse Width (XMIT RCV)		$\frac{8}{F_X(F_R)}$		μs	

AC CHARACTERISTICS (Refer to Figure 10 and Figure 11)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
t_{PS}	Sync Pulse Period (XMIT, RCV)		125		μs	
t_{XCS}	XMIT Clock-to-XMIT Sync Delay	50% of t_{FC} (t_{RS})			ns	6
t_{XCSN}	XMIT Clock-to-XMIT Sync (Negative Edge) Delay	200			ns	
t_{XSS}	XMIT Sync Set-Up Time	200			ns	
t_{XDD}	XMIT Data Delay	0		200	ns	4
t_{XDP}	XMIT Data Present	0		200	ns	4
t_{XDT}	XMIT Data Three State			150	ns	4
t_{DOF}	Digital Output Fall Time		50	100	ns	4
t_{DOR}	Digital Output Rise Time		50	100	ns	4
t_{SRC}	RVC Sync-to-RCV Clock Delay	50% of t_{RC} (t_{FS})			ns	6
t_{RDS}	RCV Data Set-Up Time	50			ns	7
t_{RDH}	RCV Data Hold Time	200			ns	7
t_{RCS}	RCV Clock-to-RCV Sync Delay	200			ns	
t_{RSS}	RCV Sync Set-Up Time	200			ns	7
t_{SAO}	RCV Sync-to-Analog Output Delay		7		μs	
SLEW+	Analog Output Positive Slew Rate		1		V/μs	
SLEW−	Analog Output Negative Slew Rate		1		V/μs	
DROOP	Analog Output Droop Rate		25		μV/μs	

AC CHARACTERISTICS (Refer to Figures 14 and 15)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	TEST COND.
GT_X	Gain Tracking Transmit	−.2 −.4 −1.25	0.0 ±0.1 ±0.2	+.2 +.4 +1.25	dB dB dB	Analog Input=+3 to −37dBm0 Analog Input=−37 to −50dBm0 Analog Input =−50 to −55dBm0 Relative to 0 dBm0
GT_R	Gain Tracking Receive	−.2 −.4 −1.25	0.0 ±0.1 ±0.2	±.2 +.4 +1.25	dB dB dB	Input Level=+3 to −37dBm0 Input Level=−37 to −50dBm0 Input Level=−50 to −55dBm0 Relative to 0 dBm0
GT_{E-E}	Gain Tracking End to End	−.4 −.8 −2.50	0.0 ±0.1 ±0.2	+.4 +.8 +2.50	dB dB dB	Analog Input=+3 to −37dBm0 Analog Input=−37 to −50dBm0 Analog Input=−50 to −55dBm0 Relative to 0 dBm0
SD_X	Signal to Distortion Transmit	37 31 26			dB dB dB	Analog Input=0 to −30dBm0 Analog Input= −40dBm0 Analog Input= −45dBm0
SD_R	Signal to Distortion Receive	37 31 26			dB dB dB	Input Level=0 to −30dBm0 Input Level= −40dBm0 Input Level= −45dBm0

AC CHARACTERISTICS (Refer to Figures 14 and 15)

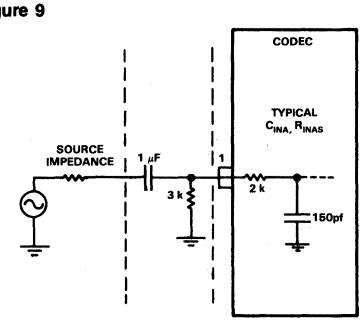
SYM	PARAMETER	MIN	TYP	MAX	UNITS	TEST COND.
SD_{E-E}	Signal to Distortion End to End	35 29 24			dB dB dB	Analog Input=0 to −30 dBm0 Analog Input= −40 dBm0 Analog Input= −45 dBm0
N_X	Idle Channel Noise Transmit			17	dBnc0	Analog Input=0 Volts
N_R	Idle Channel Noise Receive			0	dBnc0	Digital Input=0 Code
N_{E-E}	Idle Channel Noise End to End			18	dBnc0	Analog Input=0 Volts Digital Output to Digital Input
CT_{RX}	Crosstalk Receive to Transmit			−80	dB	Analog In= −50 dBm0 at 2600 H_Z Digital Input= 0 dBm0 at 1008 H_Z digital
CT_{XR}	Crosstalk Transmit to Receive			−80	dB	Analog In=0 dBm0 at 1008 H_Z Digital Input=0 Code
TLP	Transmission Level Point		+4		dB	600Ω

NOTES:

1. $+V_{REF}$ and $-V_{REF}$ must be matched within ± 1% in order to meet system requirements.
2. Sampling is accomplished by charging an internal capacitor; therefore, the designer should avoid excessive source impedance. Input-related device characteristics are derived using the Recommended Analog Input Circuit. See Figure 9.
3. When a transition from a "1" to a "0" takes place, the user must sink the "1" current until reaching the "0" level.
4. Driving 30pF with I_{OH} = 100μA, I_{OL} = 500μA.
5. Results in 30 mW typical power dissipation (clocks applied) under normal operating conditions.
6. This delay is necessary to avoid overlapping CLOCK and SYNC.
7. The first bit of data is loaded when the Sync and Clock are both "1" during bit time 1 as shown on RCV timing diagram.

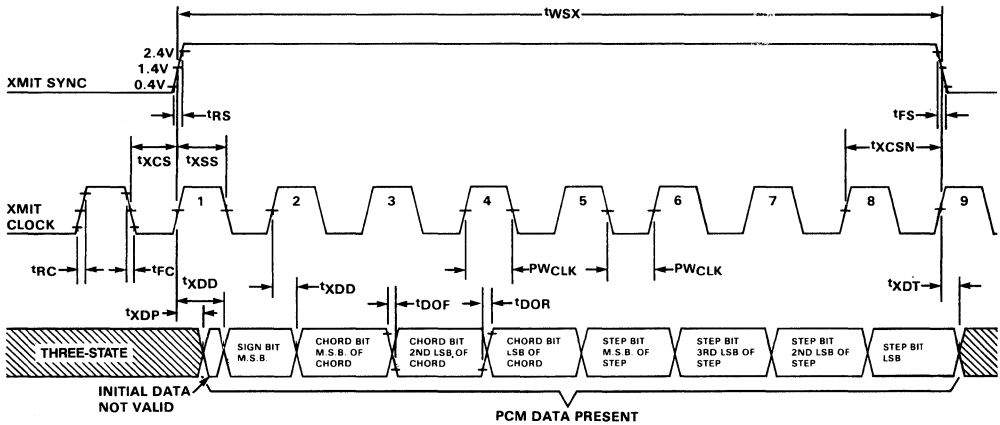
RECOMMENDED ANALOG INPUT CIRCUIT

Figure 9



TRANSMITTER SECTION TIMING

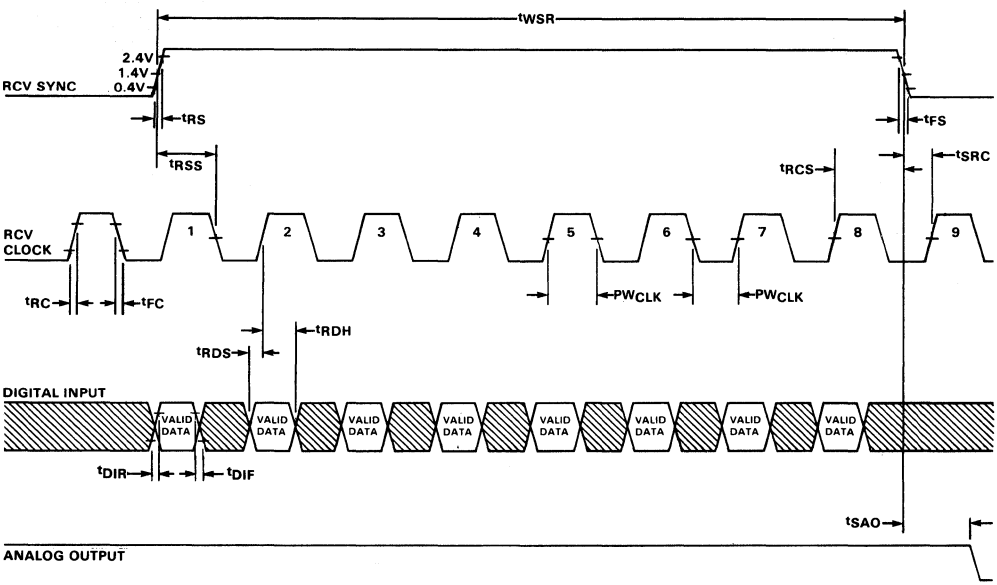
Figure 10



NOTE: All rise and fall times are measured from 0.4V and 2.4V. All delay times are measured from 1.4V.

RECEIVER SECTION TIMING

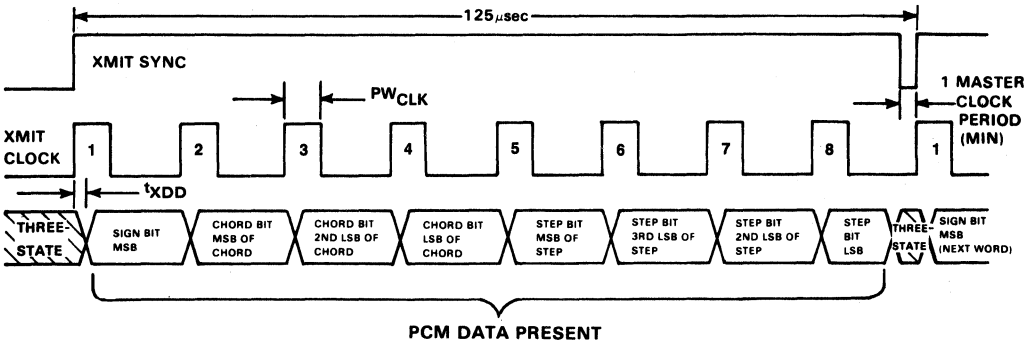
Figure 11



NOTE: All rise and fall times are measured from 0.4V and 2.4V. All delay times are measured from 1.4V.

64kHz OPERATION, TRANSMITTER SECTION TIMING

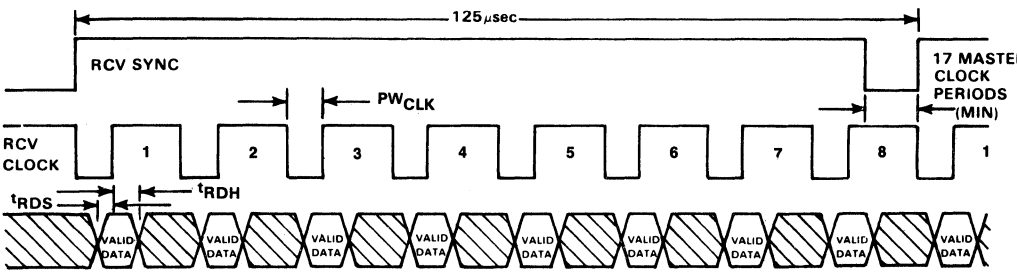
Figure 12



NOTE: All rise and fall times are measured from 0.4V and 2.4V. All delay times are measured from 1.4V.

64kHz OPERATION, RECEIVER SECTION TIMING

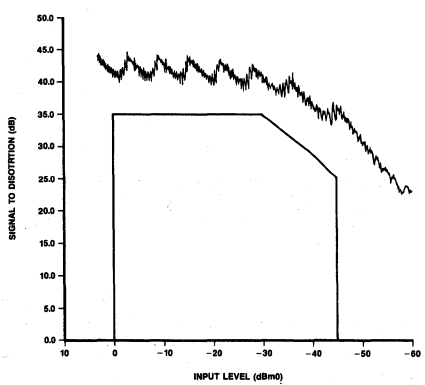
Figure 13



NOTE: All rise and fall times are measured from 0.4V and 2.4V. All delay times are measured from 1.4V.

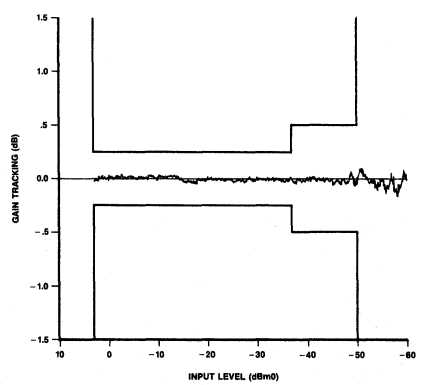
MK5116 SINGLE-ENDED SIGNAL TO DISTORTION

Figure 14



MK5116 SINGLE-ENDED GAIN TRACKING

Figure 15



THOMSON COMPONENTS
MOSTEK

MK5151(J,P)

-255 LAW COMPANDING CODEC

COMMUNICATIONS PRODUCTS

FEATURES

- ±5-Volt Power Supplies
- Low Power Dissipation - 30mW (Typ)
- **Follows the μ-255 Companding Law**
- Zero Code Suppression and Sign-Magnitude Data Format
- On-Chip Sample and Hold
- On-Chip Offset Null Circuit Eliminates Long-Term Drift Errors and Need for Trimming
- Single 24-Pin Package
- Minimal External Circuitry Required
- Serial Data Output of 64kb/s - 2.1Mb/s at 8kHz Sampling Rate
- Separate Analog and Digital Grounding Pins Reduce System Noise Problems

DESCRIPTION

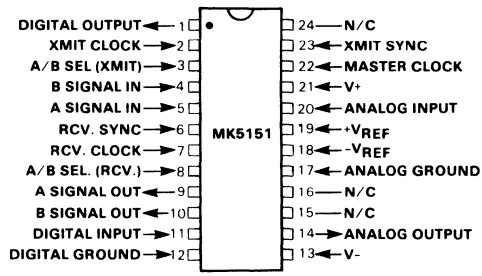
The MK5151 is a monolithic CMOS companding CODEC which contains two sections: (1) An analog-to-digital converter which has a transfer characteristic conforming to the μ-255 companding law and (2) a digital-to-analog converter which also conforms to the μ-255 law.

These two sections form a coder-decoder which is designed to meet the needs of the telecommunications industry for per-channel voice-frequency codecs used in telephone digital switching and transmission systems. Digital input and output are in serial format. Actual transmission and reception of 8-bit data words containing the analog information is done at a 64kb/s-2.1 Mb/s rate with analog signal sampling occuring at an 8kHz rate. A sync pulse input is provided for synchronizing transmission and reception of multi-channel information being multiplexed over a single transmission line.

The pin configuration of the MK5151 is shown in Figure 1.

PIN CONNECTIONS

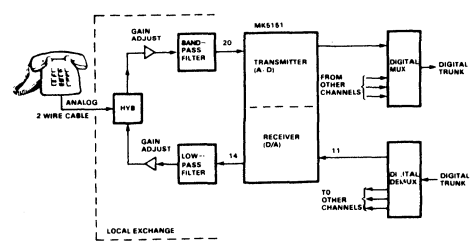
Figure 1



A block diagram of a PCM system using the MK5151 is shown in Figure 2.

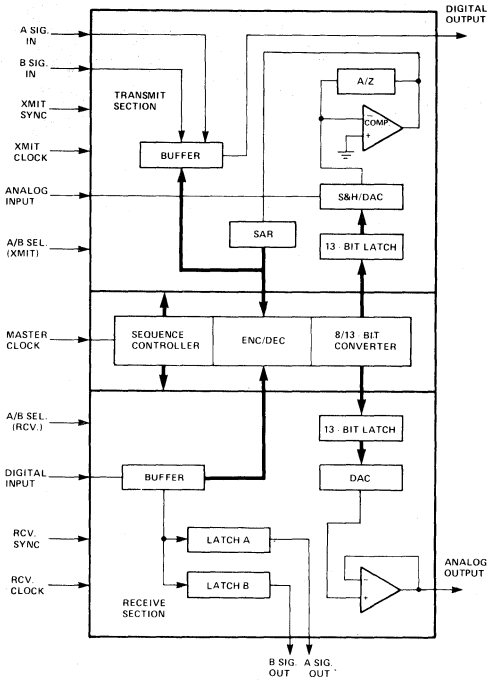
PCM SYSTEM BLOCK DIAGRAM

Figure 2



FUNCTIONAL DESCRIPTION: (Refer to Figure 3 for a Block Diagram)

MK5151 BLOCK DIAGRAM
Figure 3



POSITIVE AND NEGATIVE REFERENCE VOLTAGES ($+V_{REF}$ and $-V_{REF}$) Pins 19 and 18

These inputs provide the conversion references for the digital-to-analog converters in the MK5151. $+V_{REF}$ and $-V_{REF}$ must maintain 100ppM/°C regulation over the operating temperature range. Variation of the reference directly affects system gain.

ANALOG INPUT, Pin 20

Voice-frequency analog signals which are bandwidth-limited to 4kHz are input at this pin. Typically, they are then sampled at an 8kHz rate (Refer to Figure 4.). The analog input must remain between $+V_{REF}$ and $-V_{REF}$ for accurate conversion. The recommended input interface circuit is shown in Figure 11.

MASTER CLOCK, Pin 22

This signal provides the basic timing and control signals required for all internal conversions. It does not have to be synchronized with RCV. SYNC, RCV. CLOCK, XMIT SYNC or XMIT CLOCK and is not internally related to them.

XMIT SYNC, Pin 23 (Refer to Figure 12 for the Timing Diagram)

This input is synchronized with XMIT CLOCK. When XMIT SYNC goes high, the digital output is activated and the A/D conversion begins on the next positive edge of MASTER CLOCK. The conversion by MASTER CLOCK can be asynchronous with XMIT CLOCK. The serial output data is clocked out by the positive edges of XMIT CLOCK. The negative edge of XMIT SYNC causes the digital output to become three-state. XMIT SYNC must go low for at least 1 master clock prior to the transmission of the next digital word. (Refer to Figure 14).

XMIT CLOCK, Pin 2 (Refer to Figure 12 for the Timing Diagram)

The on-chip 8-bit output shift register of the MK5151 is unloaded at the clock rate present on this pin. Clock rates of 64kHz-2.1MHz can be used for XMIT CLOCK. The positive edge of the INTERNAL CLOCK transfers the data from the master to the slave of a master-slave flip-flop (Refer to Figure 5). If the positive edge of XMIT SYNC occurs after the positive edge of XMIT CLOCK, XMIT SYNC will determine when the first positive edge of INTERNAL CLOCK will occur. In this event, the hold time for the first clock pulse is measured from the positive edge of XMIT SYNC.

RCV. SYNC, Pin 6 (Refer to Figure 13 for the timing diagram)

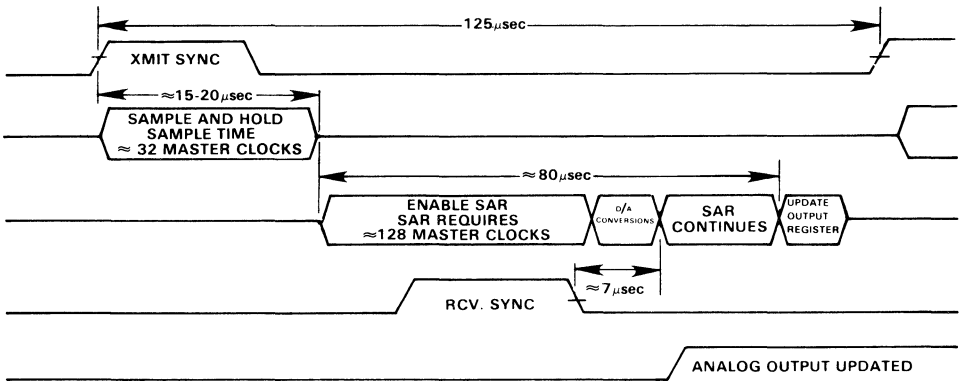
This input is synchronized with RCV. CLOCK and serial data is clocked in by RCV. CLOCK. Duration of the RCV. SYNC pulse is approximately 8 RCV. CLOCK periods. The conversion from digital-to-analog starts after the negative edge of the RCV. SYNC pulse (Refer to Figure 4). The negative edge of RCV. SYNC should occur before the 9th positive clock edge to insure that only eight bits are clocked in. RCV. SYNC must stay low for 17 MASTER CLOCKS (min.) before the next digital word is to be received (Refer to Figure 15).

RCV CLOCK, Pin 7 (Refer to Figure 13 for Timing Diagram)

The on-chip 8-bit shift register for the MK5151 is loaded at the clock rate present on this pin. Clock rates of 64kHz-2.1MHz can be used for RCV. CLOCK. Valid data should be applied to the digital input before the positive edge of the internal clock (Refer to Figure 5). This set up time, t_{RDS}, allows the data to be transferred into the MASTER of a master-slave flip-flop. The positive edge of the INTERNAL CLOCK transfers the data to the SLAVE of the master-slave flip-flop. A hold time, t_{RDH}, is required to complete this transfer. If the rising edge of RCV. SYNC occurs after the first rising edge of RCV. CLOCK, RCV. SYNC will determine when the first positive edge of INTERNAL CLOCK will occur. In this

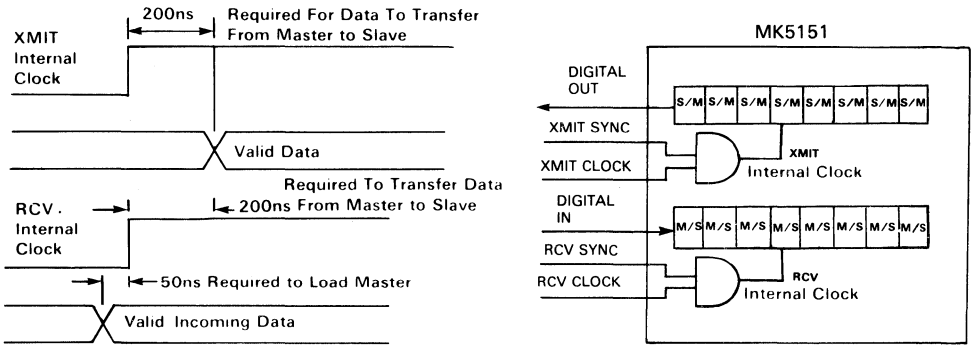
A/D, D/A CONVERSION TIMING

Figure 4



DATA INPUT/OUTPUT TIMING

Figure 5



event, the set-up and hold times for the first clock pulse should be measured from the positive edge of RCV. SYNC.

DIGITAL OUTPUT, Pin 1

The MK5151 output register stores the 8-bit encoded sample of the analog input. This 8-bit word is shifted out under control of XMIT SYNC and XMIT CLOCK. When XMIT SYNC is low, the DIGITAL OUTPUT is an open circuit. When XMIT SYNC is high, the state of the DIGITAL OUTPUT is determined by the value of the output bit in the serial shift register. The output is composed of a Sign Bit, 3 Chord Bits, and 4 Step Bits. The Sign Bit indicates the polarity of the analog input while the Chord and Step Bits indicate the magnitude. In the first Chord, the Step Bit has a value of 0.6mV. In the second Chord, the Step Bit has a value of 1.2mV. This doubling of the step value continues for each of the six successive Chords.

Each Chord has a specific value and the Step Bits, 16 in each Chord, specify the displacement from that value (Refer to Table 1). Thus the output, which follows the μ-255 law, has resolution that is proportional to the input level rather than to full scale. This provides the resolution of a 12-bit A/D converter at low input levels and that of a 6-bit converter as the input approaches full scale. The transfer characteristic of the A/D converter (μ-law Encoder) is shown in Figure 6.

DIGITAL OUTPUT CODE μ-LAW

Table 1

	Chord Code	Chord Value	Step Value
1.	111	0.0mV	0.613mV
2.	110	10.11mV	1.226mV
3.	101	30.3mV	2.45mV
4.	100	70.8mV	4.90mV
5.	011	151.7mV	9.81mV
6.	010	313mV	19.61mV
7.	001	637mV	39.2mV
8.	000	1.284V	78.4mV

EXAMPLE:

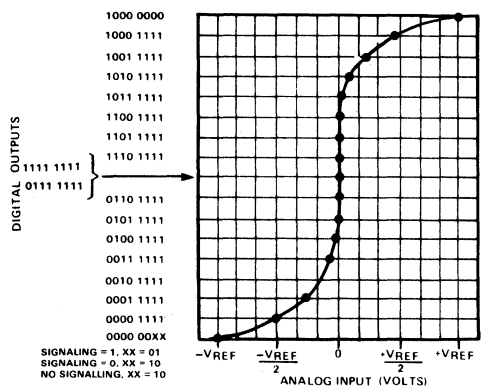
1 100 1101 = +70.8mV + (2 x 4.90mV)

Sign Bit Chord Step Bits

If the sign bit were a zero, then both plus signs would be changed to minus signs.

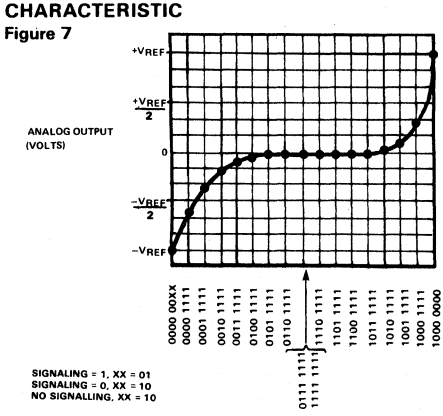
A/D CONVERTER (μ-Law Encoder) TRANSFER CHARACTERISTIC

Figure 6



D/A CONVERTER (μ-Law Decoder) TRANSFER CHARACTERISTIC

Figure 7



DIGITAL INPUT, Pin 11

The MK5151 input register accepts the 8-bit sample of an analog value and loads it under control of RCV. SYNC and RCV. CLOCK. The timing diagram is shown in Figure 13. When RCV. SYNC goes high, the MK5151 uses RCV. CLOCK to clock the serial data into its input register. RCV. SYNC goes low to indicate the end of serial input data. The 8 bits of the input data have the same functions described for the SERIAL OUTPUT. The transfer characteristic of the D/A converter (μ-law Decoder) is shown in Figure 7.

ANALOG OUTPUT, Pin 14

The analog output is in the form of voltage steps (100% duty cycle) having amplitude equal to the analog sample which was encoded. This waveform is then filtered with an external low-pass filter with sinx/x correction to recreate the sampled voice signal. When the 8th bit of the word is a signalling bit, it is assigned a value of ½ step. This results in a lower system quantization error rate than would result if the bit were arbitarily set to 0 (no step) or 1 (full step).

OPERATION OF CODEC WITH 64kHz XMIT/RCV. CLOCK FREQUENCIES

XMIT/RCV. SYNC must not be allowed to remain at a logic "1" state. XMIT SYNC is required to be at a logic "0" state for 1 master clock period (min.) before the next digital word is transmitted. RCV. SYNC is required to be at a logic "0" state for 17 master clock periods (min.) before the next digital word is received (Refer to Figures 14 and 15).

A/B SIGNAL IN, Pins 4 and 5

These two pins allow insertion of signalling information into the transmitted data stream. The inserted information occurs as the 8th bit (LSB) in the transmitted word. A positive transition occuring on A/B SEL (XMIT) selects A SIGNAL IN while a negative transition selects B SIGNAL IN.

A/B SIGNAL OUT, Pins 9 and 10

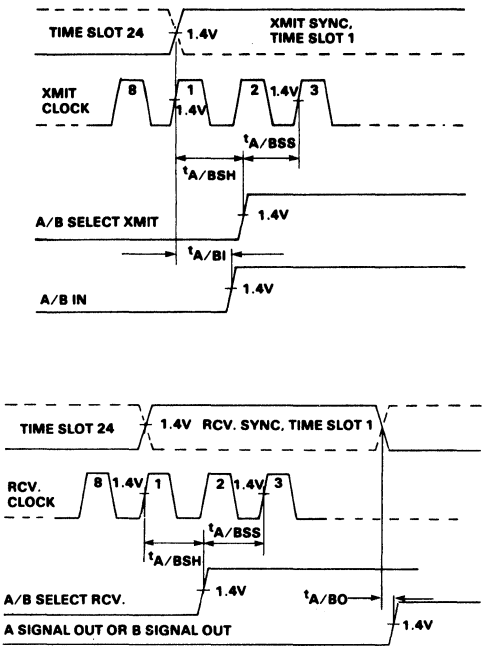
These two pins are provided to output received signalling information. A positive transition on A/B SEL (RCV.) routes the signal bit to A SIGNAL OUT while a negative transition routes the signal bit (bit 8) to B SIGNAL OUT. Refer to Figure 8.

A/B SEL (XMIT), Pin 3

This input selects either A SIGNAL IN or B SIGNAL IN as described in the A/B SIGNAL IN paragraph above, and should be changed only at the start of the 6th and 12th frames as shown in Figure 9.

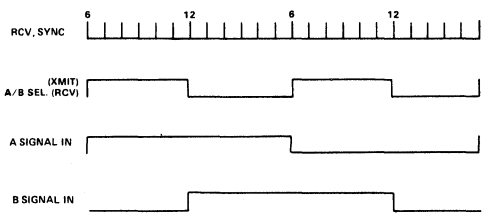
A/B SELECT TIMING

Figure 8



SIGNALLING TIMING REQUIREMENTS FOR PERFORMANCE EVALUATION

Figure 9



A/B SEL (RCV.), Pin 8

This input routes the signalling bit, bit 8, either to A SIGNAL OUT or to B SIGNAL OUT as described in the A/B SIGNAL OUT paragraph above, and should be changed only at the start of the 6th and 12th frames as shown in Figure 9.

OFFSET NULL

The offset null feature of the MK5151 eliminates long-term drift errors and conversion errors due to temperature changes by going through an offset adjustment cycle before every conversion, thus guaranteeing accurate A/D conversion for inputs near ground. There is no offset adjust of the output amplifier because, since the output is intended to be AC - coupled to the external filter, the resultant DC error ($V_{OFFSET/O}$) will have no effect. The sign bit is not used to null the analog input. Therefore, for an analog input of 0 volts, the sign bit will be stable.

PERFORMANCE EVALUATION

The equipment connections shown in Figure 10 can be used to evaluate the performance of the MK5151. An analog signal provided by the HP3551A Transmission Test Set is connected to the Analog Input (Pin 20) of the MK5151. The Digital Output of the CODEC is tied back to the Digital Input and the Analog Output is fed through a low-pass filter to the HP3551A. Remaining pins of the MK5151 are connected as follows:

(1) A/B SEL. (RCV.) is tied to A/B SEL. (XMIT).
(2) RCV. SYNC is tied to XMIT SYNC.
(3) XMIT CLOCK is tied to MASTER CLOCK. The signal is inverted and tied to RCV. CLOCK.

The following timing signals are required:

(1) MASTER CLOCK = 1.536 MHz
(2) XMIT SYNC repetition rate = 8kHz
(3) XMIT SYNC width = 8 MASTER CLOCK periods

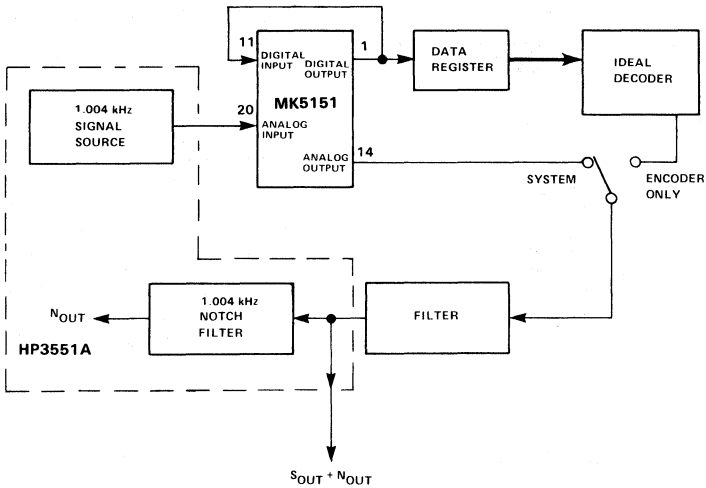
Additional timing signals are shown in Figure 9.

When all the above requirements are met, the setup of Figure 10 permits the measurement of synchronous system performance over a wide range of analog inputs. The data register and ideal decoder provide a means of checking the encoder portion of the MK5151 independently of the decoder section. To test the system in the asynchronous mode, MASTER CLOCK should be separated from XMIT CLOCK and MASTER CLOCK should be separated from RCV. CLOCK. XMIT CLOCK and RCV. CLOCK are separated also.

Some experimental results obtained with the MK5151 are shown in Figure 16 and Figure 17. In each case, both the measured results and the corresponding D3 Channel Bank specifications are shown. The MK5151 exceeds the requirements for Signal-to-Distortion ratio (Figure 17) and for Gain Tracking (Figure 16).

SYSTEM CHARACTERISTICS TEST CONFIGURATION

Figure 10



NOTE: The ideal decoder consists of a digital decompander and a 13-bit precision DAC.

ABSOLUTE MAXIMUM RATINGS

DC Supply Voltage, V+ ..... +6V
DC Supply Voltage, V– ..... –6V
Ambient Operating Temperature, T_A ..... 0°C to 70°C
Storage Temperature ..... –55°C to +125°C
Package Dissipation at 25°C (Derated 9mW/°C when soldered into PCB) 500mW
Digital Input ..... $-0.5V \leq V_{IN} \leq V+$
Analog Input ..... $V- \leq +V_{IN} \leq V+$
$+V_{REF}$ ..... $-0.5V \leq +V_{REF} \leq V+$
$-V_{REF}$ ..... $V- \leq -V_{REF} \leq 0.5V$

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL OPERATING CHARACTERISTICS
POWER SUPPLY REQUIREMENTS

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V+	Positive Supply Voltage	4.75	5.0	5.25	V	
V–	Negative Supply Voltage	–5.25	–5.0	–4.75	V	
$+V_{REF}$	Positive Reference Voltage	2.375	2.5	2.625	V	1
$-V_{REF}$	Negative Reference Voltage	–2.625	–2.5	–2.375	V	1

TEST CONDITIONS: V+ = 5.0 V, V- = -5.0 V, + V_{REF} = 2.5 V, -V_{REF} = -2.5 V, T_A = 0°C to 70°C
DC CHARACTERISTICS

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
R_{INAS}	Analog Input Resistance During Sampling		2		kΩ	2
R_{INANS}	Analog Input Resistance Non-Sampling		100		MΩ	
C_{INA}	Analog Input Capacitance		150	250	pF	2

DC CHARACTERISTICS CONTINUED

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
$V_{OFFSET/I}$	Analog Input Offset Voltage		±1	±8	mV	2
R_{OUTA}	Analog Output Resistance		20	50	Ω	
I_{OUTA}	Analog Output Current	0.25	0.5		mA	
$V_{OFFSET/O}$	Analog Output Offset Voltage		-200	± 850	mV	
I_{INLOW}	Logic Input Low Current (V_{IN} = 0.8V) Digital Input, Clock Input, Sync Input		± 0.1	±10	μA	3
I_{INHIGH}	Logic Input High Current (V_{IN} = 2.4V) Digital Input, Clock Input, Sync Input		-0.25	-0.8	mA	3
C_{DO}	Digital Output Capacitance		8	12	pF	
I_{DOL}	Digital Output Leakage Current		± 0.1	±10	μA	
V_{OUTLOW}	Logic Output Low Voltage Digital Output, A/B Signal Out			0.4	V	4
$V_{OUTHIGH}$	Logic Output High Voltage Digital Output, A/B Signal Out	3.9			V	4
I+	Positive Supply Current		4	10	mA	5
I–	Negative Supply Current		2	6	mA	5
I_{REF+}	Positive Reference Current		4	20	μA	
I_{REF-}	Negative Reference Current		4	20	μA	

AC CHARACTERISTICS (Refer to Figure 12 and Figure 13)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
F_M	Master Clock Frequency	1.5	1.544	2.1	MHz	
F_R, F_X	Receive, Transmit Clock Frequency	0.064	1.544	2.1	MHz	
PW_{CLK}	Clock Pulse Width (MASTER, XMIT, RCV.)	200			ns	
t_{RC}	Clock Rise Time (MASTER, XMIT, RCV.)			25% of PW_{CLK}	ns	
t_{RS}, t_{FS}	Sync Fall, Rise Time (XMIT, RCV.)			25% of PW_{CLK}	ns	
t_{DIR}, t_{DIF}	Digital Input Rise, Fall Time			25% of PW_{CLK}	ns	
t_{WSX}, t_{WSR}	Sync Pulse Width (XMIT, RCV.)		$\frac{8}{F_X(F_R)}$		μs	
t_{PS}	Sync Pulse Period (XMIT, RCV.)		125		μs	
t_{XCS}	XMIT Clock-to-XMIT Sync Delay	50%of t_{FC} (t_{RS})			ns	6
t_{XCSN}	XMIT Clock-to-XMIT Sync (Negative Edge) Delay	200			ns	
t_{XSS}	XMIT Sync Set-Up Time	250			ns	
t_{XDD}	XMIT Data Delay	0		200	ns	4
t_{XDP}	XMIT Data Present	0		200	ns	4
t_{XDT}	XMIT Data Three State			150	ns	4
t_{DOF}	Digital Output Fall Time		50	100	ns	4
t_{DOR}	Digital Output Rise Time		50	100	ns	4

AC CHARACTERISTICS CONTINUED (Refer to Figure 12 and 13)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
t_{SRC}	RCV. Sync-to-RCV. Clock Delay	50% of t_{RC} (t_{FS})			ns	6
t_{RDS}	RCV. Data Set-Up Time	50			ns	7
t_{RDH}	RCV. Data Hold Time	200			ns	7
t_{RCS}	RCV. Clock-to-RCV. Sync Delay	200			ns	
t_{RSS}	RCV. Sync Set-Up Time	200			ns	7
t_{SAO}	RCV. Sync-to-Analog Output Delay		7		μs	
$t_{A/BI}$	A/B Signalling Input Setup Time			200	ns	
$t_{A/BSH}$	A/B Select Hold Time	200			ns	
$t_{A/BSS}$	A/B Select Setup Time	400			ns	
$t_{A/BO}$	A/B Signalling Output Delay		200	400	ns	
SLEW+	Analog Output Positive Slew Rate		1		V/μs	
SLEW–	Analog Output Negative Slew Rate		1		V/μs	
DROOP	Analog Output Droop Rate		25		μV/μs	

SYSTEM CHARACTERISTICS (Refer to Figures 16 and 17)

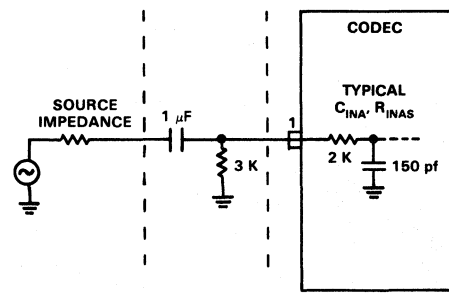
SYM	PARAMETER	MIN	TYP	MAX	UNITS	TEST COND.
S/D	Signal-to-Distortion Ratio	35 29 24	39 34 29		dB dB dB	Analog Input=0 to -30dBm0 Analog Input=-40dBm0 Analog Input=-45dm0
GT	Gain Tracking	-0.4 -0.8 -2.5	±0.1 ±0.1 ±0.2	+0.4 +0.8 +2.5	dB dB dB	Analog Input=+3 to -37dBm0 Analog Input=-37 to -50dBm0 Analog Input=-50 to -55dBm0
N_{IC}	Idle Channel Noise		10	18	dBrnc0	Analog Input=0 Volts Note 2
TLP	Transmission Level Point		+4		dB	600Ω

NOTES:

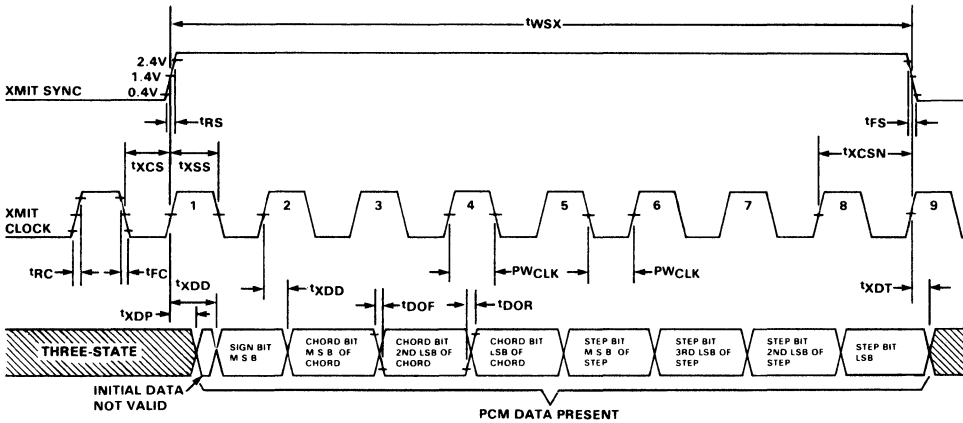
1. $+V_{REF}$ and $-V_{REF}$ must be matched within ± 1% in order to meet system requirements.
2. Sampling is accomplished by charging an internal capacitor; therefore, the designer should avoid excessive source impedance. Input related device characteristics are derived using the Recommended Analog Input Circuit. See Figure 11.
3. When a transition from a "1" to a "0" takes place, the user must sink the "1" current until reaching the "0" level.
4. Driving 30pF with $I_{OH} = -100\mu A$, $I_{OL} = 500\mu A$.
5. Results in 30 mW typical power dissipation (clocks applied) under normal operating conditions.
6. This delay is necessary to avoid overlapping CLOCK and SYNC.
7. The first bit of data is loaded when the Sync and Clock are both "1" during bit time 1 as shown on RCV timing diagram.

RECOMMENDED ANALOG INPUT CIRCUIT

Figure 11

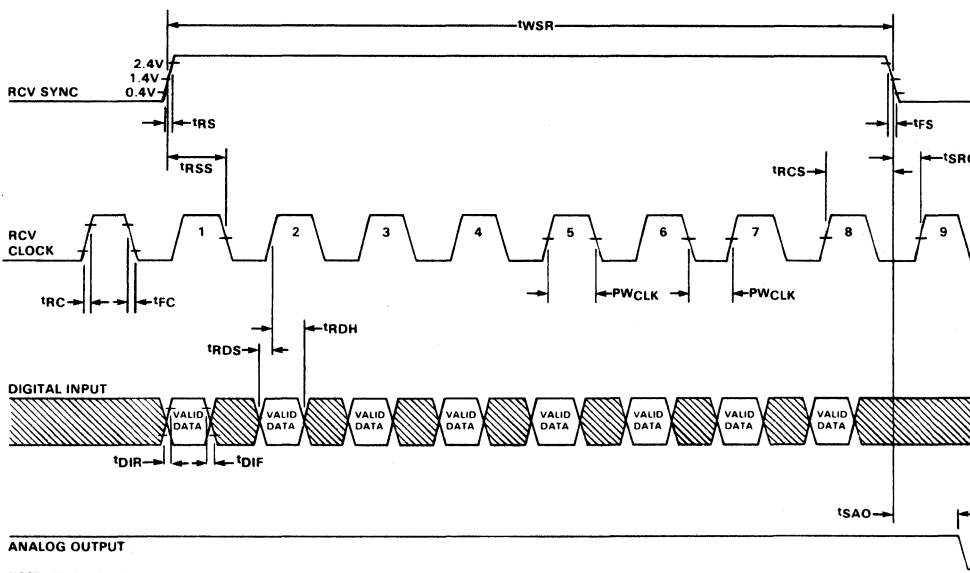


TRANSMITTER SECTION TIMING
Figure 12



NOTE: All rise and fall times are measured from 0.4V and 2.4V.
All delay times are measured from 1.4V.

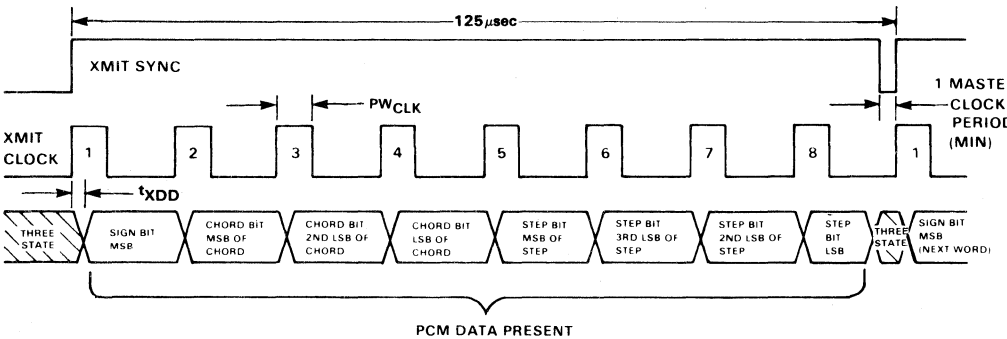
RECEIVER SECTION TIMING
Figure 13



NOTE: All rise & fall times are measured from 0.4V and 2.4V. All delay times are measured from 1.4V.

64kHz OPERATION, TRANSMITTER SECTION TIMING

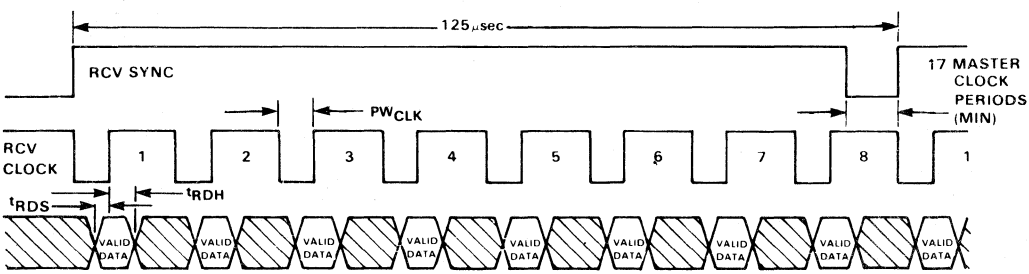
Figure 14



NOTE: All rise and fall times are measured from 0.4V and 2.4V. All delay times are measured from 1.4V.

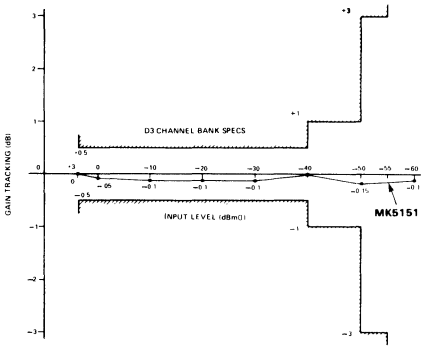
64kHz OPERATION, RECEIVER SECTION TIMING

Figure 15

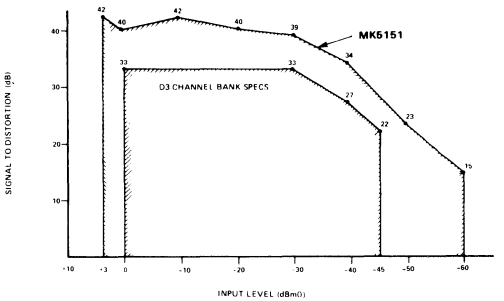


NOTE: All rise and fall times are measured from 0.4V and 2.4V. All delay times are measured from 1.4V.

MK5151 GAIN TRACKING PERFORMANCE
Figure 16

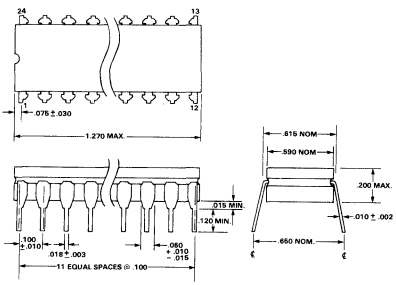


MK5151 S/D RATIO VS. INPUT LEVEL
Figure 17

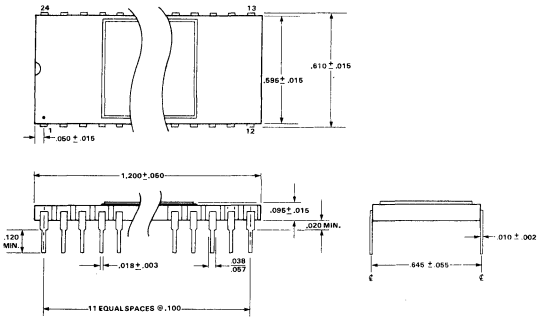


PACKAGE DESCRIPTIONS

Cerdip (J)
24-Pin
MK5151J



Side-Braze Ceramic (P)
24-Pin
MK5151P



THOMSON COMPONENTS MOSTEK

MK5156(J,N)

A LAW COMPANDING CODEC

COMMUNICATIONS PRODUCTS

FEATURES

- ☐ ±5-Volt power supplies
- ☐ Low power dissipation - 30 mW (Typ)
- ☐ Follows the A-Law companding code
- ☐ Includes CCITT recommended even-order-bit inversion
- ☐ Synchronous or asynchronous operation
- ☐ On-Chip sample and hold
- ☐ On-chip offset null circuit eliminates long-term drift errors and need for trimming
- ☐ Minimal external circuitry required
- ☐ Serial data output of 64 kb/s through 2.1 Mb/s at 8 kHz sampling rate
- ☐ Separate analog and digital grounds reduce noise problems

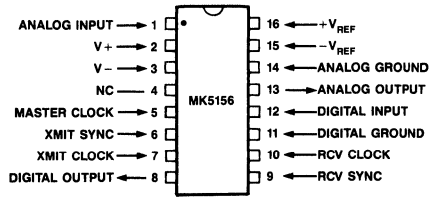


Figure 1. Pin Connections

DESCRIPTION

The MK5156 is a monolithic CMOS companding CODEC that contains two sections: (1) An analog-to-digital converter with a transfer characteristic conforming to the A-law companding code and (2) a digital-to-analog converter that also conforms to the A-law code.

These two sections form a coder-decoder designed to meet the needs of the telcommunications industry for per-channel voice-frequency CODECs used in digital switching and transmission systems. Digital input and output are in serial format. Actual transmission and reception of 8-bit data words containing the analog information is done at a 64 kb/s through 2.1 Mb/s rate with analog signal sampling occuring at an 8 kHz rate. A sync pulse input is provided for synchronizing transmission and reception of multi-channel information being multiplexed over a single transmission line. A block diagram of a PCM system using the MK5156 is shown in Figure 2.

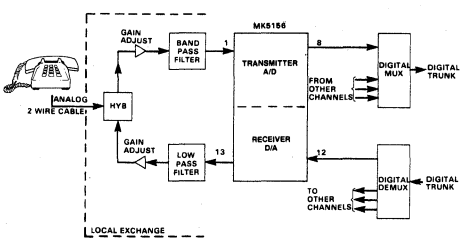


Figure 2. PCM System Block Diagram

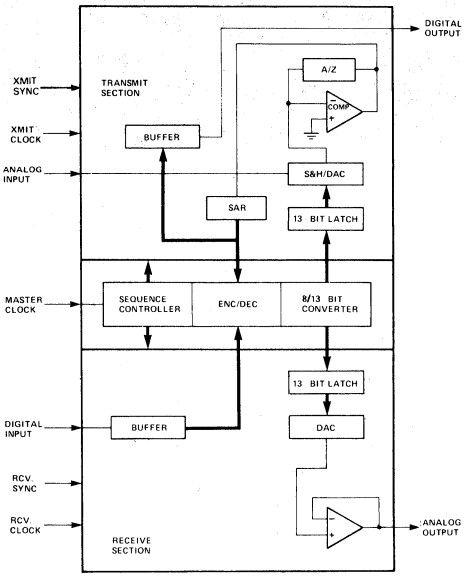


Figure 3. MK5156 Block Diagram

FUNCTIONAL DESCRIPTION

$+V_{REF}$ AND $-V_{REF}$

Input. Pins 16 and 15. These positive and negative reference voltages provide the conversion references for the digital-to-analog converters in the MK5156. $+V_{REF}$ and $-V_{REF}$ must maintain 100 ppM/°C regulation over the operating temperature range. Variation of the reference directly affects system gain.

ANALOG INPUT

Input. Pin 1. Voice-frequency analog signals that are bandwidth-limited to 4 kHz are input at this pin. Typically, they are then sampled at an 8 kHz rate. (See Figure 4.) The analog input must remain between $+V_{REF}$ and $-V_{REF}$ for accurate conversion. The recommended input interface circuit is shown in Figure 9.

MASTER CLOCK

Input. Pin 5. This signal provides the basic timing and control signals required for all internal conversions. It does not have to be synchronized with RCV SYNC, RCV CLOCK, XMIT SYNC or XMIT CLOCK and is not internally related to them.

XMIT SYNC

Input. Pin 6. This input is synchronized with XMIT CLOCK. When XMIT SYNC goes high, the digital output is activated and the A/D conversion begins on the next positive edge of MASTER CLOCK. The conversion by MASTER CLOCK can be asynchronous with XMIT CLOCK. The serial output data is clocked out by the positive edges of XMIT CLOCK. The negative edge of XMIT SYNC causes the digital output to become three-state. XMIT SYNC must go low for at least one master clock period prior to the transmission of the next digital word. (See Figure 12.)

XMIT CLOCK

Input. Pin 7. The on-chip 8-bit output shift register of the MK5156 is unloaded at the clock rate present on this pin. Clock rates of 64 kHz-2.1 MHz can be used for XMIT CLOCK. The positive edge of the INTERNAL CLOCK transfers the data from the master to the slave of a master-slave flip-flop. (See Figure 5.) If the positive edge of XMIT SYNC occurs after the positive edge of XMIT CLOCK, XMIT SYNC will determine when the first positive edge of internal clock will occur. In this event, the hold time for the first clock pulse is measured from the positive edge of XMIT SYNC.

RCV SYNC

Input. Pin 9. This input is synchronized with RCV CLOCK and serial data is clocked in by RCV CLOCK. Duration of the RCV SYNC pulse is approximately 8 RCV CLOCK periods. The conversion from digital-to-analog starts after the negative edge of the RCV SYNC pulse. (See Figure 4.) The negative edge of RCV SYNC should occur before the 9th positive clock edge to insure that only eight bits are clocked in. RCV SYNC must stay low for 17 MASTER CLOCKS (min.) before the next digital word is to be received (See Figure 13).

RCV CLOCK

Input. Pin 10. The on-chip 8-bit shift register for the MK5156 is loaded at the clock rate present on this pin. Clock rates of 64 kHz-2.1 MHz can be used for RCV CLOCK. Valid data should be applied to the digital input before the positive edge of the internal clock. (See Figure 5.) This set up time, t_{RDS}, allows the data to be transferred into the master of a master-slave flip-flop. The positive edge of the internal clock transfers the data to the slave of the master-slave flip-flop. A hold time, t_{RDH}, is required to complete this transfer. If the rising edge of RCV SYNC occurs after the first rising edge of

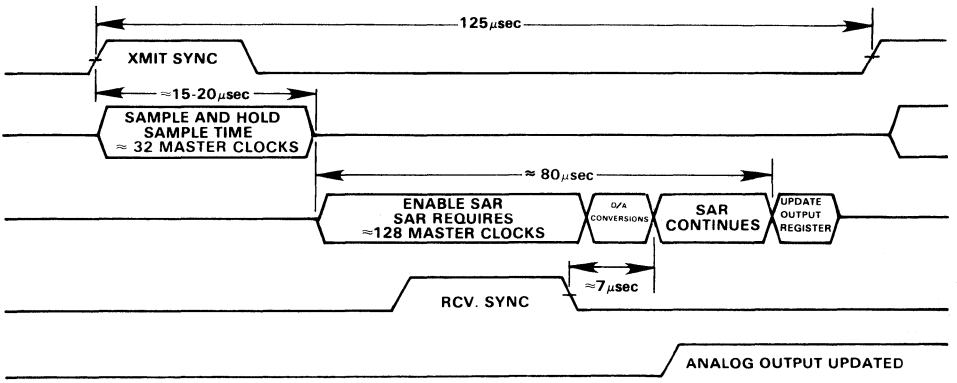


Figure 4. A/D, D/A Conversion Timing

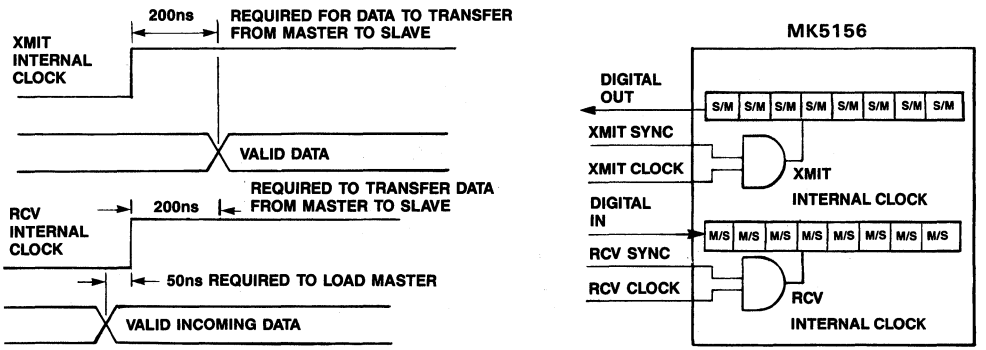


Figure 5. Data Input/Output Timing

RCV CLOCK, RCV SYNC will determine when the first positive edge of internal clock will occur. In this event, the set-up and hold times for the first clock pulse should be measured from the positive edge of RCV SYNC.

DIGITAL OUTPUT

Output. Pin 8. The MK5156 output register stores the 8-bit encoded sample of the analog input. This 8-bit word is shifted out under control of XMIT SYNC and XMIT CLOCK. When XMIT SYNC is low, the DIGITAL OUTPUT is an open circuit. When XMIT SYNC is high, the state of the DIGITAL OUTPUT is determined by the value of the output bit in the serial shift register. The output is composed of a Sign Bit, 3 Chord Bits, and 4 Step Bits. The Sign Bit indicates the polarity of the analog input while the Chord and Step Bits indicate the magnitude. In the first two Chords, the Step Bit has a value of 1.2 mV. In the third Chord, the Step Bit has a value of 2.4 mV. This doubling of the step value continues for each of the five successive Chords.

Each Chord has a specific value and the Step Bits, 16 in each Chord, specify the displacement from that value (Refer to Table 1). Thus the output, which follows the A-law, has resolution that is proportional to the input level rather than to full scale. This provides the resolution of a 12-bit A/D converter at low input levels and that of a 6-bit converter as the input approaches full scale. The transfer characteristic of the A/D converter (A-law Encoder) is shown in Figure 6.

DIGITAL INPUT

Input. Pin 12. The MK5156 input register accepts the

8-bit sample of an analog value and loads it under control of RCV SYNC and RVC CLOCK. The timing diagram is shown in Figure 11. When RCV SYNC goes high, the MK5156 uses RCV CLOCK to clock the serial data into its input register. RCV SYNC goes low to indicate the end of serial input data. The eight bits of the input data have the same functions described for the DIGITAL OUTPUT. The transfer characteristic of the D/A converter (A-law Decoder) is shown in Figure 7.

Table 1. Digital Output Code: A Law

	Chord Code	Chord Value	Step Value
1.	101	0.0mV	1.221mV
2.	100	20.1mV	1.221mV
3.	111	40.3mV	2.44mV
4.	110	80.6mV	4.88mV
5.	001	161.1mV	9.77mV
6.	000	332mV	19.53mV
7.	011	645mV	39.1mV
8.	010	1.289V	78.1mV

EXAMPLE:

1 110 0111 = +80.6mV+(2 x 4.88mV)

Sign Bit Chord Step Bits

If the sign bit were a zero, then both plus signs would be changed to minus signs.

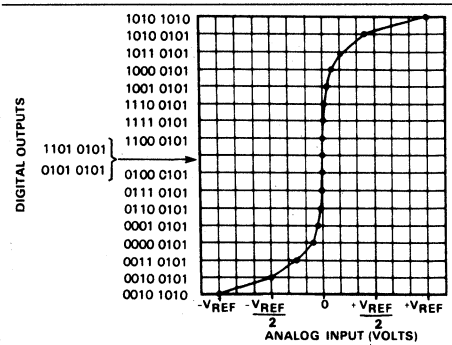


Figure 6. A/D Converter (A-Law Encoder) Transfer Characteristic

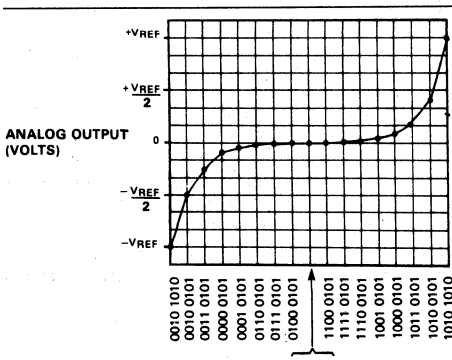


Figure 7. D/A Converter (A-Law Decoder) Transfer Characteristic

ANALOG OUTPUT

Output. Pin 13. The analog output is in the form of voltage steps (100% duty cycle) having amplitude equal to the analog sample which was encoded. This waveform is then filtered with an external low-pass filter with sinx/x correction to recreate the sampled voice signal.

OPERATION OF CODEC WITH 64kHz XMIT/RCV. CLOCK FREQUENCIES

XMIT/RCV SYNC must not be allowed to remain at a logic "1" state. XMIT SYNC is required to be at a logic "0" state for one master clock period (min.) before the next digital word is transmitted. RCV SYNC is required to be at a logic "0" state for 17 master clock periods (min.) before the next digital word is received (See Figures 12 and 13).

OFFSET NULL

The offset null feature of the MK5156 eliminates long-term drift errors and conversion errors due to temperature changes by going through an offset adjustment cycle before every conversion, thus guaranteeing accurate A/D conversion for inputs near ground. There is no offset adjust of the output amplifier because, since the output is intended to be AC-coupled to the external filter, the resultant DC error ($V_{OFFSET\ O}$) will have no effect. The sign bit is not used to null the analog input. Therefore, for an analog input of 0 volts, the sign bit will be stable.

PERFORMANCE EVALUATION

The equipment connections shown in Figure 8 can be used to evaluate the performance of the MK5156. An analog signal provided by the HP3552A Transmission Test Set is connected to the Analog Input (Pin 1) of the MK5156. The Digital Output of the CODEC is tied back to the Digital Input and the Analog Output is fed through a low-pass filter to the HP3552A. Remaining pins of the MK5156 are connected as follows:

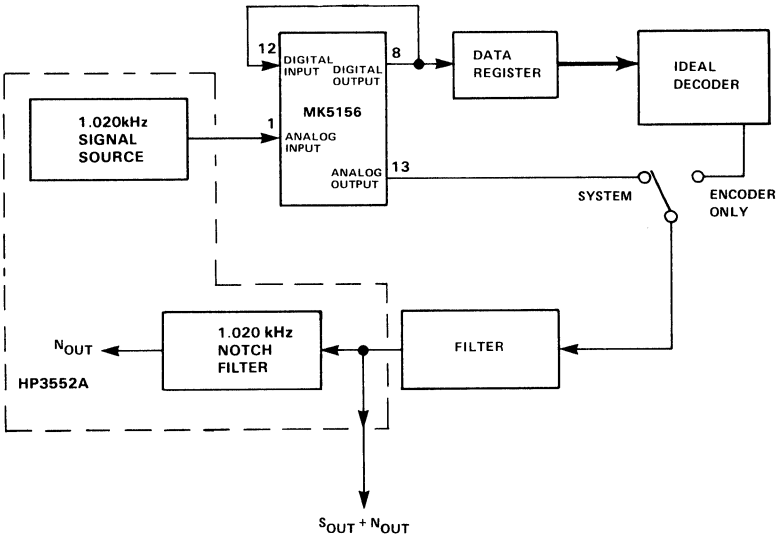
(1) RCV SYNC is tied to XMIT SYNC
(2) XMIT CLOCK is tied to MASTER CLOCK. The signal is inverted and tied to RCV CLOCK.

The following timing signals are required:

(1) MASTER CLOCK = 1.536 MHz
(2) XMIT SYNC repetition rate = 8 kHz
(3) XMIT SYNC width = 8 XMIT CLOCK periods

When all the above requirements are met, the setup of Figure 8 permits the measurement of synchronous system performance over a wide range of analog inputs.

The data register and ideal decoder provide a means of checking the encoder portion of the MK5156 independently of the decoder section. To test the system in the asynchronous mode, MASTER CLOCK should be separated from XMIT CLOCK and MASTER CLOCK should be separated from RCV CLOCK. XMIT CLOCK and RCV CLOCK are separated also.



NOTE: The ideal decoder consists of a digital decompander and a 13-bit precision DAC.

Figure 8. System Characteristics Test Configuration

ABSOLUTE MAXIMUM RATINGS*

DC Supply Voltage, V+ ..... +6V
DC Supply Voltage, V− ..... −6V
Ambient Operating Temperature, T_A ..... 0°C to 70°C
Storage Temperature ..... −55°C to +125°C
Package Dissipation at 25°C (Derated 9mW/°C when soldered into PCB) 500mW
Digital Input ..... $-0.5V \le V_{IN} \le V+$
Analog Input ..... $V- \le V_{IN} \le V+$
$+V_{REF}$ ..... $-0.5V \le +V_{REF} \le V+$
$-V_{REF}$ ..... $V- \le -V_{REF} \le +0.5V$

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL OPERATING CHARACTERISTICS

POWER SUPPLY

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V+	Positive Supply Voltage	4.75	5.0	5.25	V	
V−	Negative Supply Voltage	−5.25	−5.0	−4.75	V	
$+V_{REF}$	Positive Reference Voltage	2.375	2.5	2.625	V	1
$-V_{REF}$	Negative Reference Voltage	−2.625	−2.5	−2.375	V	1

TEST CONDITIONS: V+ = 5.0V, V− = −5.0V, + V_{REF} = 2.5V, $-V_{REF}$ = −2.5V, T_A = 0°C to 70°C

DC CHARACTERISTICS

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
R_{INAS}	Analog Input Resistance During Sampling		2		kΩ	2
R_{INANS}	Analog Input Resistance Non-Sampling		100		MΩ	
C_{INA}	Analog Input Capacitance		150	250	pF	2
$V_{OFFSETT/I}$	Analog Input Offset Voltage		±1	±8	mV	2
R_{OUTA}	Analog Output Resistance		1	50	Ω	
I_{OUTA}	Analog Output Current	0.25	0.5		mA	
$V_{OFFSET/O}$	Analog Output Offset Voltage		±50	±850	mV	
I_{INLOW}	Logic Input Low Current (V_{IN} = 0.8V) Digital Input, Clock Input, Sync Input		±0.1	±10	μA	3
I_{INHIGH}	Logic Input High Current (V_{IN} = 2.4V) Digital Input, Clock Input, Sync Input		−0.25	−0.8	mA	3
C_{DO}	Digital Output Capacitance		8	12	pF	
I_{DOL}	Digital Output Leakage Current		±0.1	±10	μA	
V_{OUTLOW}	Digital Output Low Voltage			0.4	V	4
$V_{OUTHIGH}$	Digital Output High Voltage	3.9			V	4
I+	Positive Supply Current		4	10	mA	5
I−	Negative Supply Current		2	6	mA	5
I_{REF+}	Positive Reference Current		4	20	μA	
I_{REF-}	Negative Reference Current		4	20	μA	

AC CHARACTERISTICS

SYM	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
GT_X	Gain Tracking Transmit CCITT G712 Method 2	−.2 −.4 −1.25	0.0 ±0.1 ±0.2	+.2 +.4 +1.25	dB dB dB	Analog Input = +3 to −40 dBm0 Analog Input = −40 to −50 dBm0 Analog Input = −50 to −55 dBm0 Relative to −10 dBm0
GT_R	Gain Tracking Receive CCITT G712 Method 2	−.2 −.4 −1.25	0.0 ±0.1 ±0.2	+.2 +.4 +1.25	dB dB dB	Input Level = +3 to −40 dBm0 Input Level = −40 to −50 dBm0 Input Level = −50 to −55 dBm0 Relative to −10 dBm0
GT_{EE}	Gain Tracking End to End CCITT G712 Method 2	−0.4 −0.8 −2.5	±0.1 ±0.1 ±0.2	±0.4 +0.8 +2.5	dB dB dB	Analog Input = +3 to −40dBm0 Analog Input = −40 to −50dBm0 Analog Input = −50 to −55dBm0 Relative to −10dBm0
$SD1_X$	Signal to Distortion Transmit CCITT G712 Method 1	30 36 34 30 15			dB dB dB dB dB	Analog Input = −3 dBm0 Analog Input = −6 to −27 dBm0 Analog Input = −34 dBm0 Analog Input = −40 dBm0 Analog Input = −55 dBm0 Narrow Band Noise Input
$SD1_R$	Signal to Distortion Receive CCITT G712 Method 1	30 37 35 31 16			dB dB dB dB dB	Input Level = −3 dBm0 Input Level = −6 to −27 dBm0 Input Level = −34 dBm0 Input Level = −40 dBm0 Input Level = −55 dBm0 Narrow Band Noise Input
$SD2_X$	Signal to Distortion Transmit CCITT G712 Method 2	37 31 25			dB dB dB	Analog Input = 0 to −30 dBm0 Analog Input = −40 dBm0 Analog Input = −45 dBm0
$SD2_R$	Signal to Distortion Receive CCITT G712 Method 2	37 31 25			dB dB dB	Input Level = 0 to −30 dBm0 Input Level = −40 dBm0 Input Level = −45 dBm0
SD_{EE}	Signal to Distortion End to End CCITT G712 Method 2	35 29 24	39 34 29		db db dB	Analog Input = 0 to −30dBm0 Analog Input = −40dBm0 Analog Input = −45dm0
N_X	Idle Channel Noise Transmit			−68	dBm0p	Analog Input = 0 Volts
N_R	Idle Channel Noise Receive			−90	dBm0p	Digital Input = +0 Code
N_{EE}	Idle Channel Noise End to End		−80	−68	dBm0p	Analog Input = 0 Volts
CT_{RX}	Crosstalk Receive to Transmit			−80	dB	Analog In = −50 dBm0 at 2600 Hz Digital Input = 0 dBm0 at 1008 Hz digital
CT_{XR}	Crosstalk Transmit to Receive			−80	dB	Analog In = 0 dBm0 at 1008 Hz Digital Input = +0 Code
TLP	Transmission Level Point		+4		dB	600Ω

NOTES:

1. $-V_{REF}$ and $-V_{REF}$ must be matched within ±1% in order to meet system requirements.
2. Sampling is accomplished by charging an internal capacitor; therefore, the designer should avoid excessive source impedance. Input related device characteristics are derived using the Recommended Analog Input Circuit. See Figure 9.
3. When a transition from a "1" to a "0" takes place, the user must sink the "1" current until reading the "0" level.
4. Driving 30pF with $I_{OH} = -100\ \mu A$, I_{OL} $-500\ \mu A$.
5. Results in 30 mW typical power dissipation (clocks applied) under normal operating conditions.
6. This delay is neccessary to avoid overlapping Clock and Sync.
7. This first bit of data is loaded when Sync and Clock are both "1" during bit time 1 as shown on RCV timing diagram.

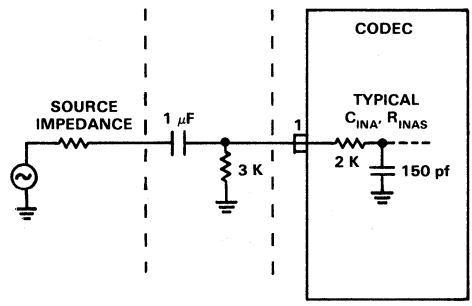
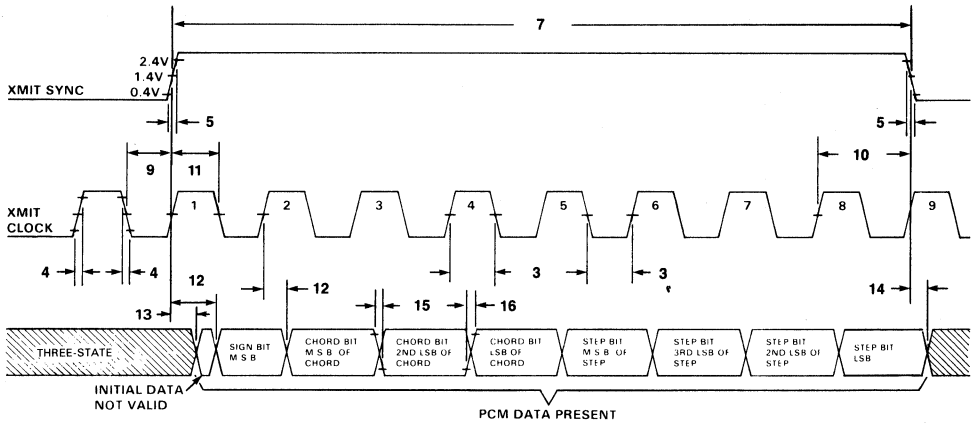


Figure 9. Recommended Analog Input Circuit

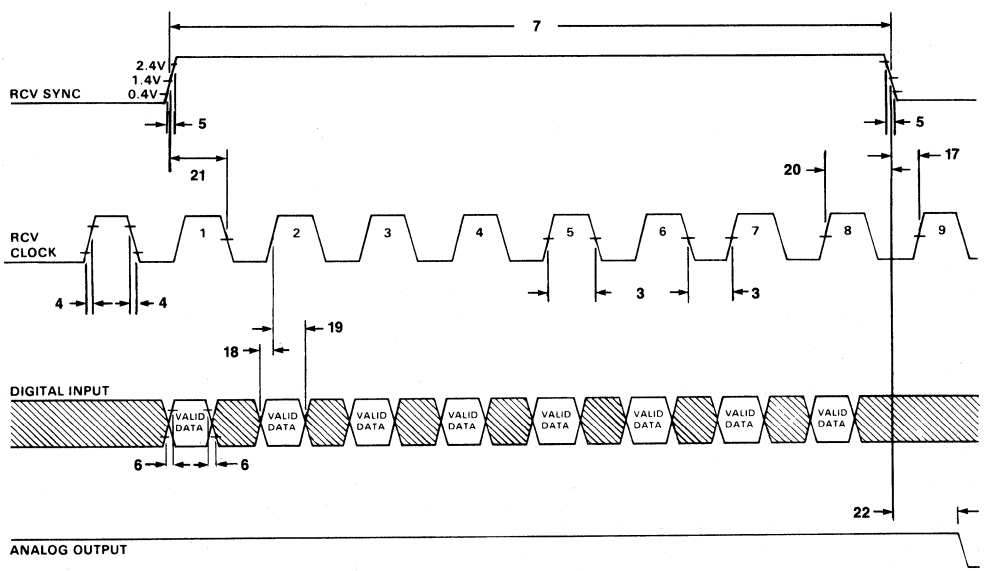
TIMING SPECIFICATIONS (Refer to Figures 10 and 11)

#	SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
1	F_M	Master Clock Frequency	1.5	2.048	2.1	MHz	
2	F_R, F_X	XMIT, RCV. Clock Frequency	0.064	2.048	2.1	MHz	
3	PW_{CLK}	Clock Pulse Width (MASTER, XMIT, RCV)	200			ns	
4	t_{RC} t_{FC}	Clock Rise, Fall Time (MASTER, XMIT, RCV)			25% of PW_{CLK}	ns	
5	t_{RS}, t_{FS}	Sync Rise, Fall Time (XMIT, RCV)			25% of PW_{CLK}	ns	
6	t_{DIR}, t_{DIF}	Data Input Rise, Fall Time			25% of PW_{CLK}	ns	
7	t_{WSX}, t_{WSR}	Sync Pulse Width (XMIT, RCV)		$\frac{8}{F_X(F_R)}$		μs	
8	t_{PS}	Sync Pulse Period (XMIT, RCV)		125		μs	
9	t_{XCS}	XMIT Clock-to-XMIT Sync Delay	50% of $t_{FC}(t_{RS})$			ns	6
10	t_{XCSN}	XMIT Clock-to-XMIT Sync (Negative Edge) Delay	200			ns	
11	t_{XSS}	XMIT Sync Set-Up Time	200			ns	
12	t_{XDD}	XMIT Data Delay	0		200	ns	4
13	t_{XDP}	XMIT Data Present	0		200	ns	4
14	t_{XDT}	XMIT Data Three State			150	ns	4
15	t_{DOF}	Digital Output Fall Time		50	100	ns	4
16	t_{DOR}	Digital Output Rise Time		50	100	ns	4
17	t_{SRC}	RCV Sync-to-RCV Clock Delay	50% of t_{RC} (t_{FS})			ns	6
18	t_{RDS}	RCV Data Set-Up Time	50			ns	7
19	t_{RDH}	RCV Data Hold Time	200			ns	7
20	t_{RCS}	RCV Clock-to-RCV Sync Delay	200			ns	
21	t_{RSS}	RCV Sync Set-Up Time	200			ns	7
22	t_{SAO}	RCV Sync-to-Analog Output Delay		7		μs	
23	SLEW+	Analog Output Positive Slew Rate		1		V/μs	
24	SLEW−	Analog Output Negative Slew Rate		1		V/μs	
25	DROOP	Analog Output Droop Rate		25		μV/μs	



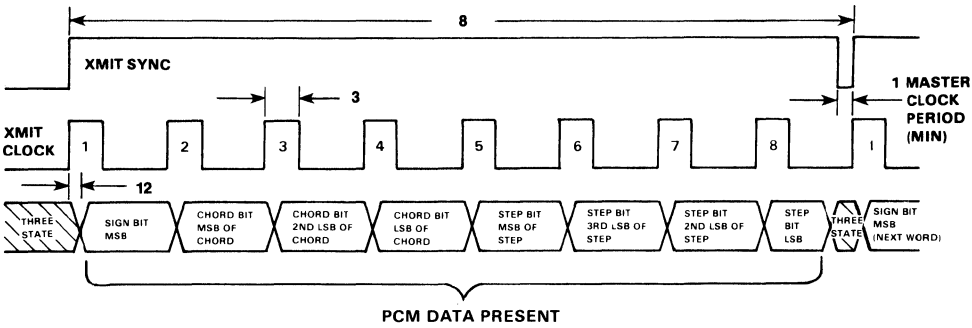
NOTE: All rise and fall times are measured from 0.4V and 2.4V. All delay times are measured from 1.4V.

Figure 10. Transmitter Section Timing



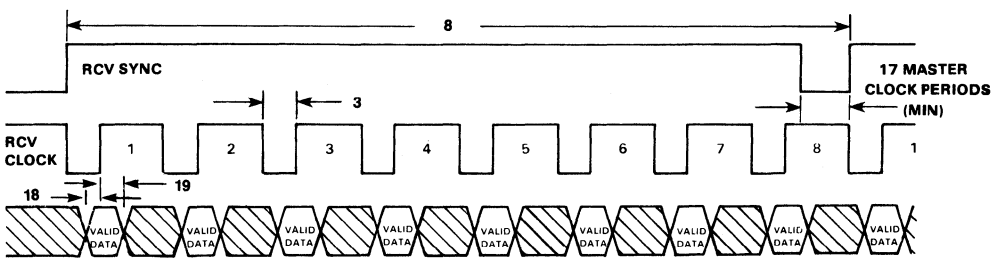
NOTE: All rise and fall times are measured from 0.4V and 2.4V. All delay times are measured from 1.4V.

Figure 11. Receiver Section Timing



NOTE: All rise and fall times are measured from 0.4V and 2.4V. All delay times are measured from 1.4V.

Figure 12. 64kHz Operation, Transmitter Section Timing



NOTE: All rise and fall times are measured from 0.4V and 2.4V. All delay times are measured from 1.4V.

Figure 13. 64kHz Operation, Receiver Section Timing

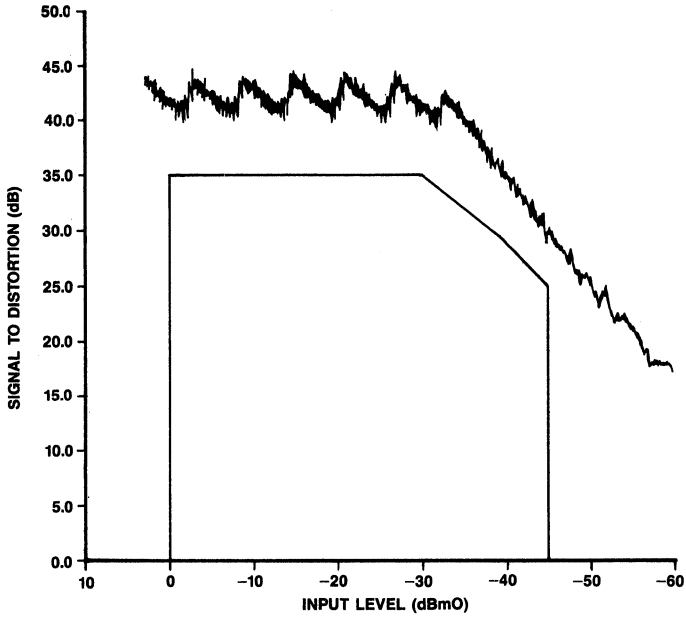


Figure 14. MK5156 Single-Ended Signal To Distortion

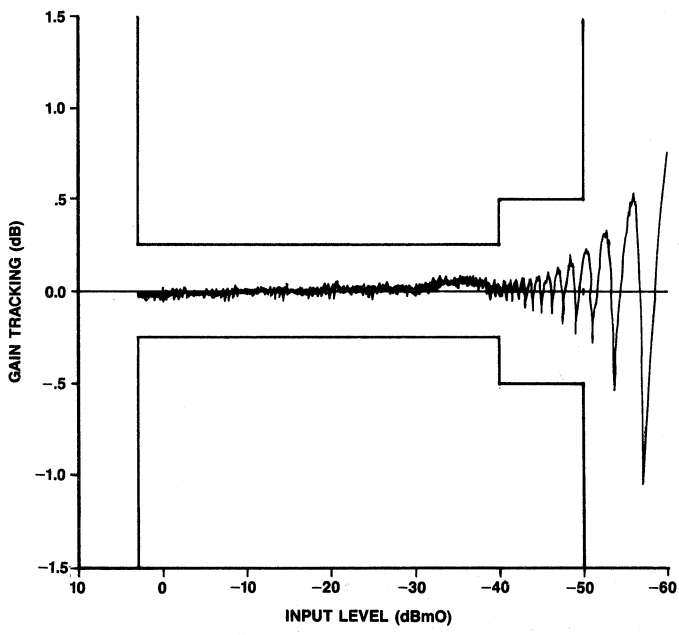
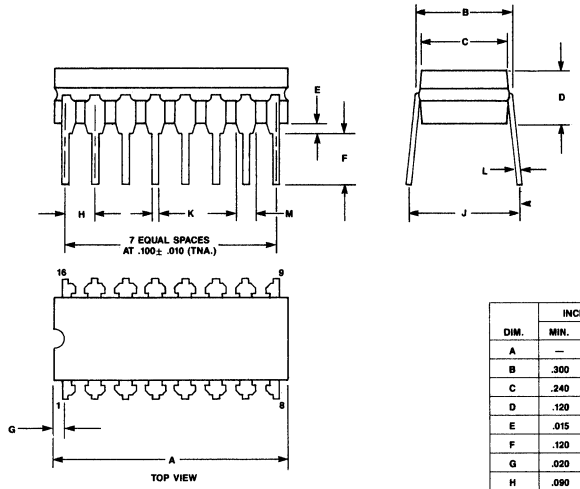


Figure 15. MK5156 Single-Ended Gain Tracking

PACKAGE DESCRIPTION
Cerdip Hermetic (J)
16-Pin MK5156

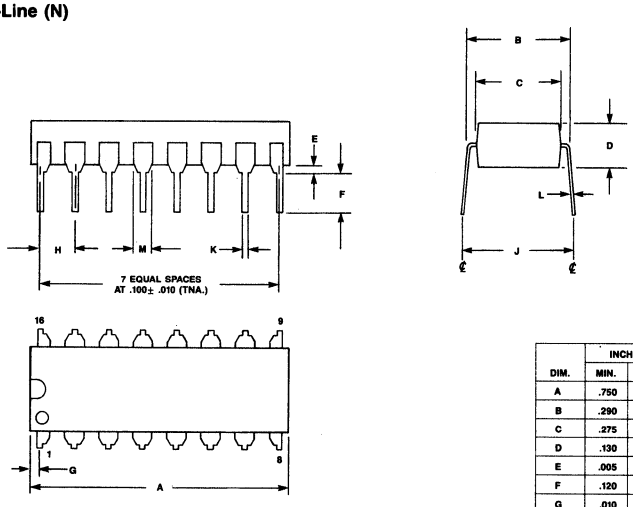


TOP VIEW

DIM.	INCHES MIN.	INCHES MAX.	NOTES
A	—	.760	2
B	.300	.325	
C	.240	.260	2
D	.120	.140	
E	.015	—	3
F	.120	.150	
G	.020	.040	
H	.090	.110	
J	.300	.400	4
K	.015	.021	5
L	.008	.012	5
M	.050	.070	6

NOTES:
1. Lead finish to be specified on the detail specifications.
2. This dimension includes base-to-cap misalignment and glass runout, except along the bottom surface of the leads.
3. Package standoff to be measured per JEDEC requirements.
4. Measured from centerline to centerline at lead tips.
5. This dimension excludes leads 1, 8, 9 and 16.

PACKAGE DESCRIPTION
Plastic Dual-In-Line (N)
16-Pin MK5156



TOP VIEW

DIM.	INCHES MIN.	INCHES MAX.	NOTES
A	.750	.780	
B	.290	.320	
C	.275	.310	2
D	.130	.200	
E	.005	.040	3
F	.120	.170	
G	.010	.060	
H	.090	.110	
J	.300	.400	4
K	.015	.021	
L	.008	.015	
M	.045	.070	5

NOTES:
1. Lead finish is to be specified on the detail specifications.
2. Overall length includes .010 in. flash on either end of the package.
3. Package standoff to be measured per JEDEC requirements.
4. Measured from centerline to centerline at lead tips.
5. When the solder lead finish is specified, the maximum limit shall be increased by .003 in.
6. This dimension excludes leads 1, 8, 9 and 16.

INTRODUCTION

A general trend towards the conversion of voice signals to digital information is currently occurring. TDM PCM is the most popular form of digital transmission.

Today there are several important applications for this TDM scheme:

1. A high speed digital data link between central offices to pass many conversations over one pair of wires.
2. The electronic connection of two different circuit paths.
3. Concentrators

Traditionally this connection had been done by electromechanical crossreed switches. Very low "on" resistance, low crosstalk, and immunity from the large ringing or transient voltages were required. Since the electromechanical technique was deemed to be of lower reliability, an all electronic approach was desired. Electronic cross point switches were designed and built, but because the electrical requirements mentioned above are extremely difficult to meet, the results were not entirely satisfying.

The digital approach obviates the analog switch problem by first performing an A to D conversion, then assigning a time slot for each voice channel. For the D3 channel bank, 24 channels of digital data of 8 bits per word are transmitted in a serial bit stream at 1.544 Mbits/sec. Each voice channel is sampled at an 8kHz rate so this signal must be bandlimited to less than 4kHz in order to prevent undesirable aliasing.

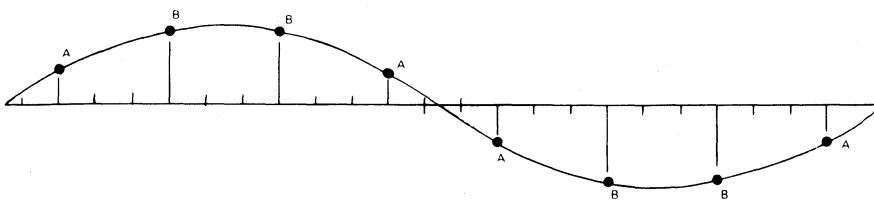
Figure 1 shows how a 1kHz input signal is sampled every 125 μsec. At each of these sampling times, the analog information is converted into an eight-bit digital word that is later sent out in serial format at the 1.544 Mbits/sec rate.

Figure 2 shows how the 24 voice channels are time division multiplexed onto one wire (for simplicity only simplex operation is shown).

Channel 1 analog information is first bandlimited to less than 4kHz, then sampled and converted to a companded digital code. This 8 bit word is serially transmitted to a multiplexer where digital information from all the other channels are assimalated. The final bit stream of 1.544mbit/sec is sent to the demultiplexer where the appropriate alphanumeric channel is connected to numeric channel. This control (selection) is done by the main computer or processor. One may see that any numeric channel could be connected to any alphanumeric channel by means of a different time slot assignment. This completes the switching in a completely digital manner.

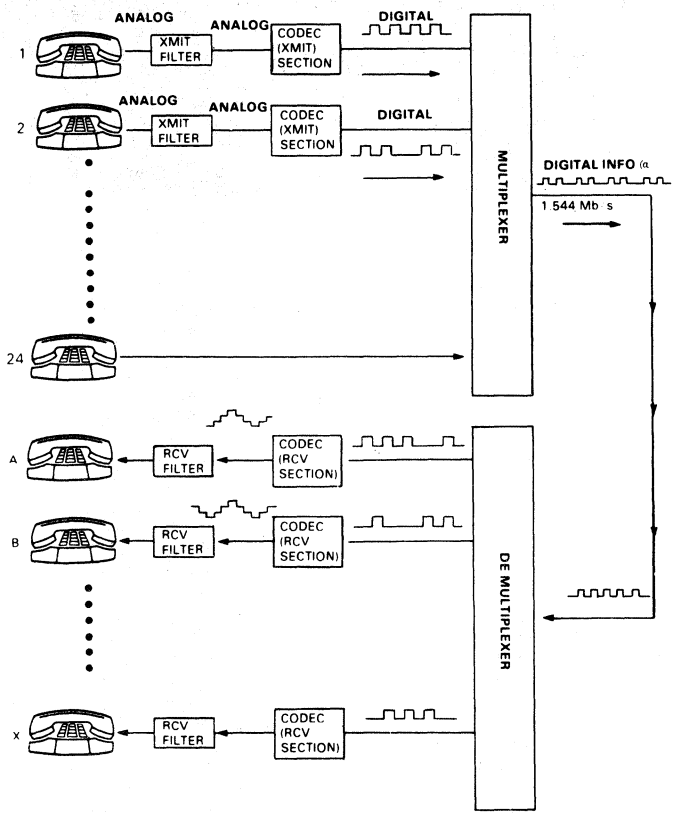
8kHz SAMPLING SYSTEM

Figure 1



24 CHANNEL MULTIPLEXING

Figure 2



For T1 carrier systems, the digital PCM information might be transmitted between central offices. For PBX applications, the PCM technique is used to allow the switching to be done digitally. The accuracy of the subsequent D-A conversion preserves the voice quality so that insertion loss is not a problem.

We selected the metal gate CMOS process for several reasons. First it is extremely low power, which is of great concern. Secondly, it allows for high-quality, matched capacitors in a minimum of chip size. Critical analog circuit design is done well in CMOS: for example, high gain amplifiers and comparators. Also, the metal gate CMOS process is one that is well proven in high volume production.

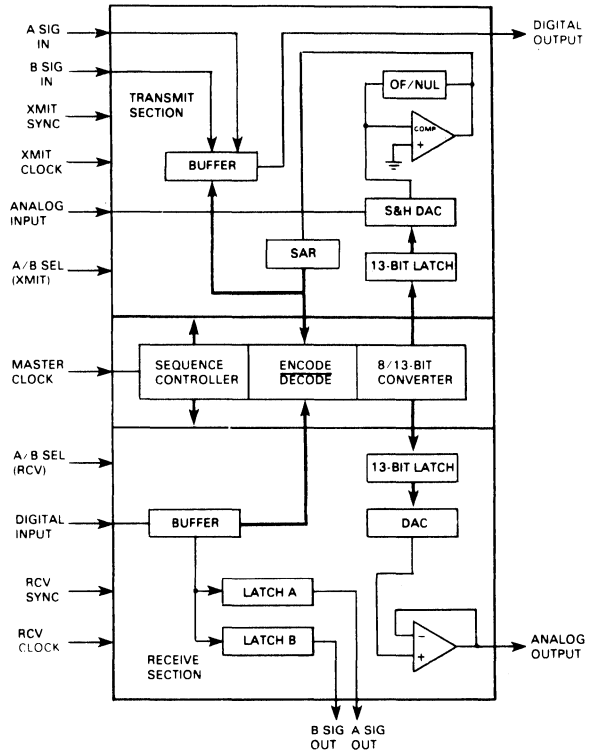
By using the CMOS process, only two supplies are necessary, plus and minus five volts. To minimize power, all the digital logic is run from the plus 5V supply to ground, and only the analog section operates from ± 5 volts.

CHIP ARCHITECTURE

Figure 3 shows the block diagram representation of the CODEC chip. The important features of the scheme used are listed below:

1. Two independent DAC's for encode and decode functions provide system isolation not achievable using shared DAC approach. The capacitive two DAC approach also eliminates external sample/hold capacitors as well as an external filter for offset which is required in the shared DAC approach. This minimizes the external components required.
2. Complete signalling compatibility with D3 channel bank requirements.
3. Since the companding law is implemented using 8 to 13 bit converter, the DAC is a linear DAC thus minimizing the number of analog components to only the minimum required for system implementation, namely two: one comparator and only one op-amp on the entire chip. Minimizing the linear

CODEC BLOCK DIAGRAM
Figure 3



components helps reduce system operating power which was the overriding consideration in chip design. Using the CMOS process, the digital portions dissipate power only during transitions. The linear sections consume power continuously.

4. The digital companding section allows easy conversion from mu-law to A-law. The CODEC allows data input/output rates from 64kHz to 2.1MHz.
5. Asynchronous or synchronous operation.

MODES OF OPERATION

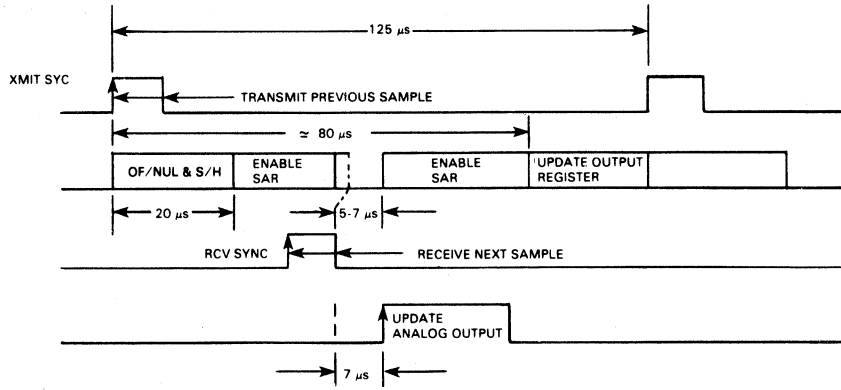
The XMIT and Receive function are completely independent of each other and of the master clock. Thus the chip can operate in synchronous/asynchronous mode at various input/output clock rates. The chip timing diagram is shown in Figure 4 and the Receive and XMIT modes of operation are described in detail below:

(a) Receive Mode of Operation
In the receive mode of operation, the serial input data is shifted into the input buffer at the receive clock rate during the period receive sync. is high. The encode process is halted after the falling edge of receive sync pulse) for about 5 to 7μs, and the translated data from 8 to 13 bit converter is latched into the 13 bit receive latch which updates the output of the receive DAC with 100% duty cycle. The receive DAC acts as a sample and hold and is buffered by the unity gain op amp to the output. During the signalling frame a 7 bit decode is performed and the 8th data bit is latched into the SigA/SigB output latch as selected by the A/B Select (RCV) input. When the eight bit of a word is a signalling bit, it is assigned the value of ½ step. This results in a lower S/D ratio than if it were arbitrarily set to either a one or zero.

(b) Transmit Mode of Operation:
In this mode of operation the analog signal is sampled in the input sample/hold which performs the offset-null function simultaneously as described in the circuit operation section. Following the hold mode, the encoding process is completed using successive approximation technique. The operation of the XMIT DAC is similar to the operation of the receive DAC as described earlier. After the encode

A/D AND D/A CONVERSION TIMING

Figure 4



process is completed, the output of the SAR is loaded into the output buffer. The data is transmitted serially at the output clock rate during the period the XMIT SYNC is high. During the signalling frame, signalling information (SigA/SigB) is inserted into the output bit stream in place of the 8th data bit as selected by the A/B select (SMIT) input.

CIRCUIT DESCRIPTION

The system timing is controlled by the sequence controller which operates at master clock rate of 1.5 - 2.1 MHz. All necessary signals, e.g. and S&H, SAR clock Encode/Decode control, etc; are generated in this section. To insure proper encode operation, decode interrupt is allowed only when the internal SAR clock is low thus resulting in a variable (5-7μs) decode interrupt interval.

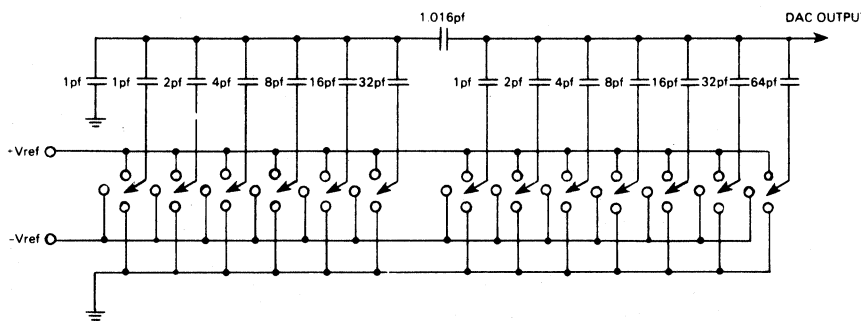
The 8 to 13 bit converter gives a one-to-one translation between 8 bit companded code at its input to a 13 bit linear code at its output thus allowing the use of a linear DAC in the digital-to-analog conversion process.

The 13-bit linear DAC operates on the charge distribution principal of a binary weighted capacitor ladder.

As shown in Figure 5, the capacitor ladder has two sections of 7 bits (7 most significant bits) and 6 bits (6 least significant bits) connected by a 64:1 capacitor divider. The equivalent circuit of the two sections can be drawn as shown in Figure 6.

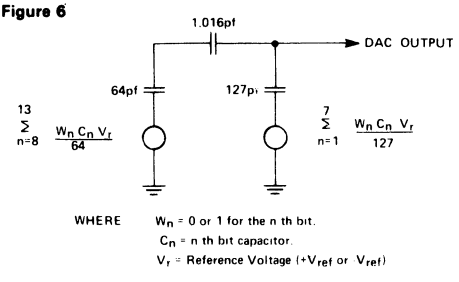
CAPACITOR LADDER

Figure 5



CAPACITOR LADDER EQUIVALENT CIRCUIT

Figure 6



The output of the DAC can be written as:

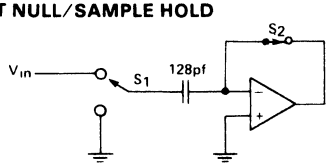
$$V_{DAC} = \frac{V_r}{128}\left[\sum_{n=1}^{7} W_n C_n + \sum_{n=8}^{13} W_n (C_n/64)\right]$$

which is equivalent to the output of a 13 bit DAC with an equivalent output capacitance of 128pF.

In the encode section this equivalent capacitor of 128pF is also employed to perform the additional function of offset-null and sample-hold as shown in Figure 7.

OFFSET NULL/SAMPLE HOLD

Figure 7



Initially S_1 is connected to V_{in} and S_2 is closed. The op. amp. is operating as a unity gain follower and its offset voltage (V_{off}), along with the analog input voltage, is stored on the capacitor.

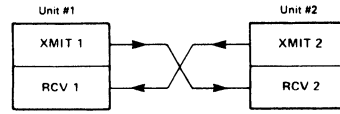
Then switch S_2 is opened and S_1 is switched to analog ground. The voltage at the inverting input of the op-amp is now V_{off}-V_{in}. Thus when the amplifier operates with S_2 open it acts as a comparator with effectively zero offset and $-V_{in}$ applied on its inverting input. The other end of the capacitor can now be operated as a DAC. Thus the capacitor ladder performs all the necessary functions of offset-null sample-hold as well as a DAC in the encode section of the chip.

EXPERIMENTAL RESULTS

The set up of Figure 8 was used to evaluate the chip performance.

CHIP PERFORMANCE

Figure 8

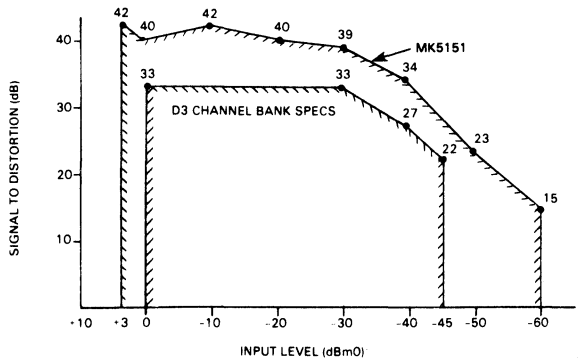


The MK5151 CODEC performance exceeds the AT&T D3 channel bank specifications. Figure 9 shows the signal-to-quantizing distortion as a function of input level.

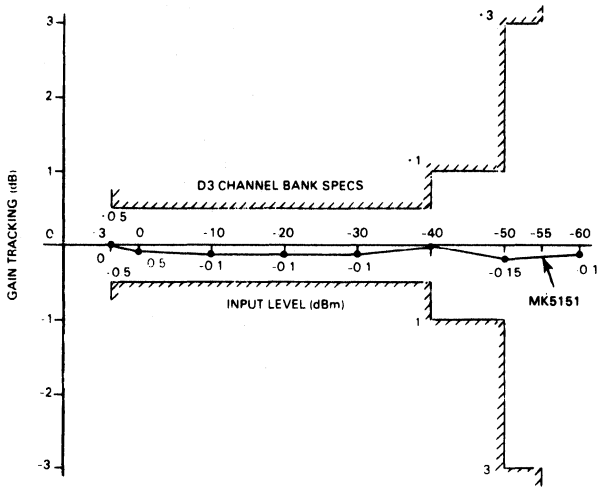
Idle channel noise of 13-14dBrnC0 is better than the D3 spec by 9-10dB. Gain tracking is shown in Figure 10.

SIGNAL-TO-NOISE RATIO

Figure 9



GAIN TRACKING
Figure 10



Operating power measured at room temperature typically is 30mW. This is low enough that a stand-by mode is not deemed necessary. The European A-law version of the CODEC is also available and is simply a metal mask variation of this product. Chip size is 170 x 184 mils.

PCM MONOLITHIC FILTER

The ETC5040/ETC5040A filter is a monolithic circuit containing both transmit and receive filters specifically designed for PCM CODEC filtering applications in 8 kHz sampled systems.

The filter is manufactured using double-poly silicon gate CMOS technology. Switched capacitor integrators are used to simulate classical LC ladder filters which exhibit low component sensitivity.

TRANSMIT FILTER STAGE

The transmit filter is fifth order elliptic low pass filter in series with a fourth order Chebychev high pass filter. It provides a flat response in the passband and rejection of signals below 200 Hz and above 3.4 kHz.

RECEIVE FILTER STAGE

The receive filter is a fifth order elliptic low pass filter designed to reconstruct the voice signal from the decoded/demultiplexed signal which, as a result of the sampling process, is a stair-step signal having the inherent sin x/x frequency response. The receive filter approximates the function required to compensate for the degraded frequency response and restore the flat pass-band response.

- Exceeds all D3/D4 and CCITT specifications
- + 5V, −5V power supplies
- Low power consumption :

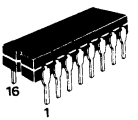
  45 mW (600 Ω-0 dBm load)

  30 mW (power amps disabled)
- Power down mode : 0.5 mW
- 20 dB gain adjust range
- No external anti-aliasing components
- Sin x/x correction in receive filter
- 50/60 Hz rejection in transmit filter
- TTL and CMOS compatible logic
- All inputs protected against static discharge due to handling

CMOS

PCM
MONOLITHIC FILTER

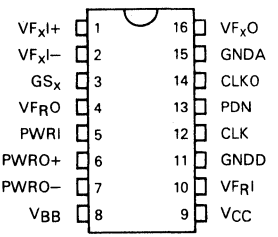
CASE



J SUFFIX

CERDIP PACKAGE

PIN ASSIGNMENT



BLOCK DIAGRAM

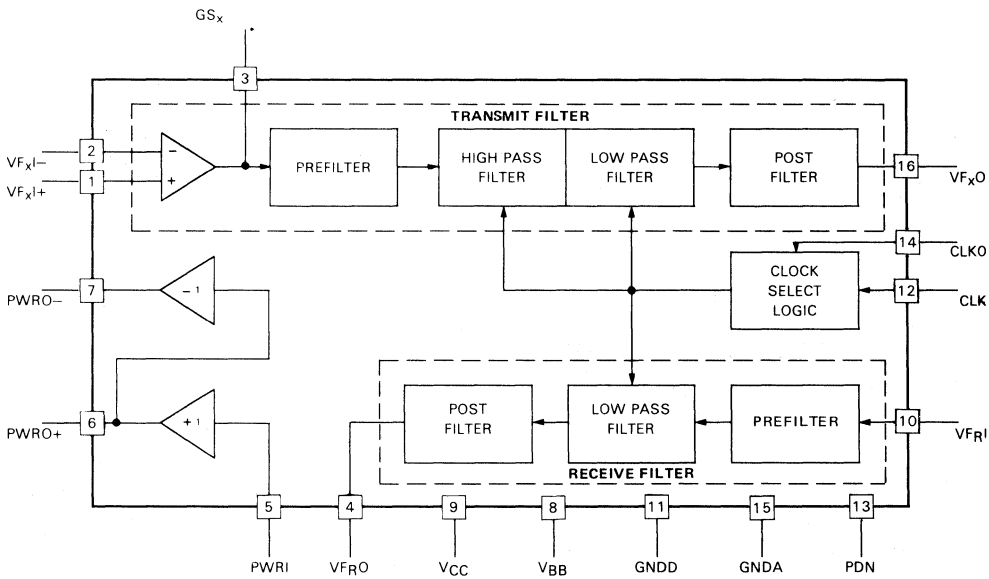


FIGURE 1

PIN DESCRIPTION

Name	Pin Type	N°	Description
VF_XI+	I	1	The non-inverting input to the transmit filter stage
VF_XI-	I	2	The inverting input to the transmit filter stage
GS_X	O	3	The output used for gain adjustments of the transmit filter
VF_RO	O	4	The low power receive filter output. This pin can directly drive the receive port of an electronic hybrid.
PWRI	I	5	The input to the receive filter differential power amplifier.
PWRO+	O	6	The non-inverting output of the receive filter power amplifier. This output can directly interface conventional transformer hybrids.
PWRO–	O	7	The inverting output of the receive filter power amplifier. This output can be used with PWRO+ to differentially drive a transformer hybrid.
V_{BB}	S	8	The negative power supply pin. Recommended input is –5 V.
V_{CC}	S	9	The positive power supply pin. The recommended input is 5 V.
VF_RI	I	10	The input pin for the receive filter stage.
GNDD	GND	11	Digital ground input pin. All digital signals are referenced to this pin.
CLK	I	12	Master input clock. Input frequency can be selected as 2.048 MHz, 1.544 MHz or 1.536 MHz.
PDN	I	13	The input pin used to power down the ETC5040/ETC5040A during idle periods. Logic 1 (V_{CC}) input voltage causes a power down condition. An internal pull-up is provided.
CLKO	I	14	This input pin selects internal counters in accordance with the CLK input clock frequency : **CLK** **Connect CLK0 to:** 2048 kHz V_{CC} 1544 kHz GNDD 1536 kHz V_{BB} An internal pull-up is provided.
GNDA	GND	15	Analog ground input pin. All analog signals are referenced to this pin. Not internally connected to GNDD.
VF_XO	O	16	The output of the transmit filter stage.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply voltage	V_{CC}	±7	V
Input voltage	V_{in}	±7	V
Operating temperature range	T_A	−25°C to +125 °C	°C
Storage temperature	T_{stg}	−65°C to + 150°C	°C
Power dissipation	P_D	1/package	W
Output short-circuit duration		continuous	
Lead temperature		300	°C

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%, V_{BB} = − 5.0V ± 5%, clock frequency is 2.048 MHz
Typical parameters are specified at T_A = + 25°C, V_{CC} = 5.0V, V_{BB} = − 5.0 V (Unless otherwise specified)
Digital interface voltages measured with respect to digital ground, GNDD. Analog voltages measured with respect to analog ground, GNDA.

POWER DISSIPATION

Characteristic	Symbol	Min	Typ	Max	Unit
V_{CC} standby current (PDN = V_{DD}, power down mode)	I_{CC0}	–	50	100	μA
V_{BB} standby current (PDN = V_{DD}, power down mode)	I_{BB0}	–	−50	−100	μA
V_{CC} operating current (PWRI = V_{BB}, power amp inactive)	I_{CC1}	–	3.0	4.0	mA
V_{BB} operating current (PWRI = V_{BB}, power amp inactive)	I_{BB1}	–	−3.0	−4.0	mA
V_{CC} operating current (Note 1)	I_{CC2}	–	4.6	6.4	mA
V_{BB} operating current (Note 1)	I_{BB2}	–	−4.6	−6.4	mA

DIGITAL INTERFACE

Characteristic	Symbol	Min	Typ	Max	Unit
Input current, CLK (0 V ≦ V_{IN} ≦ V_{CC})	I_{INC}	−10	–	10	μA
Input current, PDN (0 V ≦ V_{IN} ≦ V_{CC}−2 V)	I_{INP}	−100	–	–	μA
Input current, CLK0 (V_{BB} ≦ V_{IN} ≦ V_{CC}−2 V)	I_{INO}	−10	–	−0.1	μA
Input low voltage, CLK, PDN	V_{IL}	0	–	0.8	V
Input high voltage, CLK, PDN	V_{IH}	2.2	–	V_{CC}	V
Input low voltage, CLK0	V_{ILO}	V_{BB}	–	V_{BB}+0.5	V
Input intermediate voltage, CLK0	V_{IIO}	−0.8	–	0.8	V
Input high voltage, CLK0	V_{IHO}	V_{CC}−0.5	–	V_{CC}	V

TRANSMIT INPUT AMP. OP.

Characteristic	Symbol	Min	Typ	Max	Unit
Input leakage current, VF_xI (V_{BB} ≦ VF_xI ≦ V_{CC})	IB_xI	−100	–	100	nA
Input resistance VF_xI (V_{BB} ≦ VF_xI ≦ V_{CC})	RI_xI	10	–	–	MΩ
Input offset voltage, VF_xI (−2.5 V ≦ V_{IN} ≦ +2.5 V)	VOS_xI	−20	–	20	mV
Common-mode range, VF_xI	V_{CM}	−2.5	–	2.5	V
Common-mode rejection ratio (−2.5V ≦ V_{IN} ≦ 2.5 V)	CMRR	60	–	–	dB
Power supply rejection of V_{CC} or V_{BB}	PSRR	60	–	–	dB
Open loop output resistance GS_x	R_{OL}	–	1	–	kΩ
Minimum load resistance, GS_x	R_L	10	–	–	kΩ
Maximum load capacitance, GS_x	C_L	–	–	100	pF
Output voltage swing, GS_x (R_L ≧ 10 kΩ)	VO_xI	± 2.5	–	–	V
Open loop voltage gain, GS_x (R_l ≧ 10 kΩ)	A_{VOL}	5,000	–	–	V/V
Open loop unity gain bandwidth, GS_x	F_C	–	2	–	MHz

AC ELECTRICAL CHARACTERISTICS

T_A = + 25° C. All parameters are specified for a signal level of 0 dBm0 at 1 kHz. The 0 dBm0 level is assumed to be 1.54 Vrms measured at the output of the transmit or receive filter. (Unless otherwise specified).

TRANSMIT FILTER (Note 2)

Characteristic		Symbol	Min	Typ	Max	Unit
Minimum load resistance		RL_X				kΩ
$-2.5\ V < V_{out} < +2.5\ V$			3	–	–	
$-3.2\ V < V_{out} < +3.2\ V$			10	–	–	
Load capacitance, VF_XO		CL_X	–	–	100	pF
Output resistance, VF_XO			–	1	3	Ω
V_{CC} power supply rejection VF_XI (f=1kHz, VF_XI+ = 0 Vrms)		PSRR1	30	–	–	dB
V_{BB} power supply rejection, VF_XO. (Same as above)		PSRR2	35	–	–	dB
Absolute gain (f = 1 kHz)		GA_X				dB
	ETC5040A		2.9	3.0	3.1	
	ETC5040		2.875	3.0	3.125	
Gain relative to GA_X		GR_X				dB
Below 50 Hz			–	–	−35	
50 Hz			–	−41	−35	
60 Hz			–	−35	−30	
200 Hz	ETC5040A		−1,5	–	0	
	ETC5040		−1.5	–	0.05	
300 Hz to 3 kHz	ETC5040A		−0.125	–	0.125	
	ETC5040		−0.15	–	0.15	
3.3 kHz	ETC5040A		−0.35	–	0.03	
	ETC5040		−0.35	–	0.125	
3.4 kHz			−0.70	–	−0.1	
4.0 kHz			–	−15	−14	
4.6 kHz and above			–	–	−32	
Absolute delay at 1 kHz		DA_X	–	–	230	μs
Differential envelope delay from 1 kHz to 2.6 kHz			–	–	60	μs
Single frequency distortion products		DP_X1	–	–	−48	dB
Distortion at maximum signal level		DP_X2				dB
1.6 Vrms, 1kHz signal applied to VF_XI+, gain = 20 dB, R_L = 10 kΩ			–	–	−45	
Total C message noise at VF_XO		NC_X1	–	2	5	dBrnc0
Total C message noise at VF_XO		NC_X2				dBrnc0
Gain setting Op Amp at 20 dB, non inverting, note 3, $0°C \leq T_A \leq +70°C$			–	3	6	
Temperature coefficient of 1 kHz gain		GA_XT	–	0.0004	–	dB/°C
Supply voltage coefficient of 1 kHz gain		GA_XS	–	0.01	–	dB/V
Crosstalk, receive to transmit 20 log $\frac{VF_XO}{VFRO}$		$CTRX$				dB
Receive filter output = 2.2 Vrms,						
VF_XI+ = 0 Vrms, f= 0.2 kHz to 3.4 kHz, measure VF_XO			–	–	−70	
Gaintracking relative to GA_X		GR_XL				dB
Output level = + 3 dBm0			−0.1	–	0.1	
+ 2 dBm0 to − 40 dBm0			−0.05	–	0.05	
− 40 dBm0 to − 55 dBm0			−0.1	–	0.1	

AC ELECTRICAL CHARACTERISTICS (Continued)

T_A = + 25° C. All parameters are specified for a signal level of 0 dBm0 at 1 kHz. The 0 dBm0 level is assumed to be 1.54 Vrms measured at the output of the transmit or receive filter. (Unless otherwise specified).

RECEIVE FILTER (Unless otherwise noted, the receive filter is preceded by a sin x/x filter within an input signal level of 1.54 Vrms).

Characteristic	Symbol	Min	Typ	Max	Unit
Input leakage current, VF_RI ($-3.2\ V \leqq V_{IN} \leqq 3.2\ V$)	IB_R	−100	–	100	nA
Input resistance, VF_RI	RI_R	10	–	–	MΩ
Output resistance, VF_RO	RO_R	–	1	3	Ω
Load capacitance, VF_RO	CL_R	–	–	100	pF
Load resistance, VF_RO	RL_R	10	–	–	kΩ
Power supply rejection of V_{CC} or V_{BB} (VF_RO VF_RI connected to GNDA, f = 1 kHz)	PSRR3	35	–	–	dB
Output DC offset, VF_RO (VF_RI connected to GNDA)	VOS_RO	− 200	–	+ 200	mV
Absolute gain (f = 1 kHz)	GA_R				dB
ETC5040A		−0.1	0	0.1	
ETC5040		−0.125	0	0.125	
Gain relative to gain at 1 kHz below 300 Hz	GR_R	–	–	0.125	dB
300 Hz to 3.0 kHz ETC5040A		− 0.125	–	0.125	
3.3 kHz ETC5040A		− 0.35	–	0.03	
3.4 kHz		− 0.70	–	− 0.1	
4.0 kHz		–	–	− 14	
4.6 kHz and above		–	–	− 32	
Absolute delay at 1 kHz	DA_R	–	–	100	μs
Differential envelope delay 1 kHz to 2.6 kHz	DD_R	–	–	100	μs
Single frequency distortion products (f = 1 kHz)	DP_R1	–	–	−48	dB
Distortion at maximum signal level 2.2 Vrms input to sin x/x filter, f = 1 kHz, R_L = 10 kΩ	DP_R2	–	–	−45	dB
Total C-message noise at VF_RO	NC_R	–	3	5	dBrnc0
Temperature coefficient of 1 kHz gain	GAR_T	–	0.0004	–	dB/°C
Supply voltage coefficient of 1 kHz gain	GAR_S	–	0.01	–	dB/V
Crosstalk, transmit to receive 20 log $\frac{VF_RO}{VF_XO}$ (Transmit filter output = 2.2 Vrms, VF_RI = 0 Vrms, f = 0.3 kHz to 3.4 kHz, measure VF_RO)	$CTXR$	–	−80	−70	dB
Gaintraking relative to GA_R	$GRRL$				dB
Output level = 3 dBm0		−0.1	–	0.1	
+ 2 dBm0 to − 40 dBm0		−0.05	–	0.05	
− 40 dBm0 to 55 dBm0		−0.1	–	0.1	

AC ELECTRICAL CHARACTERISTICS (Continued)

RECEIVE OUTPUT POWER AMPLIFIER

Characteristic	Symbol	Min	Typ	Max	Unit
Input leakage current, PWRI ($-3.2\ V \leqq V_{IN} \leqq 3.2\ V$)	IBP	0.1	–	3	μA
Input resistance, PWRI	RIP	10	–	–	MΩ
Output resistance, PWRO+, PWRO – (amplifiers active)	ROP1	–	1	–	Ω
Load capacitance, PWRO+, PWRO–	CLP	–	–	500	pF
Gain, PWRI to PWRO+ (R_L = 600 Ω connected between)	GAP+	–	1	–	V/V
Gain, PWRI to PWRO– PWRO + and PWRO –, input, level = 0 dBm0 (Note 4)	GAP–	–	–1	–	V/V
Gaintraking relative to 0dBm0 output level V = 2.05 Vrms, R_L = 600 Ω (Notes 4, 5) V = 1.75 Vrms, R_L = 300 Ω (Notes 4, 5)	GRpL	 –0.1 –0.1	 – –	 0.1 0.1	dB
Signal/distortion V = 2.05 Vrms, R_L = 600 Ω (Notes 4, 5) V = 1.75 Vrms, R_L = 300 Ω (Notes 4, 5)	S/Dp	 – –	 – –	 –45 –45	dB
Output DC offset, PWRO+, PWRO– (PWRI connected to GNDA)	VOSP	–50	–	50	mV
Power supply rejection of V_{CC} or V_{BB} (PWRI connected to GNDA)	PSRR5	45	–	–	dB

Note 1. Maximum power consumption depend on the load impedance connected to the power amplifier. The specification listed assumes 0 dBm is delivered to 600 Ω connected from PWRO+ PWRO

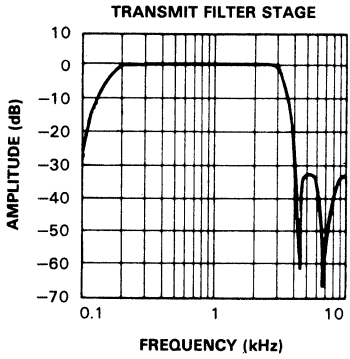
Note 2. Transmit filter input op amp set to the non inverting unity gain mode, with VF_XI+ = 1.1 Vrms, unless otherwise noted

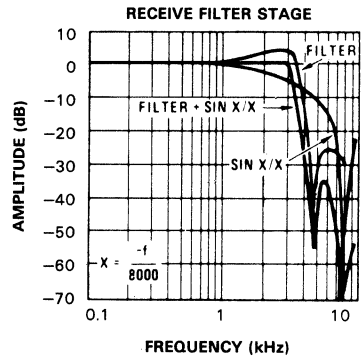
Note 3. The 0 dBm0 level for the filter is assumed to be 1.54 Vrms measured at the output of the XMT or RCV filter

Note 4. The 0 dBm0 level for the power amplifiers is load dependent. For R_L = – 600 Ω to GNDA, the 0 dBm0 level is 1.43 Vrms measured at the amplifier output. For R_L = 300 Ω the 0 dBm0 level is 1.22 Vrms.

Note 5. VF_RO connected to PWRI, input signal applied to VF_RI

TYPICAL PERFORMANCE CHARACTERISTICS





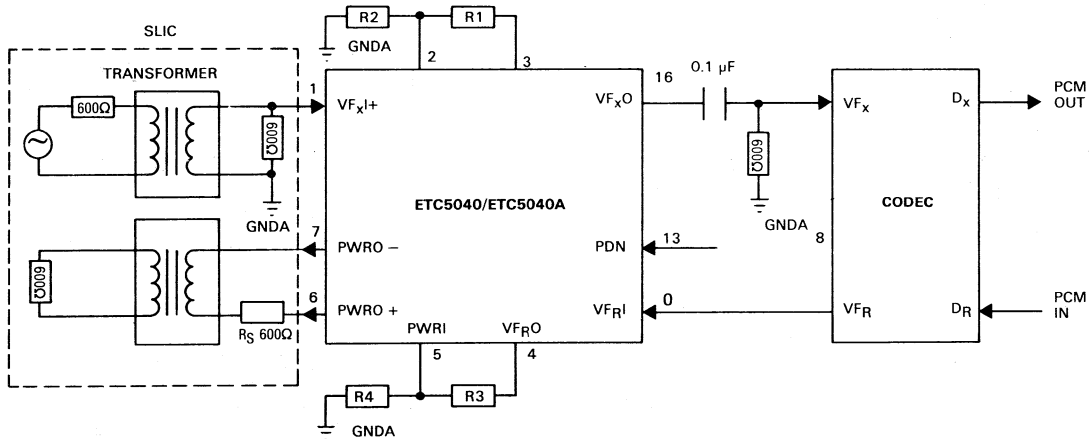


FIGURE 2

Note 1 : Transmit voltage gain $= \frac{R1 + R2}{R2} \times \sqrt{2}$ (The filter itself introduces a 3 dB gain) (R1 + R2 ≧ 10 kΩ)

Note 2 : Receive gain $= \frac{R4}{R3 + R4}$

(R3 + R4 ≧ 10 kΩ)

Note 3 : In the configuration shown, the receive filter power amplifiers will drive a 600 Ω T to R termination to a signal level of 8.5 dBm. An alternative arrangement using a transformer winding ratio equivalent to 1.414.1 and 300 Ω resistor R_S, will provide a maximum signal level of 10 dBm across 600 Ω termination impedance.

FUNCTIONAL DESCRIPTION

The ETC 5040/ETC 5040A monolithic filter contains four main sections; Transmit Filter, Receive Filter, Receive Filter Power Amplifier, and Frequency Divider/Select Logic (figure 1). A brief description of the circuit operation for each section is provided below.

Transmit Filter

The input stage of the transmit filter is a CMOS operational amplifier which provides an input resistance greater than 10 MΩ, a voltage gain of greater than 10.000, low power consumption (less than 3 mW), high power supply rejection, and is capable of driving a 10 kΩ load parallel with up to 25 pF. The inputs and output of the amplifier are accessible for added flexibility. Non-inverting mode, inverting mode, or differential amplifier mode operation can be implemented with external resistors. It can also be connected to provide a gain of up to 20 dB without degrading the overall filter performance.

The input stage is followed by a prefilter which is a two-pole RC active low pass filter designed to attenuate high frequency noise before the input signal enters the switched-capacitor high pass and low pass filters.

A high pass filter is provided to reject 200 Hz or lower noise which may exist in the signal path. The low pass portion of the switched-capacitor filter provides stopband attenuation which exceeds the D3 and D4 specifications as well as the CCITT G712 recommendations.

The output of the transmit filter, the postfilter, is also a two-pole RC active low pass filter which attenuates clock frequency noise by at least 40 dB. The output of the transmit filter is capable of driving a ± 3.2 V peak to peak signal into a 10 kΩ load in parallel with up to 25 pF.

Receive filter

The input stage of the receive filter is a prefilter which is similar to the transmit prefilter. The prefilter attenuates high frequency noise that may be present on the receive input signal. A switched capacitor low pass filter follows the prefilter to provide the necessary passband flatness, stopband rejection and sin x/x gain correction. A postfilter which is similar to the transmit postfilter follows the low pass stage. It attenuates clock frequency noise and provides a low output impedance capable of directly driving an electronic subscriber-line-interface circuit.

Receive filter power amplifiers

Two power amplifiers are also provided to interface to transformer coupled line circuits. These two amplifiers are driven by the output of the receive postfilter through gain setting resistors, R3, R4 (figure 2). The power amplifiers can be deactivated, when not required, by connecting the power amplifier input (pin 5) to the negative power supply V_{BB}. This reduces the total filter power consumption by approximately 10 mW-20 mW depending on output signal amplitude.

Power down control

A power down mode is also provided. A logic 1 power down command applied on the PDN pin (pin 13) will reduce the total filter power consumption to less than 1 mW and turn the power amplifier outputs into high impedance state.

Frequency divider and select logic circuit

This circuit divides the external clock frequency down to the switching frequency of the low pass switched capacitor filters. The divider also contains a TTL-CMOS interface circuit which converts the external TTL clock level to the CMOS logic level required for the divider logic. This interface circuit can also be directly driven by CMOS logic.

A frequency select circuit is provided to allow the filter to operate with 2.048 MHz, 1.544 MHz or 1.536 MHz clock frequen-cies. By connecting the frequency select pin CLKO (pin 14) to V_{CC}, a 2.048 MHz clock input frequency is selected. Digital ground selects 1.544 MHz and V_{BB} selects 1.536 MHz.

APPLICATIONS INFORMATION

Gain adjust

Figure 2 shows the signal path interconnections between the ETC5040/ETC5040A and single-channel CODEC. The transmit RC coupling components have been chosen both for minimum passband droop and to present the correct impedance to the CODEC during sampling.

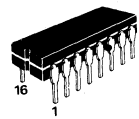
Optimum noise and distortion performance will be obtained from the ETC5040/ETC5040A filter when operated with system peak overload voltages of ± 2.5 V to ± 3.2 V at VF_XO and VF_RO. When interfacing to a PCM CODEC with a peak overload voltage outside this range, further gain or attenuation may be required.

For example, the ETC5040/ETC5040A filter can be used with CODEC which has a 5.5 V peak overload voltage. A gain stage following the transmit filter output and an attenuation stage following the CODEC output are required.

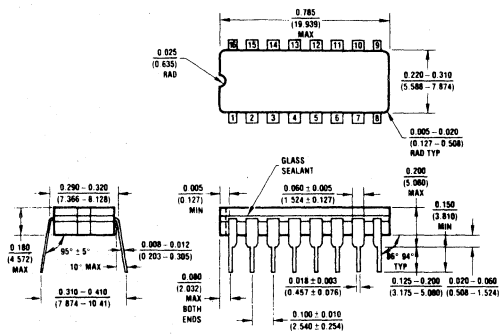
Board layout

Care must be taken in PCB layout to minimize power supply and ground noise. Analog ground (GNDA) of each filter should be connected to digital ground (GNDD) at a single point, which should be bypassed to both power supplies.

Further power supply decoupling adjacent to each filter and CODEC is recommended. Ground loops should be avoided, both between the GNDA traces of adjacent filters and CODECs.



J SUFFIX
CERDIP PACKAGE



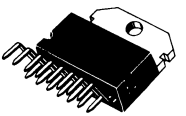
This kit of two circuits is designed to ensure the BORSHT functions of the central office line card.

- Battery:
  - — Normal and reverse mode.
  - — Power down mode.
  - — Power denial.
- Overvoltage:
  - — Voltage and current limitation.
- Ringing:
  - — Ringing is externally injected.
  - — Ring trip is internally detected.
- Signaling:
  - — Off-Hook detection.
  - — Ground key detection.
  - — Dialing detection.
- Hybrid:
  - — 2 to 4-wire conversion.
- Test:
  - — External.
- Complementary functions:
  - — Power saving.
  - — Tax metering signal sending.
  - — Automatic reset at power-up.

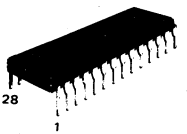
SUBSCRIBER LINE INTERFACE CIRCUIT (SLIC)

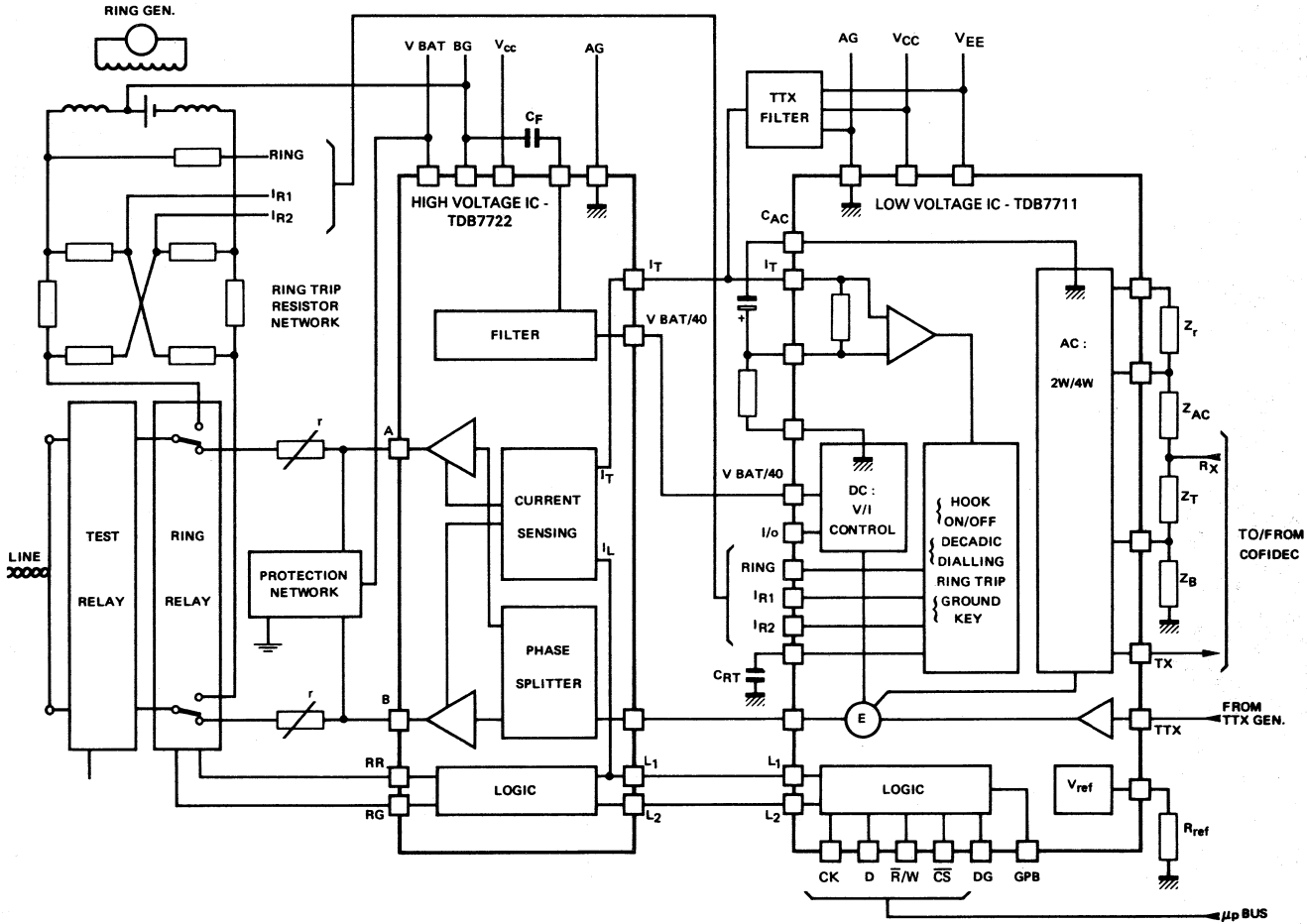
CASES

CB 501



CB 132




RING GEN.
V BAT
BG
Vcc
AG
CF
RING
IR1
IR2
RING TRIP RESISTOR NETWORK
HIGH VOLTAGE IC - TDB7722
FILTER
IT
V BAT/40
TTX FILTER
AG
VCC
VEE
LOW VOLTAGE IC - TDB7711
CAC
AC : 2W/4W
ZR
ZAC
RX
ZT
ZB
TO/FROM COFIDEC
TX
FROM TTX GEN.
TTX
LINE
TEST RELAY
RING RELAY
PROTECTION NETWORK
r
A
B
CURRENT SENSING
IL
PHASE SPLITTER
DC : V/I CONTROL
I/o
RING
IR1
IR2
HOOK
ON/OFF
DECADIC
DIALLING
RING TRIP
GROUND KEY
CRT
E
RR
RG
LOGIC
L1
L2
Vref
Rref
CK
D
R/W
CS
DG
GPB
µp BUS

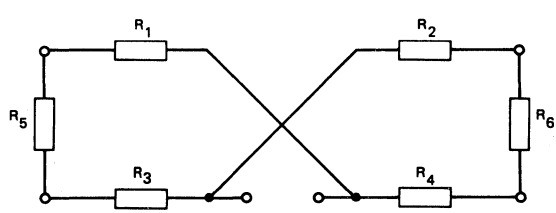
FUNCTIONAL DESCRIPTION

- Battery:
  - — Programmable current limit.
  - — Apparent battery independent of actual battery.
  - — Programmable feeding resistor (ext. comp.).
  - — Max. battery voltage is 72 V.
  - — Power saving possibilities.
  - — In power down mode, power dissipation is 70 mW (V_{BAT} = 48 V).
  - — In power denial, line feeding disabled. Line is in high impedance position.
- Overvoltage: power dissipation is maintained inside S.O.A. of output devices. Thermal warning.
- Ringing:
  - — Large AC and DC voltages allowed.
  - — Perturbation free detection system.
- Hybrid:
  - — Synthesized impedance externally programmable (complex impedance possible).
  - — Balance impedance externally programmable (complex impedance is possible).
- Complementary functions:
  - — Power saving by comparison of battery voltage and line voltage and connection of a reduced voltage battery.

EXTERNAL COMPONENTS
(See block diagram)

Name	Function	Typical value
r	Protection CTP resistor	⩾ 30 Ω
C_f	Battery voltage filtering capacitor	470 nF/100 V
R_f	Feeding bridge programming resistor, must be equal to: (total desired value - 2r) x 2.5	1 KΩ
C_{AC}	A.C. coupling capacitor	47 µF/10 V
C_{RT}	Ring trip capacitor (50Hz ring freq.)	220 nF/10 V/low leakage
R_{ref}	Reference resistor	16 KΩ 1 %
Z_r	Compensation of CTP resistor effect on gain and impedance, must be equal to : 50 x 2r	3 KΩ (r = 30 Ω)
Z_{AC}	Impedance programing network, must be equal to : 50 x (Desired imp. val. - 2 x r) NB : can be complex	27 KΩ (Z = 600 Ω)
Z_T	K x Desired impedance value	60 KΩ (Z = 600 Ω)
Z_B	K x Desired balance impedance val. NB : can be complex	60 KΩ (Z_{Bal} = 600 Ω)
C_{BW}	Bandwith capacitor, must be such that : $C_{BW} \times (Z_r + Z_{AC}) = 8\ \mu s$	270 pF/10 V
C'_{BW}	Compensation of bandwith cap. for transhybrid rejection $C'_{BM} \times Z_T = 8\ \mu s$	120 pF/10 V

Ring trip network



$R_1 = R_2 = R_3 = R_4$ relative precision ±0.5%.

R_1 = 500K absolute precision ±5%.

$R_5 = R_6 = 200\Omega/2W$ ±5%.

LOGIC INTERFACE

Input and output structures are serial register type.

Data input

Two 8-bit words can be written in the SLIC.

B7	B6	B5	B4	B3	B2	B1	B0
Val	Data	Data	Data	Data	Data	Data	Regist Select

For B0: "0"
- B1: Power down
- B2: Special DC characteristics
- B3: Real battery voltage
- B4: I Limit 1 (30 mA)
  Remark: Power denial mode if $B1.\overline{B4}.\overline{B5}.\overline{B6}$ = "1"
- B5: I Limit 2 (20 mA)
- B6: I Limit 3 (12 mA)
- B7: Validation

For B0: "1"
- B1: General purpose
- B2: Analog input/output "0" = Input mode
- B3: TTX
- B4: Reverse battery
- B5: Ringing
- B6: Not used
- B7: Validation

Data output

One 12-bit word can be read in the SLIC.

B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Val	Data Input	Data Input	Data Input	Data Input	Data Input	Data Input	Regist Select	TW	GK	CRB	HS

Last loaded word (for checking).

NOTE: - HS is always present on Data bus even without clock pulse
- At first clock rising edge HS can be read a second time.

HS: Hook Status

CRB: Comparison Result Bit between V BAT and V LINE

GK: Ground Key

TW: Thermal Warning

The data are latched in the SLIC when B7 (data input) = "1" (Validation) and $\overline{CS}$ = "1"

The data are stored in the 6 first registers if B0 = "1" and in the 6 last registers if B0 = "0"

The data are written in the shift register at each clock rise edge when $\overline{CS} = 0$ and $\overline{R}/W = 1$

The data are read at each clock rise edge when $\overline{CS} = 0$ and $\overline{R}/W = 0$

The first bit (B0 = HS) can be read without clock when $\overline{CS} = 0$

MAXIMUM RATINGS

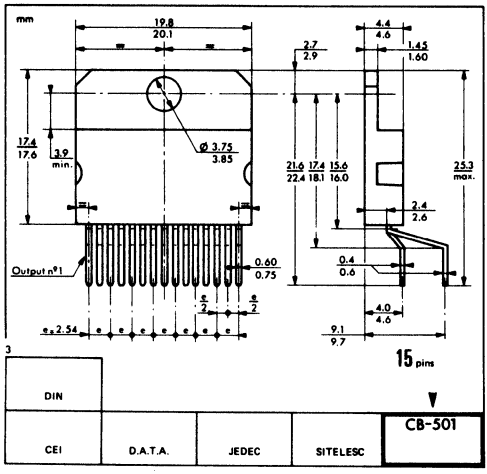
Rating	Symbol	Value	Unit
Power supply			
Battery voltage	V_{BAT}	- 20 to - 72	V
Supply voltage	V_{CC}	+ 4.5 to + 5.5	V
	V_{EE}	- 4.5 to - 5.5	V
Voltage drop between analog ground (AG) and battery ground (BG) (For $\|V_{BAT}\| \geq 30$ V)		- 2 to + 2	V
Voltage drop between analog ground (AG) and digital ground (DG)		- 1 to + 1	V
Power supply rejection ratio (speech band) with : 0.2 V voltage ripple on V_{CC}/V_{EE} 0.6 V voltage ripple on V_{BAT}		40	dB
Line			
Line current (I Longituvinal + I Transversal)		120 max	mA
Line voltage		$\|V_{BAT}\|$ - 13	V
Power dissipation, in power down mode (line current = 0)		70	mW
Overvoltage protection			
Voltage on Tip or Ring during overvoltage		TBD	
All other inputs/outputs are protected by diode clamping to supply rails			
Temperature			
Operating temperature range	T oper	0 to + 70	°C
Storage temperature range	T stg	- 55 to + 150	°C
Junction (thermal warning sets SLIC in power denial mode automatically)		150	°C
Thermal resistance: junction to ambient		40	°C/W
(case = SIL 15: junction to case		3	°C/W

ELECTRICAL OPERATING CHARACTERISTICS Unless otherwise specified

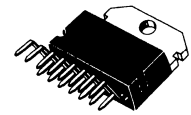
T_A = 25 °C, V_{BAT} = - 30 to - 72 V, V_{CC} = + 5 V ± 5 %, V_{EE} = - 5 V ± 5 %
Transversal line current: I_T = 30 mA 0)
Longitudinal line current: I_L = 0

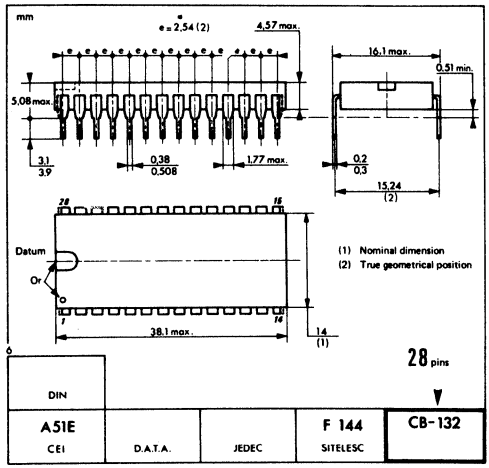
Characteristic	Symbol	Min	Typ	Max	Unit
Line feeding characteristics					
Line voltage (see DC curve, $I_T = I_{limit}$)	I_{Limit}	0	—	$\|V_{BAT}\| - 13$	V
Line current (see DC curve)		0	—	I_{limit}	mA
Loop current at constant current feed (I_{prog} programmed by steps thru the bus)		- 5 %	I_{prog}	+ 5 %	mA
Line voltage at constant voltage feed		—	$\|V_{BAT}\| - 13$	—	V
Feeding bridge resistor (set by ext. comp.)		60		800	Ω
Loop current in power denial mode		—	—	1	mA
Loop current matching in normal/reverse battery mode		- 1 %	—	+ 1 %	
Signaling					
Off-hook detection threshold (Power down or power up)		7	—	10	mA
On hook detection threshold (Power down or power up)		4	—	7	mA
Off hook/on hook hysteresis		—	3	—	mA
Dialing rate		—	—	22	pulse/s
Dialing distortion		—	—	3	ms
Off-hook response time (I_{DC} = 20 mA; power down)		—	—	70	ms
Ground key detection threshold		10	—	20	mA
Ground key detection response time ($I_{LONG\ DC}$ = 20 mA)		—	—	250	ms
Ring trip detection threshold		5	—	10	mA
Ringing frequency		16	—	70	Hz
Ring trip delay (I_{DC} = 15 mA, Ring frequency = F_R)		—	—	$4/F_R$	s
Teletaxe sending					
Line level (F < 18 KHz, RL = 200 Ω)		2.2	2.5	—	Vrms
Gain		7	8	9	
AC characteristics (without TTX signal)					
- 2 Wire port					
Overload level (100 < f < 4000 Hz)		6.27	—	—	dBm
Return loss (300 < f < 3400 Hz)		20	—	—	dB
Longitudinal impedance (on/off - hook - r = protection P TC)		r - 10	—	r + 10	Ω/wire
Longitudinal balance					
100 < f < 3400 Hz		52	60	—	dB
100 < f < 3400 Hz on - hook		30	40	—	dB
Longitudinal signal generation (100 < f < 3400 Hz)		52	60	—	dB
Longitudinal handling capability (on/off hook)			35	—	mA rms/wire
- 4 Wire port					
Overload level RX/TX		3.17	—	—	dBm
TX output offset voltage		—	—	100	mV
RX input offset voltage		—	—	50	mV
TX output impedance		—	—	10	Ω
RX input impedance		1	—	—	MΩ
Insertion loss RX to line, line to TX (f = 820 Hz, $V_{TX/RX}$ = 0 dBm)		- 0.15	0	+ 0.15	dB
Frequency response (300 < f < 3400 Hz)		- 0.1	0	+ 0.1	dB
Gain linearity					
$V_{TX/RX}$: + 3 to - 40 dBm		- 0.05	—	+ 0.05	dB
- 40 to - 50 dBm		- 0.1	0	+ 0.1	dB
- 50 to - 55 dBm		- 0.2	0	+ 0.2	dB
Transhybrid loss (with theoretical ext. comp. values level 0 dBm)		30	40	—	dB
Harmonic distortion RX/TX (0 dBm, f = 820 Hz)		- 50	—	—	dB
Noise (V_{TX}/V_{LINE})		- 75	—	—	dBmp
PSRR (F = 300 to 3400 Hz)		- 40	—	—	dB
Relay driver					
Sinking current		—	—	200	mA
Leakage current		—	—	100	μA
Voltage drop (switch on)		—	—	1	V
Breakdown voltage		—	80	—	V
Digital interface					
Clock frequency		—	128	150	KHz

PHYSICAL DIMENSIONS

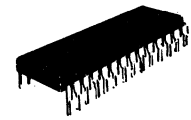


CB-501





CB-132



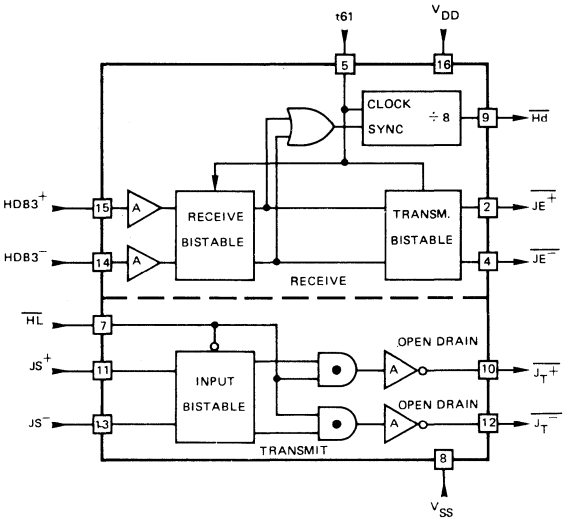
NOTES

PCM LINE TRANSCEIVER

The EF 7332 provides the interface between a 2.048 or 1.544 Mbits/s PCM trunk and the switching equipment. The receiving side amplifies and reshapes the bipolar signals from a receive transformer and extracts from the signals the distant clock Hd. On the transmitting side it calibrates pulses in terms of duration and amplitude by means of transistor circuits directly coupled to the primary winding of a transmit transformer.

- NMOS technology.
- Operates from + 5 V supply.
- Digital technology throughout.
- Extracts distant clock transmitted by a PCM trunk.
- Can handle peak to peak jitter amplitude up to 0.25 bit for an 8-bit period.
- Integrated transmit and receive amplifiers.
- TTL-compatible input/ output.

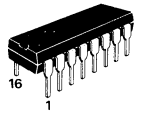
BLOCK DIAGRAM



NMOS

PCM LINE TRANSCEIVER

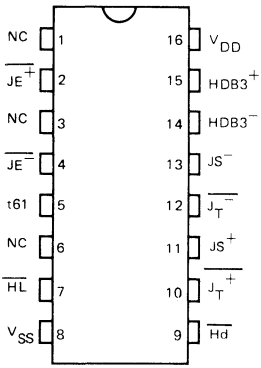
CASE CB-79



P SUFFIX
PLASTIC PACKAGE

C SUFFIX
CERAMIC PACKAGE

PIN ASSIGNMENT



PIN DESCRIPTION

Power supply

Name	Type	No	Function	Description
V_{SS}	S	8	Supply	Ground
V_{DD}	S	16		+5 V ± 5 %

Receive

t b1	I	5	–	16 384 kHz or 15 352 kHz clock (minimum high and low duration: 20 ns) Synchronises outputs $\overline{JE^+}$, $\overline{JE^-}$ and $\overline{Hd}$.
HDB 3+	I	15	Data	Bipolar signals in HDB3 code are received from the receive transformer. The amplitude of these signals is between –5 V and +5 V. Each positive pulse on HDB3+ (HDB3–) resynchronises the circuit clock and is reconstitutedin calibrated form on output $\overline{JE^+}$ ($\overline{JE^-}$). Negative pulses have no effect on this circuit as the inputs are protected.
HDB 3–	I	14	data	
$\overline{JE+}$	O	2	Data	Received HDB3 signals are resynchronised with $\overline{Hd}$ and calibrated in terms of amplitude (TTL LS compatible levels).
$\overline{JE-}$	O	4	output (I/ C trunk)	The distant clock is recovered from the signal on HDB3+, HBD3–.
$\overline{Hd}$	O	9	Distant clock output	The nominal frequency is 2 048 kHz or 1544 kHz in the absence of jitter.

Transmit

$\overline{H\ 1}$	I	7	Clock	Local clock, nominal frequency 2048 kHz or 1544 kHz.
JS+	I	11	Data	The data is recognised on the falling edge of H1.
JS–	I	13	input (O/ G trunk)	
$\overline{JT+}$	O	10	Data	These open drain outputs are connected to the windings of the transmit transformer. Recognition of a "1" on $\overline{JS^+}$ ($\overline{JS^-}$) grounds the winding of transformer connected to $\overline{JT^+}$ ($\overline{JT^-}$) for the duration of "1" level of H1. These outputs are protected against short-circuits by current limiting internal to the circuit.
$\overline{JT-}$	O	12	output (transmitted trunk)	

FUNCTIONAL DESCRIPTION

Receive path

The PCM Line Transceiver receives directly from the receive transformer on inputs HDB3+ and HDB3– data in HDB3 code. It synchronises this data by means of the clock on input t61 and converts it to voltage pulses of calibrated duration on outputs $\overline{JE+}$ and $\overline{JE-}$. To be recognised correctly by this circuit the received data must satisfy minimum and maximum duration conditions (Cf. page 4).

Distant clock $\overline{Hd}$ is provided by a counter which divides by 8 the frequency of the clock t61. This counter is resynchronised with the data of the PCM trunk on each positive-going edge at HDB3+ or HDB3–. The period 0.25 eb of $\overline{Hd}$ may vary by within a period of 8 eb without degradation of the phase relationships between $\overline{JE+}$ $\overline{JE-}$ and $\overline{Hd}$ (Cf. receive timing diagram No 1). If the variation occurs in an interval exceeding 4 eb but less than 8 eb the phase relationships between $\overline{JE+}$, $\overline{JE-}$ and $\overline{Hd}$ are modified (See receive timing diagrams 2 and 3).

In all cases outputs $\overline{JE+}$ and $\overline{JE-}$ remain stable on either side of the falling edge of $\overline{Hd}$ so as to be sampled correctly by the EF7333.

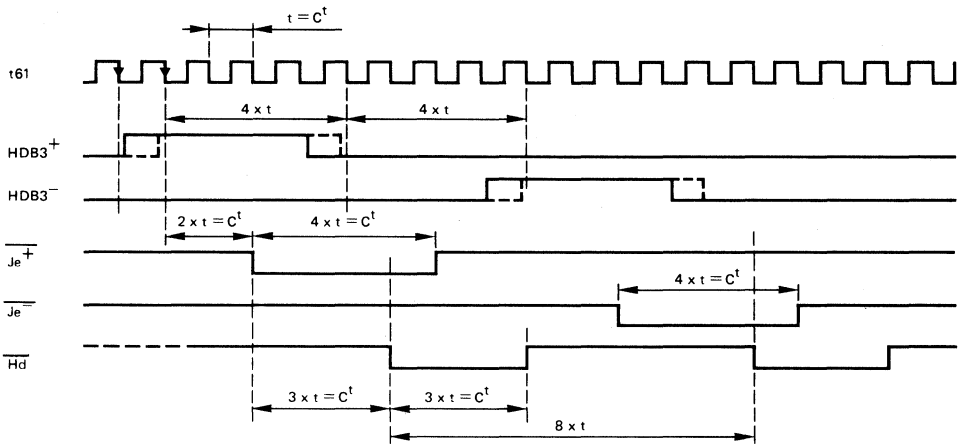
Transmit path

The signals JS+ and JS– to transmit are sampled on the falling edge of clock signal $\overline{Hl}$ and calibrated by the duration for which this signal is high.

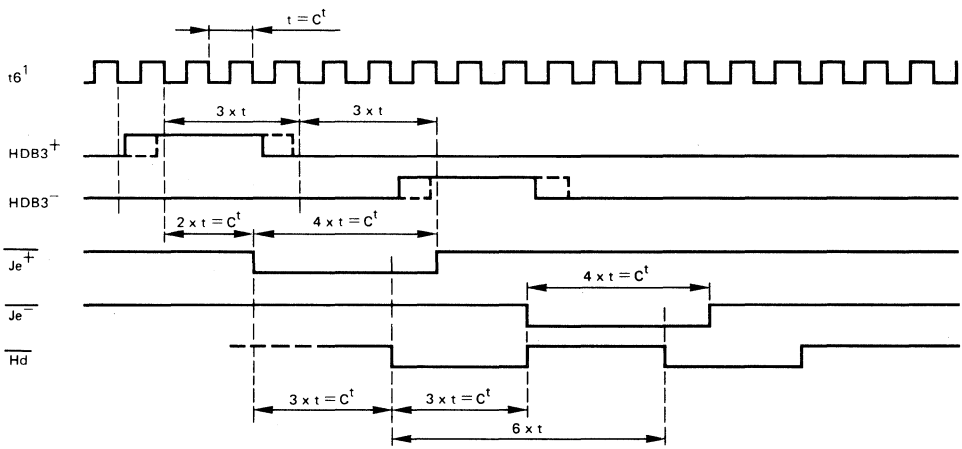
Open drain outputs $\overline{JT+}$ and $\overline{JT-}$ drive the primary windings of the transmit transformer directly. They are protected against overcurrents occurring should the secondary windings of this transformer be short-circuited, in which case the primary behaves as a very low resistance connecting the output to supply rail V_{DD}.

TIMING DIAGRAM

1 – EXTERNAL SIGNALS WITH JITTER < 0.25 BIT WITHIN 8-BIT PERIOD

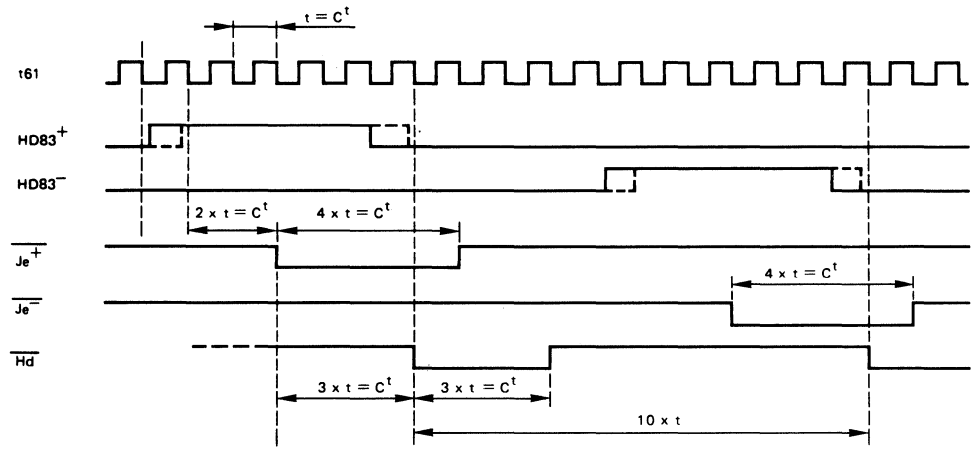


2 – EXTERNAL SIGNALS WITH HDB3^{+} AND HDB3^{-} SIGNAL PERIOD 6 x t

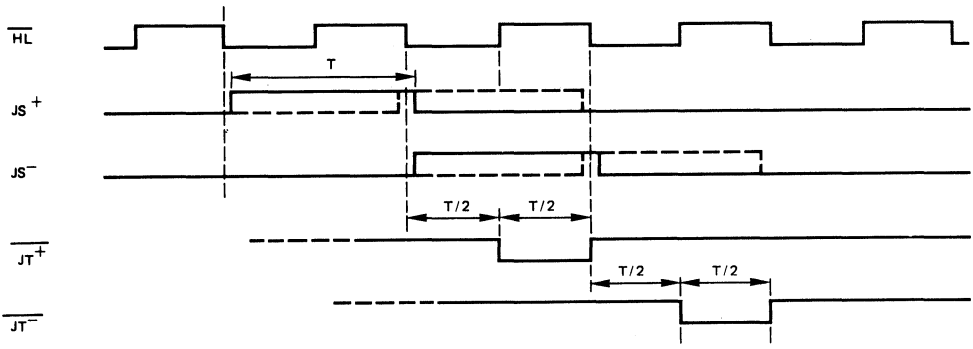


c^t = CONSTANT

3 – EXTERNAL SIGNALS WITH HDB3 + AND HDB3 – SIGNAL PERIOD 10 x t.

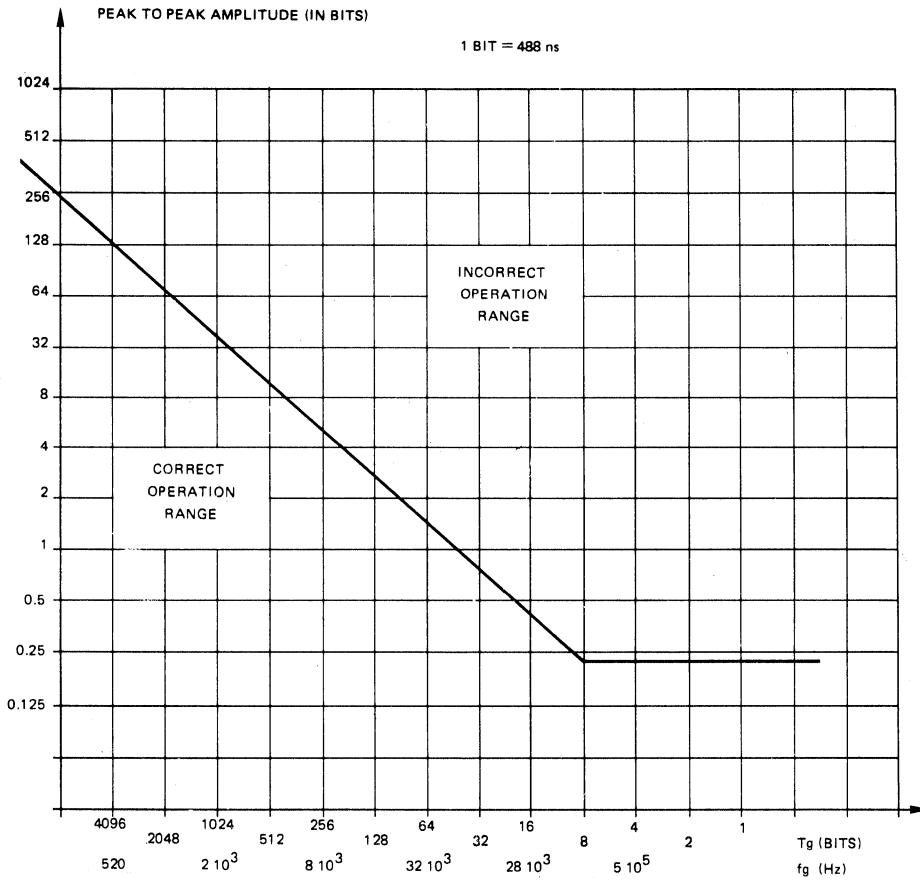


TRANSMIT



Ct = CONSTANT

EF7332 OPERATING RANGE AS A FUNCTION OF JITTER AND FREQUENCY

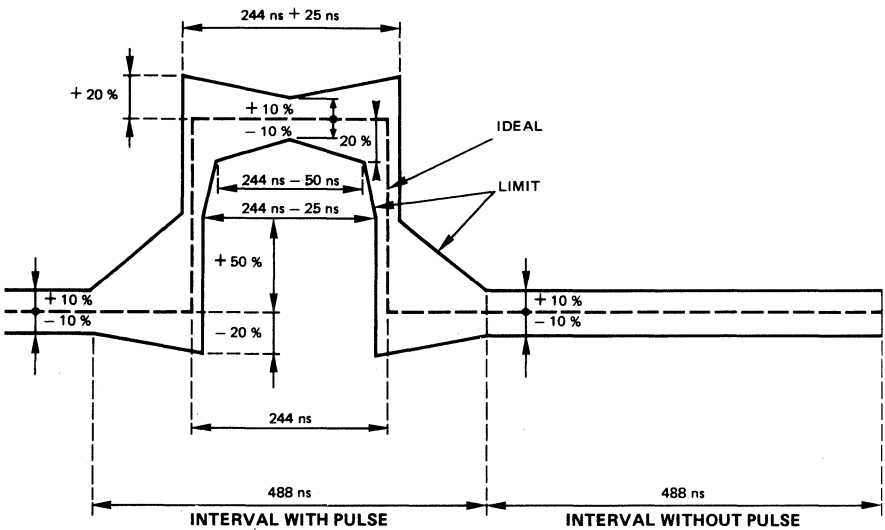


Tg = « PERIOD » OF THE JITTER IN BITS

fg = « FREQUENCY » OF THE JITTER IN Hz

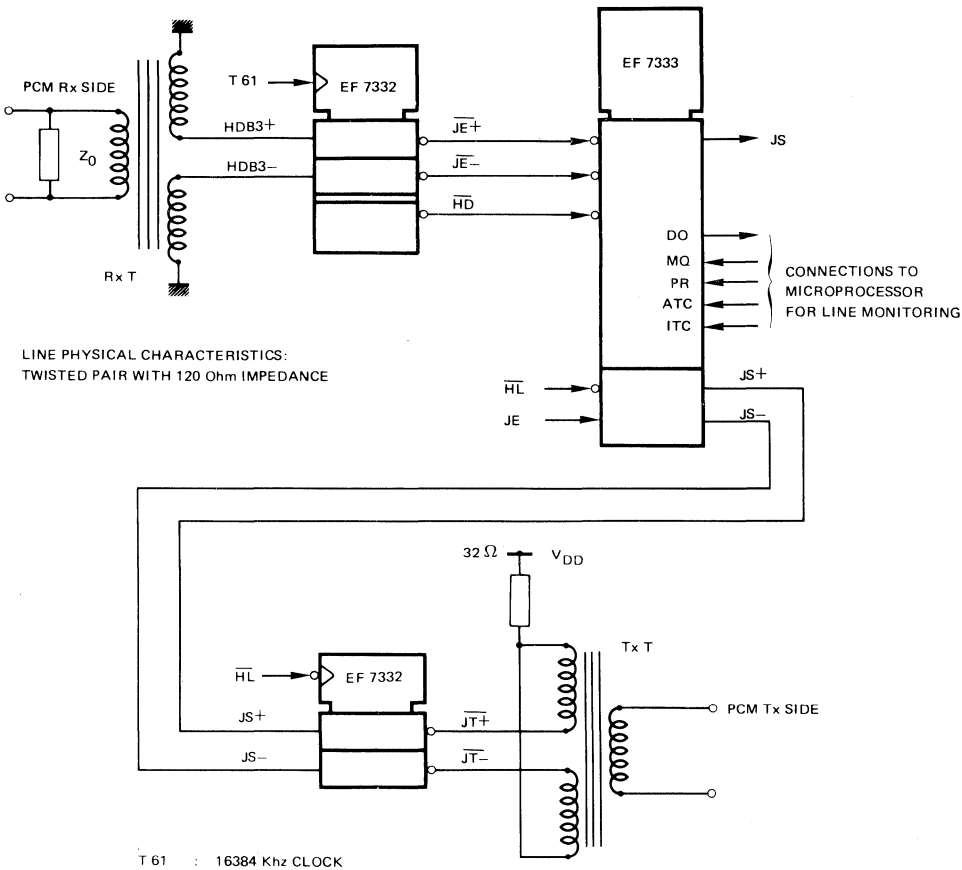
Pulse limiting curves for 2 048 kbit/s CEPT PCM trunk.

The limiting curves below are for a resistive load of 120 Ω connected across the secondary winding of the transmit transformer.



TYPICAL APPLICATION

USING EF 7333 AND EF 7332 IN A 2048 Khz PCM LINE
FOR DATA TRANSMISSION/RECEPTION AND FRAME MONITORING



LINE PHYSICAL CHARACTERISTICS:
TWISTED PAIR WITH 120 Ohm IMPEDANCE

T 61 : 16384 Khz CLOCK
Rx T : LINE RECEIVE TRANSFORMER
Tx T : LINE TRANSMIT TRANSFORMER
$\overline{HL}$: LOCAL 2048 Khz CLOCK

NOTE : EF 7332 LAY OUT CONSIDERATIONS: FOR CORRECT OPERATION OF TRANSMISSION DRIVERS A 100 nF DECOUPLING CAPACITOR MUST BE CONNECTED TO VDD AND LOCATED AS CLOSE AS PRACTICAL

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply voltage	$V_{DD} - V_{SS}$	$-0.3\ V \geqslant V_{DD} - V_{SS} \geqslant 7\ V$	V
Input voltage range (except inputs HDB3 + and HBD3–)	V_E	$V_{SS} - 0.3\ V \geqslant V_I \geqslant V_{DD} + 0.3\ V$	V
Maximum power	P	$P_{max} = 250$ mW in 0°C to 70°C range	mW
Storage temperature range	T_{stg}	– 55°C to + 150°C	°C

STATIC ELECTRICAL CHARACTERISTICS - TYPICAL VALUES ET + 25°C

Ambient temperature range: 0°C to + 70°C.

Characteristic	Symbol	Min	Typ	Max	Unit
Positive power supply	V_{DD}	+ 4.75	+ 5	+ 5.25	V
Supply current	I_{DD}	+ 4.75	20	30	mA
Stray capacitance between one input and ground (outputs loaded with $C_L = 25$ pF)	–	–	5	10	pF
Inputs					
Voltage at input HDB3⁺/ HDB3⁻					
when low	–	– 5	–	0.6	V
when high	–	2.2	–	5	V
Resistance at input HDB3⁺/ HDB3⁻ (inverse voltage)	–	–	10	–	kΩ
Voltage at input JS⁺/ JS⁻/ $\overline{H1}$ ($V_I = -5$ V)					
when low	–	– 0.3	–	0.6	V
when high	–	2.2	–	V_{DD}	V
Voltage at input t61					
when low	–	0	–	0.6	V
when high	–	2.6	–	V_{DD}	V
Output					
Voltage at output $\overline{Hd}$/ $\overline{Je^+}$/ $\overline{Je^-}$					
when low ($I_{OL} = 0.4$ mA)	–	0	–	0.4	V
when high ($I_{OH} = -40$ µA)	–	2.6	–	V_{dd}	V
Voltage at output $\overline{JT^+}$/ $\overline{JT^-}$ when low ($R_L = 175\ \Omega$ to V_{DD})	–	250	450	750	mV
Current at output $\overline{JT^+}$/ $\overline{JT^-}$ when high ($V_{OH} = 12$ V9	–	–	–	100	µA
Current at output $\overline{JT^+}$1$\overline{JT^-}$ (output current limited)	–	–	–	35	mA

DYNAMIC CHARACTERISTICS

Typical values at + 25°C (o°C < T_A < + 70°C)

Clocks

Characteristic	Symbol	Min	Typ	Max	Unit
Clock T61 (Fig. 1)	–	–	12 352	–	kHz
Duration	–	–	16 384	16 500	kHz
when low	t_{PLH}	20	–	–	nS
when high	t_{PHL}	20	–	–	nS
Clock $\overline{H1}$ (fig. 3)	–	–	1544	–	kHz
	–	–	2048	2200	kHz
Fall time	t_{THL}	–	–	30	nS
Rise time	t_{TLH}	–	–	30	nS

Inputs

Inputs HDB3⁺/ HDB3⁻ (f = 12352 kHz, fig.2)	–	81	–	405	nS
Min. pulse duration (f = 16384 kHz)	t_{PHL}	61	–	–	nS
Max. pulse duration (f = 16384 kHz)	t_{PLH}	–	–	305	nS
Inputs JS⁺/ JS⁻ (fig. 3)					
Set up time	$t_{set\text{-}up}$	20	–	–	nS
Hold time	t_{hold}	30	–	–	nS

Outputs

Outputs $\overline{JE^+}$/ $\overline{JE^-}$ relative to $\overline{Hd}$ (C_L = 25 pF, fig. 4)					
Set up time	t Set-up	150	3 x t	–	nS
Hold time	t_{hold}	30	t	–	nS
Fall time	t_{THL}	–	15	–	nS
Rise time	t_{TLH}	–	20	–	nS
Outputs $\overline{JT^+}$/ $\overline{JT^-}$ (R_L = 175 Ω to V_{DD}, Fig. 5)					
Pulse duration (C_L = 25 pF)	t_{WM}	–	–	–	–
H_L = 2048 kHz	–	219	244	269	nS

FIG. 1

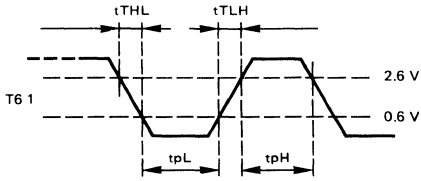


FIG. 2

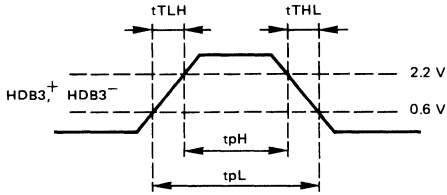


FIG. 3

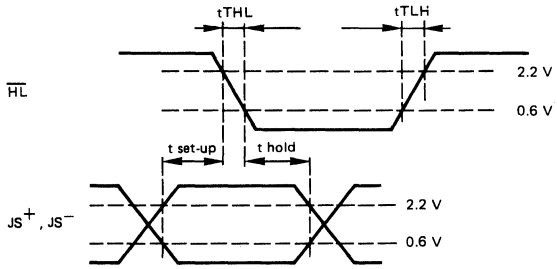


FIG. 4

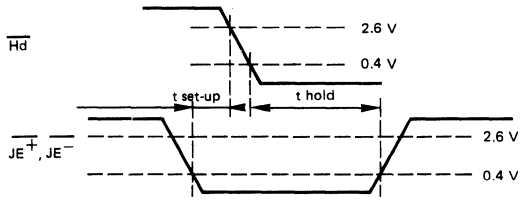
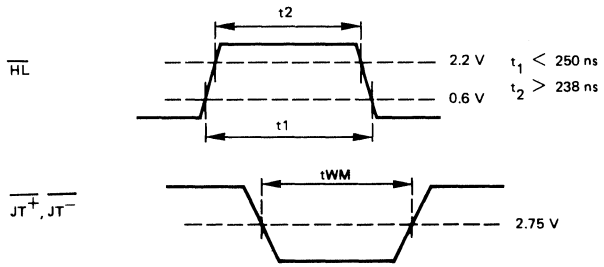
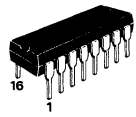


FIG. 5

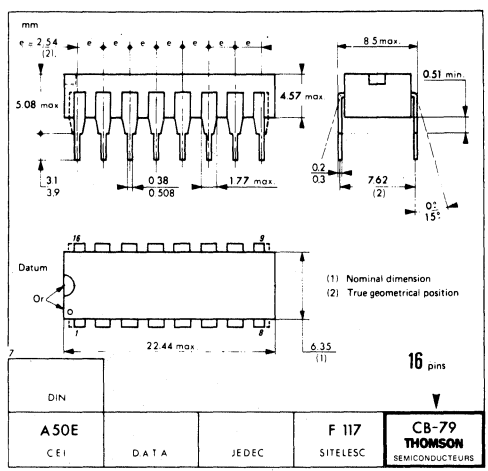


CASE CB-79



C SUFFIX
CERAMIC PACKAGE

P SUFFIX
PLASTIC PACKAGE



THOMSON COMPONENTS

MOSTEK

COMMUNICATIONS PRODUCTS

APPLICATION NOTE

CLOCK EXTRACTION MODULE-CIRCUIT 73321 AND TERMINAL SWITCHING MODULE-CIRCUIT 7333

1 - CLOCK EXTRACTION MODULE (MEH) - CIRCUIT 73321

1.1 Circuit description

The specifications of this circuit are given in the TELECOM ICS catalog by THOMSON-SEMICONDUCTEURS. This circuit provides the 2 Mbit/s - 6 dB -HDB3 interface as per international standards.

PCM junction time recovery as defined by the CCITT generally requires a damped oscillator sustained by logic 1's detected by the PCM junction.

Most of the time the oscillator consists of coils, capacitors, basic capacitors, and varicaps whose wiring diagram is not easily integrated.

The solution retained is the use of a digital integrated circuit for PCM junction transmission and reception (Fig. 1).

A 16,384 kHz crystal oscillator delivers a square clock signal with a 61 ns period to 73321 circuit(s). The circuit accepts external clock frequencies lower than or equal to 16,384 kHz for in line outputs smaller than or equal to 2,048 kbits/s.

1.2 Bipolar and HDB3 conversion review

Portion A of Fig. 2 shows a series of NRZ (non return to zero) linear data to be transmitted.

The logic 1 or 0 is present throughout the propagation of a bit. There is no return to zero for a logic 1 during this time.

In portion B this signal is converted to bipolar form, logic 0's remain as they are but 1's alternately take a positive and a negative value.

In portion C and D of the figure this same signal is converted to HDB3; not more than three 0's may be received in line. A fourth 0 would systematically be transmitted as a 1 whose bipolarity has been violated with respect to the last 1 transmitted but whose bipolarity is respected compared to the last violation.

Two cases are possible:

— In C of figure 2, the preceding violation not represented on the figure was positive, the first 4-bit word fill-in sequence will be:

0 0 0 V

where V is negative, the following fill-in sequence will be :

B 0 0 V

where B is a signal element different from zero, that is equal to + 1 in this case since B should respect the polarity with respect to the last logic 1.

— In D of figure 2, the preceding violation, not represented on the figure was negative. In this case the first fill-in sequence will be:

B 0 0 V

where V is positive since the preceding violation was negative, and in order that this polarity really be a bipolarity violation, B is also positive. The value of the second sequence is:

B 0 0 V

where V is negative since the preceding bit V was positive and B is also negative and not equal to zero to ensure violation.

Then, it is verified that the sequences described are such that the in-line dc component is really equal to zero. Thus it is possible to use pulse transformers for galvanic insulation between line and terminals.

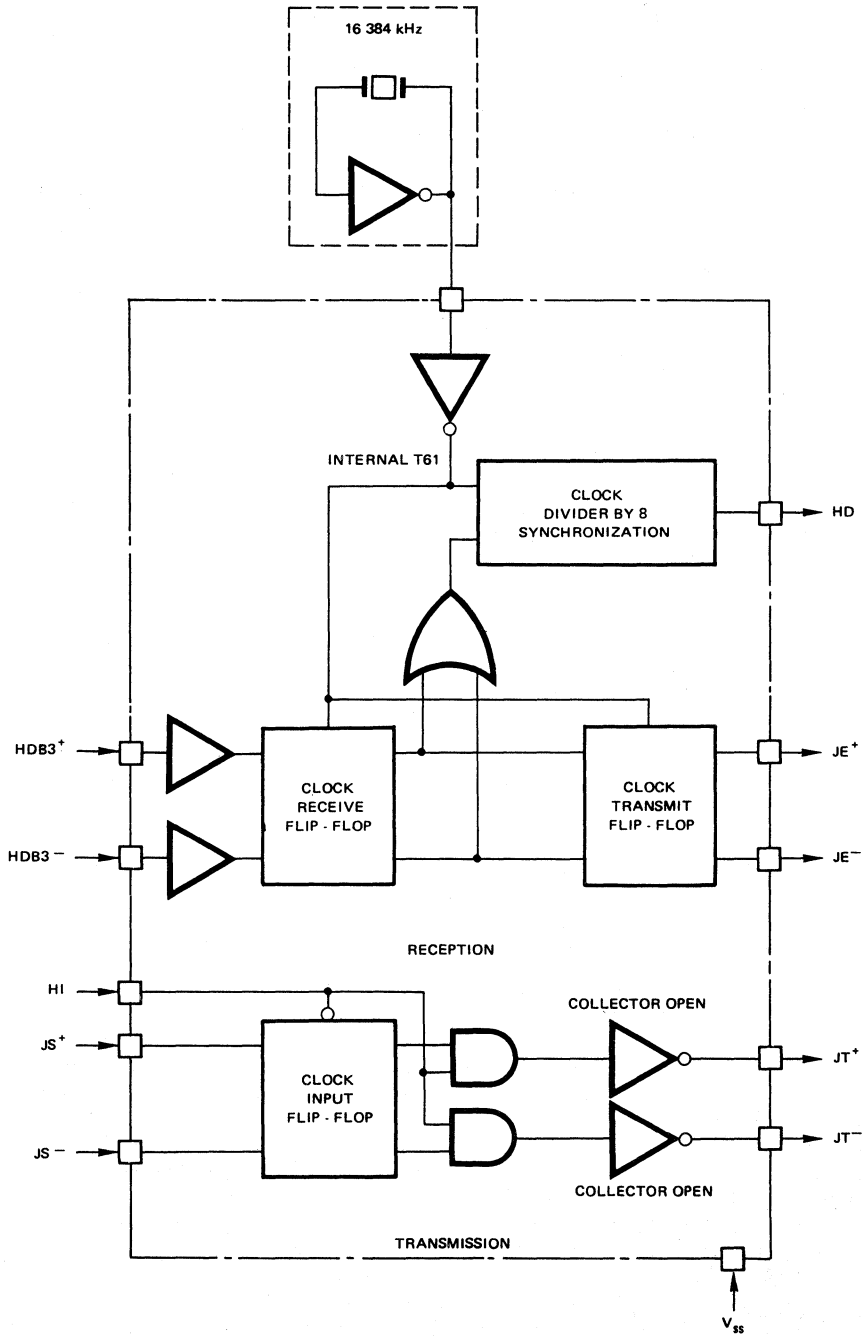


FIGURE 1 – MEH BLOCK DIAGRAM

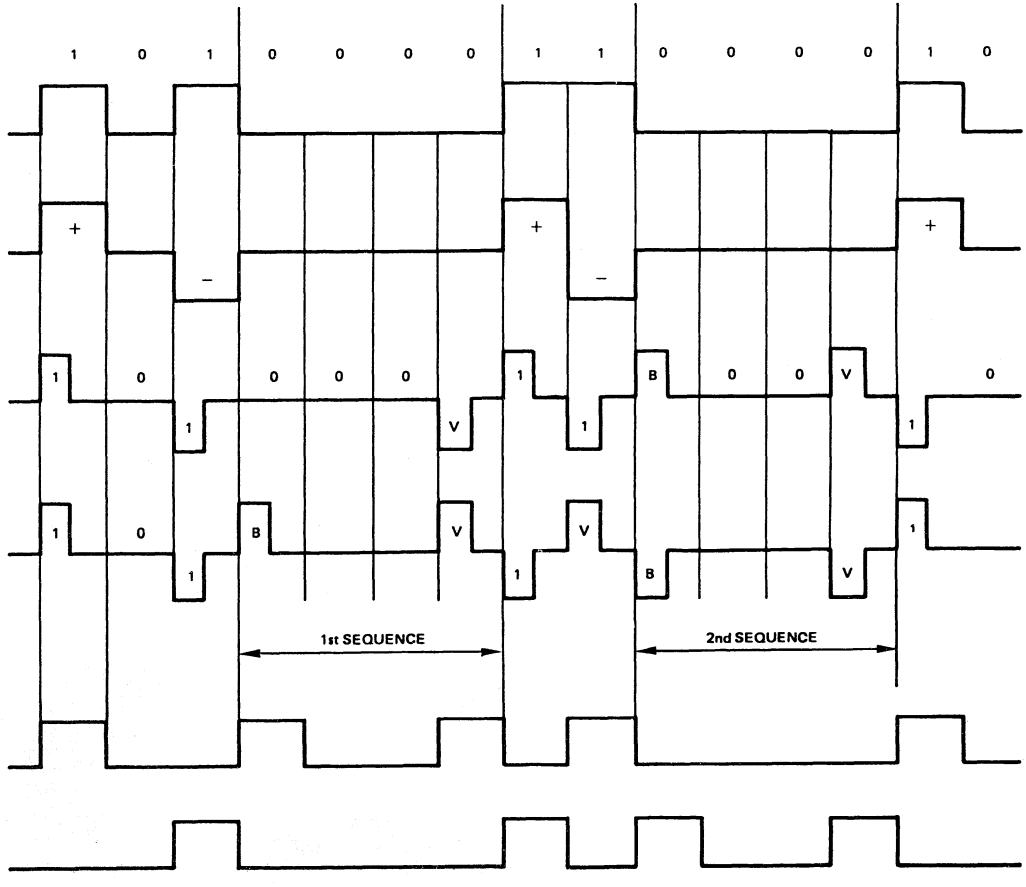


FIGURE 2 – 73321 RECEIVE CODES

1.3 Application No. 1: using circuit 73321 with free oscillator

The Quartz oscillator shown in figure 3 is of the stand-alone type, its precision is on the order of 50×10^{-6}, and its frequency in this application is 16,834 kHz.

It delivers several t 61 signals. Gates 74LS04 fan out is 8.

This oscillator can be constructed using HCMOS gates. The 6.8 k pull up resistors are thus suppressed. The in-line signal is a HDB3 coded signal with an attenuation of 6 dB max for a 3 V pulse delivered by a remote transmitter. Figure 6 shows the pulse for PCM CEPT junction.

Transmit and receive transformers are the same type. The transformation ratio between primary winding and the two secondary windings of the receive transformer is 3 : 2. The transmit transformer is of the step-down type (Fig 4.5).

Figure 4 shows an output transistor blocking device used in the event of a short-circuit on the line.

1.3.1 RECEIVE SECTION

The information delivered in the form JE+ and JE— at the output of the 73321 circuit receive side (which are the HDB3 signal rectified components) have a constant phase relationship with the recovered clock signal HD. The HD clock period will be:

$$8t +/- 2t$$

where t is the crystal-delivered signal period (61 ns for our example).

1.3.2 IN-LINE TRANSMISSION

The phase relationship of information JS+ and JS— with local clock HL should be constant at the transmission function input. The HL positive pulse width defines line pulse width.

There is no logical relationship between circuit 73321 transmit and receive sides.

In this application, transmission and reception are not synchronized.

The delay t1 caused at the input by the receive logic (between HDB3+ and JE+) is equal to 3t (if t = 61 ns, t1 = 183 ns).

The delay t2 caused at the output by the transmit logic (between JS+ and JT+) is 1.5 HL (if HL = 488 ns, t2 = 732 ns).

1.4 Application No. 2: using circuit 73321 with slaved oscillator

A buffer memory is used to overcome the differences in the information bit durations caused by the transmission and circuit 73321. The information will be written at HD rate and read at the rate of the local clock from the oscillator slaved by HD rate. The buffer memory capacity only depends from the jitter characteristics and the slaved oscillator correction speed. Figure 7 gives the block diagram of such a memory associated with circuit 73321. The functions represented are:

- HDB3/BIN code conversion,
- slaved Crystal oscillator,
- frequency dividers,
- buffer memory and its write/read control.

1.4.1 HDB3/BIN CONVERSION

This circuit is used to convert the two HDB3 components to one NRZ signal with the same jitter as the two original components. It makes also possible code conversion of a NRZ signal before amplification in circuit 73321 transmission section for application to the line.

1.4.2 CRYSTAL OSCILLATOR

The crystal oscillator frequency is 16,384 kHz. It delivers a time t61 in the form of a square signal with a 61 ns period driving the internal logic of circuit 73321 and the oscillator-associated frequency divider. A submultiple of the crystal frequency is slaved by a submultiple of the frequency received in line.

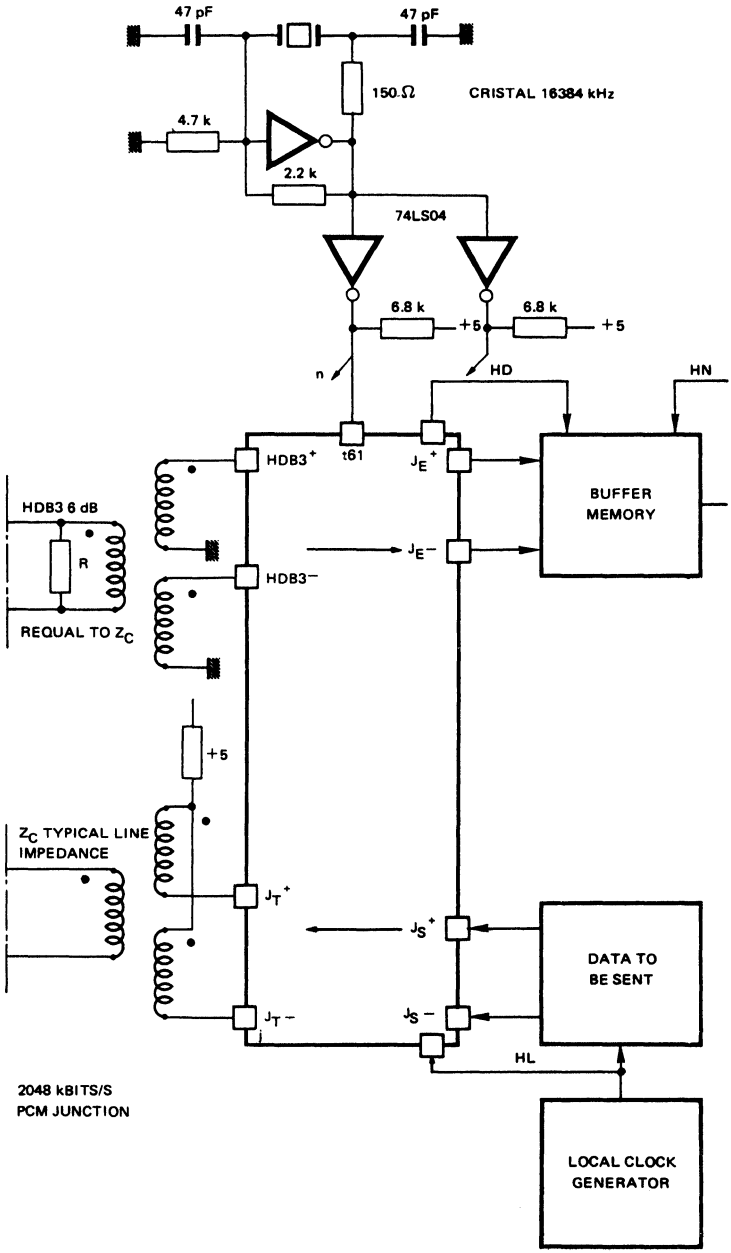


FIGURE 3 – APPLICATION N0 1 – USING FREE CRYSTAL OSCILLATION

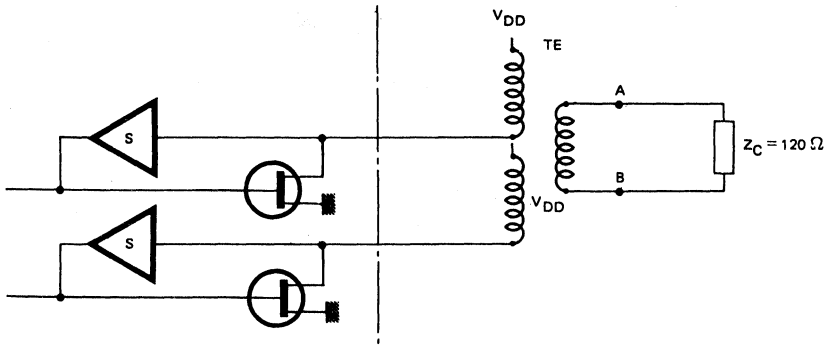


FIGURE 4 – MEH CIRCUIT BUILT-IN TRANSMIT AMPLIFIER

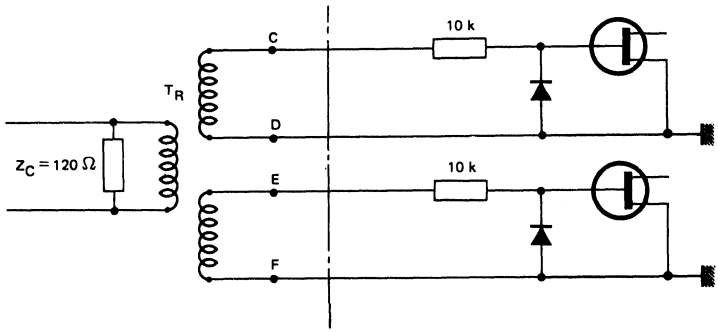


FIGURE 5 – MEH CIRCUIT BUILT-IN RECEIVE AMPLIFIER

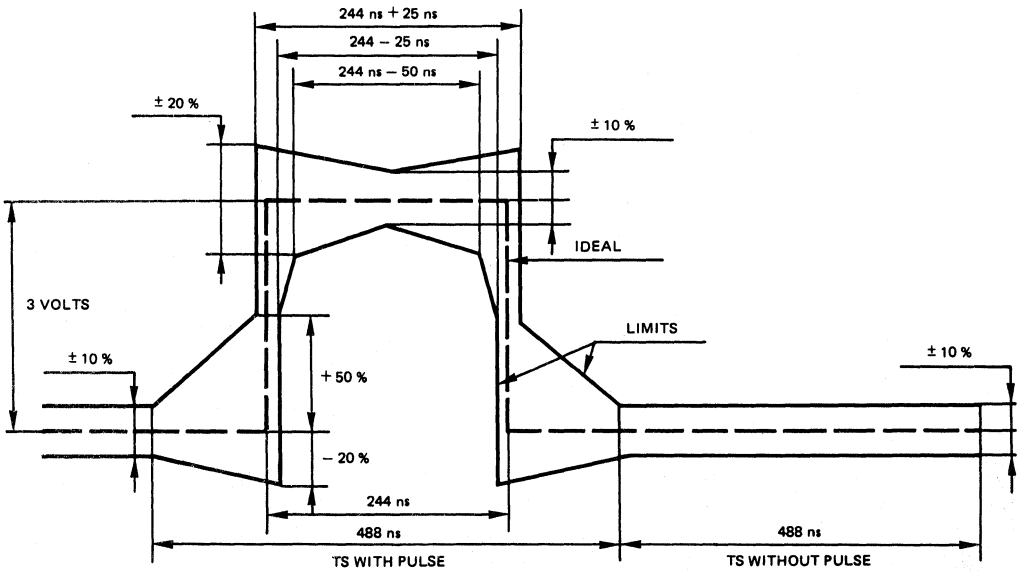


FIGURE 6 – PULSE SHAPE FOR 2048 BIT/S CEPT PCM JUNCTION

1.4.3 FREQUENCY DIVIDER ASSOCIATED WITH THE CRYSTAL

This is a counter in which each stage divides the input signal frequency by 2. The first 3 bits deliver time t1 (at 2,048 kHz) corresponding to time HD whose jitter amplitude was reduced by the extreme values taken by the slaved oscillator.

The following two bits A' and B' are used to select the buffer memory reading time (see timing diagram of figure 8). The n following bit should be chosen by the user to set the crystal oscillator correction frequency. If n = 6, the oscillator frequency will be corrected every 125 μs.

1.4.4 FREQUENCY DIVIDER ASSOCIATED WITH HD

The first two bits A and B define the reading time in the buffer memory. If HD shows no jitter, counters A' B' and A, B are in phase and reading takes places with a time delay of 2 bits after writing.

Note: If 3 bits (A, B and C) define the writing time and 3 bits the reading time, reading will take place with a time delay of 4 bit-durations compared to the writing time.

1.4.5 BUFFER MEMORY

This memory consists of a number of bistable circuits depending on the jitter to be recovered. In our example the 4 bistable circuits are used to recover a signal with a jitter of + / — 2 bits in amplitude without loosing information.

When the write counter A, B defines 2 as writing time, the read counter A' B' defines 0 as reading time and so on.

The maximum phase shift between the two counters A, B and A', B' is 2 bits in either direction without fault. Time t1 and data are the same residual jitter characteristic given by the slaved crystal oscillator selected.

1.4.6 TRANSMIT SECTION

In this application signal t1 can be used to sample the data to be transmitted (Fig. 7).

Residual jitter is small enough to drive BIN/HDB3 decoder logic and to calibrate line pulse width.

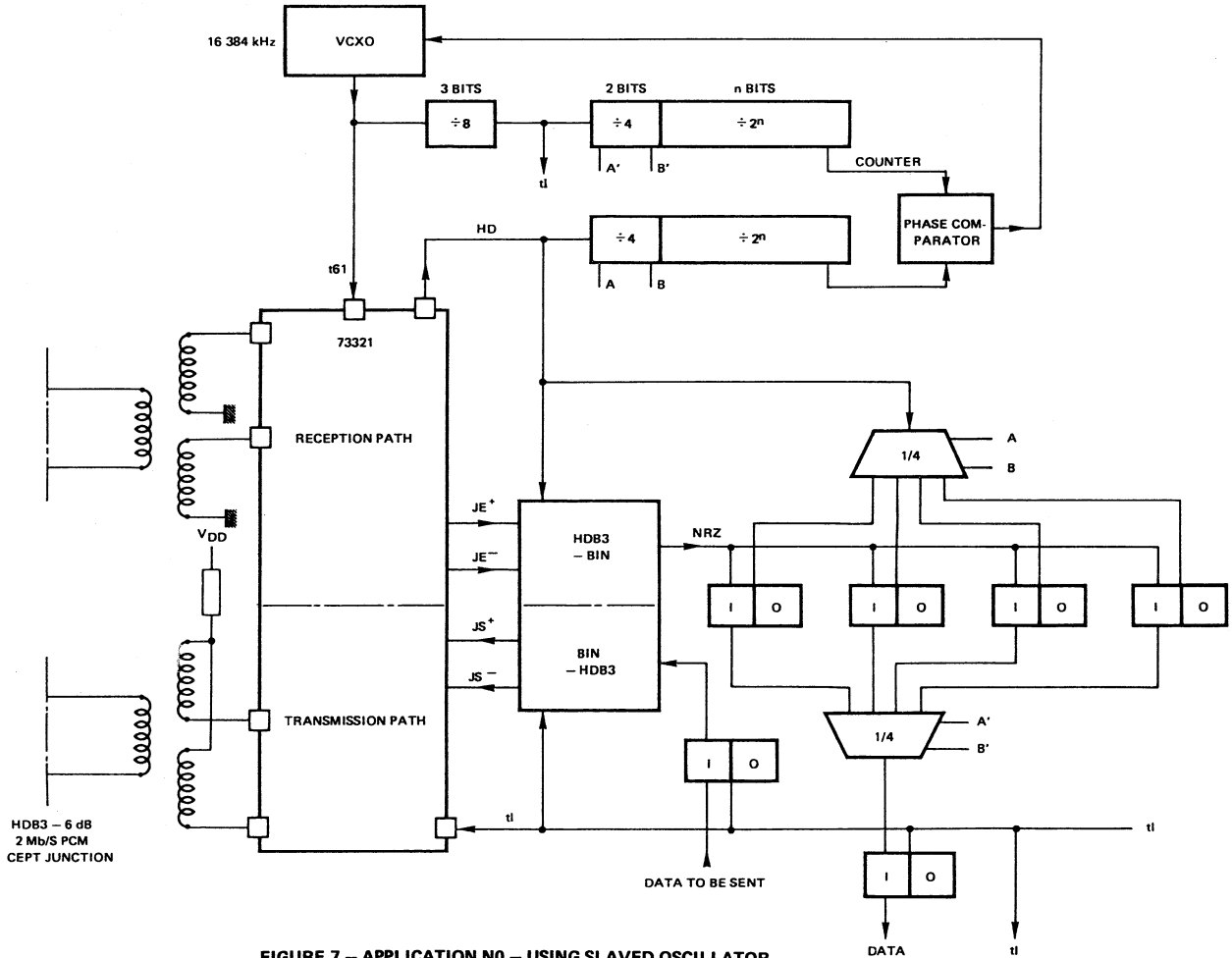


FIGURE 7 – APPLICATION N0 – USING SLAVED OSCILLATOR

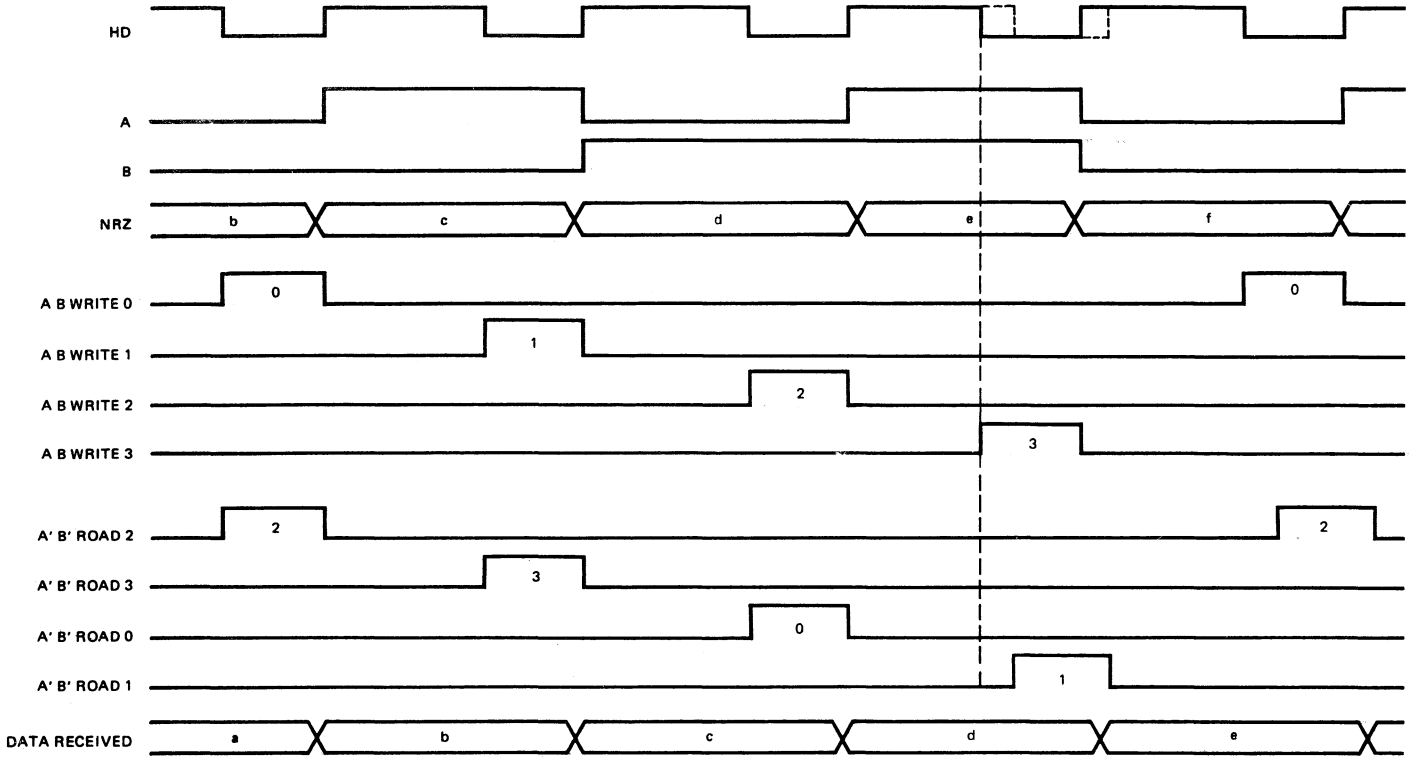


FIGURE 8 – APPLICATION TIMING DIAGRAM – 72321 WITH SLAVED OSCILLATOR

2 - TERMINAL SWITCHING MODULE (MTC) CIRCUIT 7333

2.1 Circuit description

The specifications of this circuit are given in the TELECOM ICS catalog by THOMSON-SEMICONDUCTEURS. It conforms to CCITT recommendation G737. In most applications it is connected between a clock extraction circuit of a MIC junction at 2.048 Mbits/s and multiplex switching circuits at 2.048 Mbits/s.

The 7333 circuit buffer memory function is twofold:

- frame synchronization of PCM junction input section with local clock,
- absorption of line jitter whose amplitude and frequency are given in circuit 7333 specifications.

The receive function provides a multiplex signal at 2.048 Mbit/s synchronized with local center clock (Fig. 9). The local center can be a connection network, a time concentrator, a computer interface, etc.

So, the PCM junctions from various centers in a plesiochronous network can be synchronized with the local center clock. Figure 10 shows that whatever the phase relationship between remote clocks td1, td21... tdn, circuit 7333 associated with a remote center can set in phase not only time slots but also incoming multiplex frames.

Special case

If remote centers are asynchronous, circuit 7333 synchronizes the multiplexes by skipping or doubling frames without loss of synchronization.

In this application, HDB3-BIN conversion is made in circuit 7333 (pin 9 to VSS). A pin (MQ) is provided for this purpose without using associated microprocessor. In this case the three alarms detected by the 7333 receive circuits:

- JDSY: junction desynchronized compared to CCITT algorithm,
- TE: error ratio too high compared to CCITT algorithm,
- MQX: clock missing (no Hd),

will be processed as follows:

They are considered as a logic OR whose value is transmitted in bit 3 of the odd frame time slot 0 by the 7333 transmit circuits.

When pin MQ is wired as "1" a microprocessor can access the six registers R1 to R6.

Register 1 contains the outgoing junction even frame TSO value. Only TSO bit 1 can be microprocessor-modified. The content of this register will be transmitted in line if the circuit is not operating on the looping mode.

Register 2 contains the outgoing junction odd frame TSO value. Only bit 2 cannot be microprocessor-modified, it remains 1. Bit 3 of register R2 can be either 1 or 0 as a result of a logic OR with the 3 alarms defined above (junction desynchronized, error ratio too high, HD clock missing). The content of register R2 will be transmitted in line only if the circuit is not operating on the looping mode.

Register R6 contains only one bit. It indicates whether a loop between outgoing and incoming HDB3 components is desired for test. In this case:

Register R3 (8 bits) will contain a value to be introduced into even frame TSO and **register 4** (8 bits) will contain a value to be introduced into odd frame TSO. The content of registers R3 and R4 is transmitted in line when the value of R6 (loop) = 1.

If R6 = 0 the contents of R1 and R2 are in line.

If R6 = 1 the contents of R3 and R4 are looped.

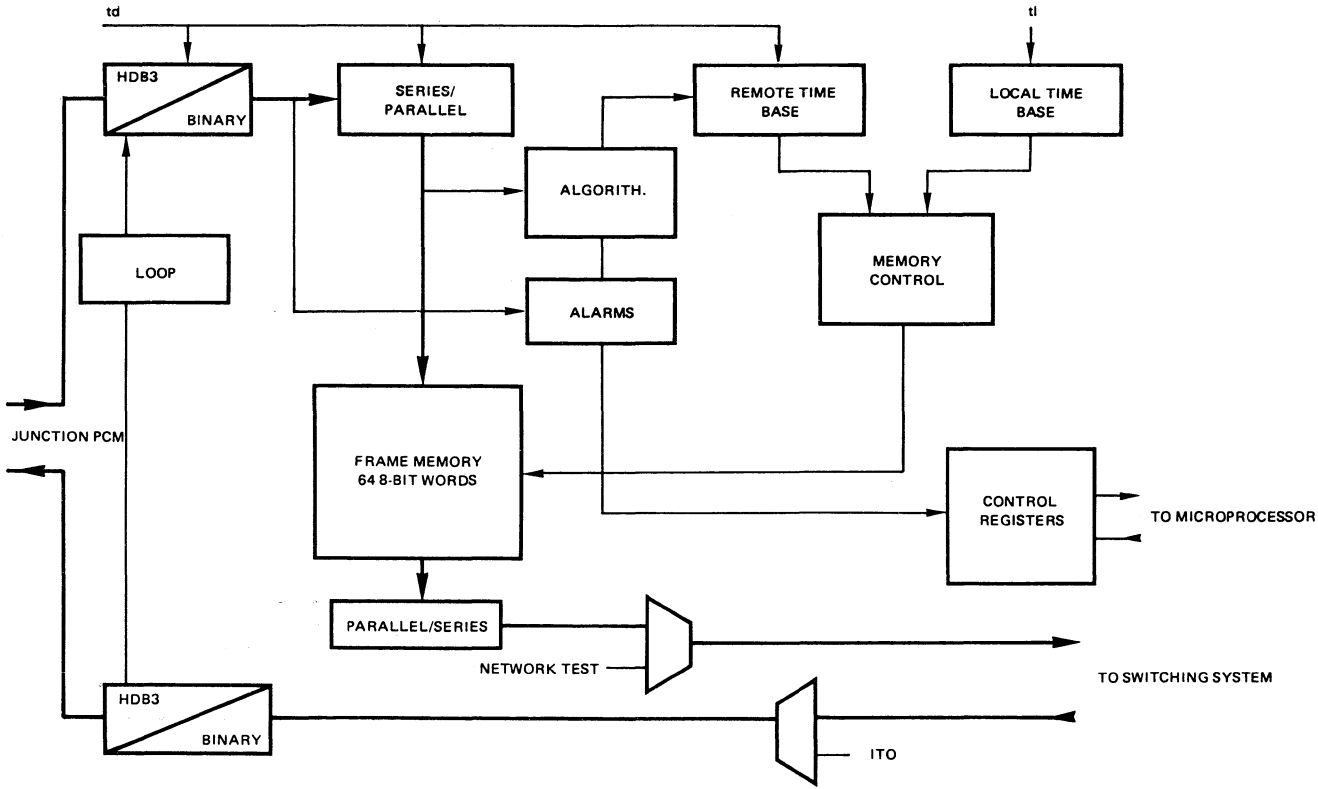


FIGURE 9 – SWITCHING TERMINAL MODULE

TSO \ R6	R6 = 0	R6 = 1
Out put JS + and JS —	Content of R1 and R2	Content of R3 and R4
Input Reception	Content of JE+ and JE—	Content of R3 and R4

Register R5 cannot be modified but only read by the microprocessor. It is managed by the 7333 circuit Receive function. The alarms detected are indicated in this register.

The value of bit 3 of incoming junction odd frame TSO is transferred in **bit 1 of register R5.** When the value of this bit is 1, this means that the remote end does not control the frame it receives any more (PVT: Perte de Verrouillage de Trame distante - Frame locking loss -).

Bit 2 of register R5 indicates that the 7333 sync device has found no frame locking code (PVT1: Perte de Verrouillage de Trame locale - Local frame locking loss -).

Bit 3 of register R5 indicates that time HD is missing (MQHX). In this application, this means that the crystal oscillator has stopped operating.

Bit 4 of register R5 indicates that the sync device is no more synchronized (JDSY).

Bit 5 of register R5 indicates the SIA value (SIA: Signal d'indication d'alarme distante-remote alarm indication signal). When JDSY = 0, the junction-is synchronized, SIA = 0; when JDSY = 1 (junction not synchronized), during two frames.

Bit 6 of register R5 indicates an excessive error ratio higher than 10^{-3} detected on the frame locking code.

Bit 8 SAUT indicates frame skip or doubling on reading frame memory (if phase relationship between remote end and local center is not defined: local and remote clock are plesiochronous).

Bit 7 of Register R5 indicates local clock lead (AV) or delay compared to remote clock.

If distant and local centers are synchronized by a common clock (not represented in figure 10) thus circuits 7333 resynchronize multiplex signals without loss of information accepting a peak-to-peak jitter of several TSs for very low jitter frequencies.

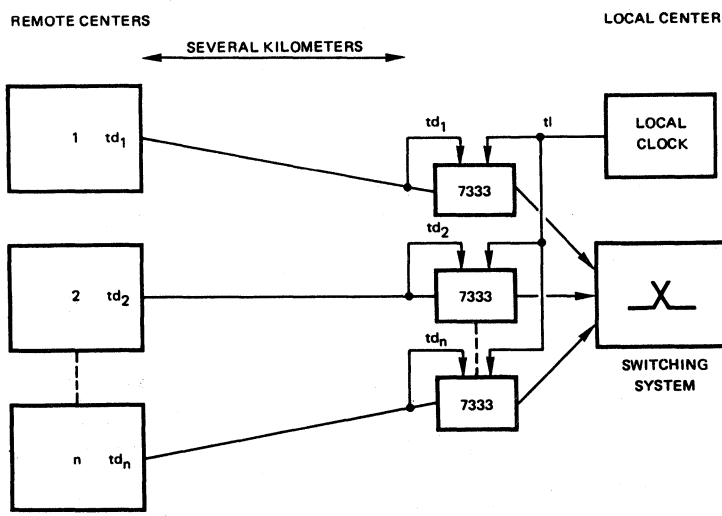


FIGURE 10 – PLESIOCHRONOUS NETWORK

2.2 Application No. 3: Binary inputs - Binary output

Figure 11 shows an environment where the 7333 incoming and outgoing data are binary. Pin 9 is used to select the incoming data code. In the receive mode a device external to circuit 7333 should deliver:

- the clock signal recovered from an amplifier that has reshaped the signal likely to have been attenuated during line propagation,
- the associated information which has been converted (from HDB3 to binary):

In the same way, in the transmission mode circuit 7333 receives a multiplex signal from the line, processes the 0 time slot content (IT0) in accordance with CCITT recommendations. A device external to the 7333 circuit receives the processed multiplex signal and can convert it from binary to HDB3 before transmitting it in line.

This application enables the user to select line reception and transmission amplifiers depending on transmission characteristics.

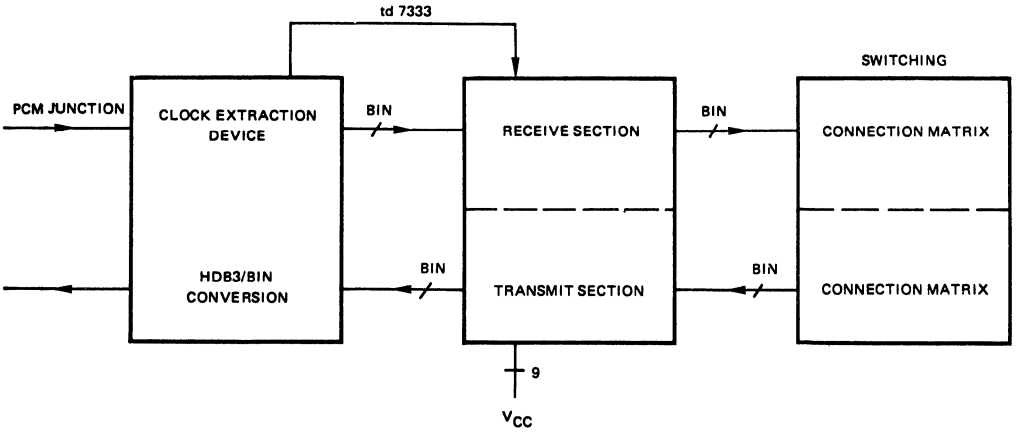


FIGURE 11 – BINARY INCOMING AND OUTGOING INFORMATION

2.3 Application No. 4: 73321-7333 association

The diagram in figure 12 shows the whole switching terminal function. No additional circuitry is required between circuits 73321 and 7333. They are designed for direct interface.

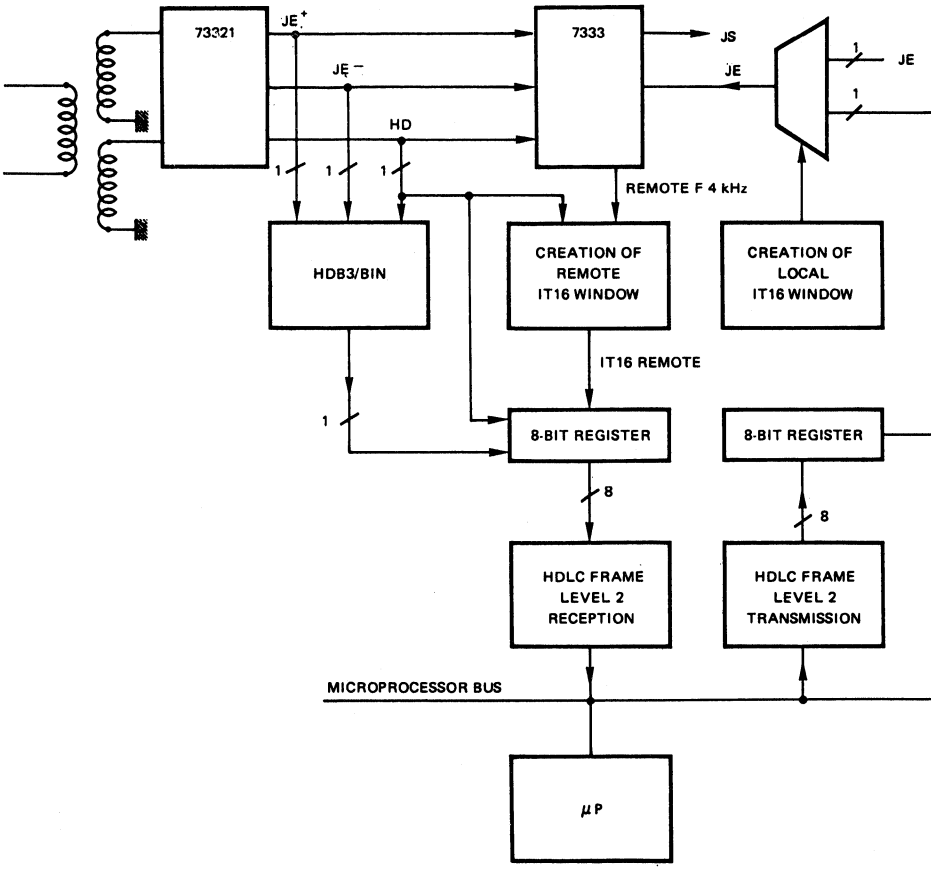


FIGURE 12 – REMOTE TS16 EXTRACTION

2.4 Application No 5: extraction of IT16 content without loss of information

We have seen that, when the remote device was asynchronous with the local 7333 there may be loss or repetition of information depending on the relative values of transmit and receive clocks.

For 64 kbit-speech channels, the users will not be aware of frame skips or doubling, but, for data channels, OSI system levels 2 (or 3) ensuring the exchange protocol between the two units will request repetition of the message. The following device avoids message repetition although the units are of the plesiochronous type.

Device description

One of the 7333 outputs labeled F4kHz (pin 15) delivers 4 kHz for the remote clock. The 7333 extracts the 4 kHz remote clock from the incoming junction in the same way as the 7332 extracts the Hd 2 MHz remote clock from the incoming junction.

It is possible to extract an TS content, for example TS16 content from incoming signals HD, JE+, JE— and from signal F 4 kHz (Fig. 12).

An 8-bit word is delivered to a series-parallel register by a HDB3 converter operating at HD clock rate. This word is selected by a device giving the time slot chosen, for example TS16. At the end of TS16 the register content is loaded into a parallel-parallel register; a microprocessor can read this word after an interrupt for example. In the transmit mode, the microprocessor of figure 12 delivers a HDLC frame that can be inserted in TS16 of circuit 7333 local multiplex JE (transmit side).

Position of signal F 4 kHz with respect to:

J+, J—, $\overline{HD}$

The 7333 internal logic works on HD falling edge (receive side). Figure 13 shows the 250 μs period F4kHz signal with respect to:

- recovered remote clock (pin 12),
- JE+, JE—,

the 4 kHz signal switches to another state on $\overline{HD}$ falling edge when bit 5 of IT0 arrives on $\overline{JE}$ —, $\overline{JE}$+ (pins 7 and 8).

The delay (tpd) compared to $\overline{HD}$ falling edge is 250 ns max for a 50 pF load.

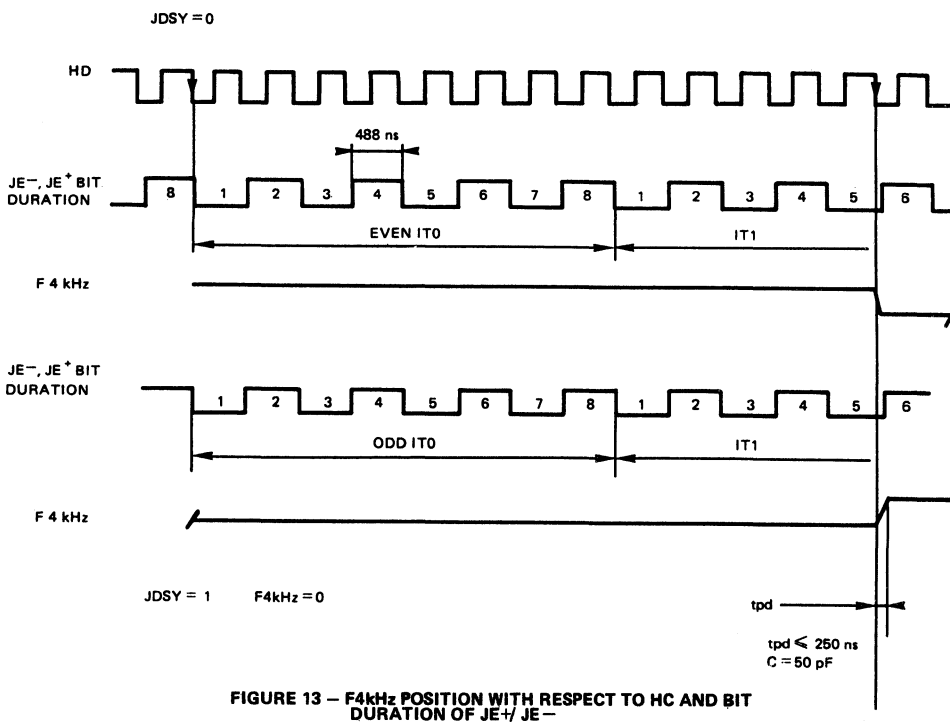


FIGURE 13 – F4kHz POSITION WITH RESPECT TO HC AND BIT DURATION OF JE+/ JE—

CHAPTER 5 - TELEPHONE SET ICs

COMPARISON OF THOMSON-MOSTEK TONEPULSE™ DIALERS

Feature/Parameter	MK5370	MK5371	MK53721	MK53731	MK5375	MK5376	MK53761	MK53762	MK53763
1. Memory/ No. of Digits	Redial/ 28	Redial/ 28	Redial/ 28	Redial/ 28	10 no./ 16 ea.	10 no./ 16 ea	10 no./ 18 ea.	10 no./ 18 ea.	13 no./ 18 ea.
2. Key(s) Used For Redialing	* or #	LND key	LND key	LND key	*, 0-9	*, 0-9 or Control 0-9	Mem, 0-9 and LND	Single Keys Mem 1 - Mem 9 and LND	Single Keys Mem 1 - Mem 9 E1 - E3 & LND
3. Pulse/Tone Switchable	Manual	Manual or Softswitch	Manual or Softswitch	Manual or Softswitch	Manual	Manual	Manual or Softswitch	Manual or Softswitch	Manual or Softswitch
4. Pacifier Tone	Yes	Yes	No	Yes	Yes	Yes	Yes	Yes	Yes
5. BCD Interface	No	Yes	No	No	No	No	No	No	No
6. 10/20 PPS Select	No	No	Yes	No	RC variable	RC variable	No	No	Yes
7. M/B Ratio Select	No	No	Yes	No	No	Yes	No	No	Yes
8. Continuous Tone	No	No	Yes	Yes	No	No	Yes	Yes	Yes
9. Single Tones	No	No	Yes	Yes	No	No	Yes	Yes	Yes
10. Timed Hookflash	No	600 ms	Selectable	560 ms	No	No	560 ms	560 ms	Selectable
11. PABX Pause	No	Yes	Yes	Yes	Yes	Yes	No	Yes	Yes
12. Dialing Rate Tone - Pulse -	Fixed 5 TPS 10 PPS	Fixed 5 TPS 10 PPS	Selectable 5-6 TPS 10/20 PPS	Fixed 8 TPS 10 PPS	RC Variable 5 TPS typ 10 PPS typ	RC Variable 5 TPS typ 10 PPS typ	Fixed 8 TPS 10 PPS	Fixed 8 TPS 10 PPS	Selectable 5-6 TPS 10/20 PPS
13. Voltage (Tone) (Pulse)	2.5-6.0 V 2.5-6.0 V	2.5-6.0 V 2.5-6.0 V	2.5-6.0 V 1.8-6.0 V	2.5-6.0 V 1.8-6.0 V	2.5-6.0 V 2.5-6.0 V	2.5-6.0 V 2.5-6.0 V	2.5-6.0 V 1.8-6.0 V	2.5-6.0 V 1.8-6.0 V	2.5-6.0 V 1.8-6.0 V
14. Package Size	18 pin	18 pin	20 pin	18 pin	18 pin	24 pin	18 pin	20 pin	24 pin

GLOSSARY

1. Control - To allow normal dialing of * and #, the MK5376 may use a separate Control Key for autodialing.
2. Mem - The MK53761, 53762, 53763 use separate Mem and PROG keys to store and autodial from memories 0 to 9. The MK53763 also uses keys E1 - E3 to autodial 3 emergency numbers.
3. LND - Last Number Dialed; a separate redial key on the MK5371, MK53721, MK53731, MK53761, MK53762, and MK53763.
6. RC - Resistor Capacitor; timing elements used to determine the dialing rate on the MK5375/6. So by varying the RC values, the MK5375/6 may dial at rates from 5 to 10 TPS and 10 to 20 PPS.
7. Softswitch - Keyboard entry (storable in memory) to switch signalling modes.
8. Continuous Tone - The selected DTMF tone will be output for the duration of the key closure. The MK53721, 53731, 53761, 53762 and MK53763 feature this as well as a guaranteed minimum output dura-

THOMSON COMPONENTS
MOSTEK

MK5375N

TEN-NUMBER REPERTORY
TONE/PULSE DIALER

COMMUNICATIONS PRODUCTS

FEATURES

- ☐ CMOS Technology provides low-voltage operation
- ☐ Converts push-button inputs to both DTMF and loop-disconnect signals
- ☐ Stores ten 16-digit telephone numbers, including last number dialed
- ☐ Pacifier tone and PBX pause
- ☐ Last-number-dialed (LND) privacy
- ☐ Manual and auto-dialed digits may be cascaded
- ☐ Ability to store and dial both "*" and "#" DTMF signals
- ☐ Variable dialing rate
- ☐ On-chip power-up-clear guarantees data integrity

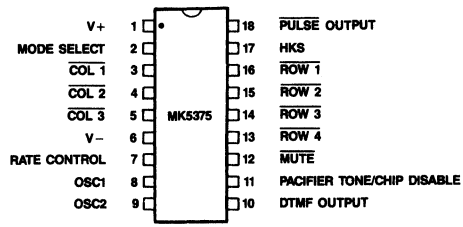


Figure 1. Pin Connections

DESCRIPTION

The MK5375 is a monolithic, integrated circuit manufactured using Mostek's proprietary Silicon Gate CMOS process. This circuit provides the necessary signals for either DTMF or loop disconnect dialing. It also allows for the storage of ten telephone numbers, including as many as 16 digits each, in on-chip memory.

The MK5375 accepts rapid keypad inputs (up to 25 key entries per second) and buffers these inputs in the FIFO (First-In-First-Out) LND (Last-Number-Dialed) register. Each digit entry is accompanied by a pacifier tone, which is activated after the digit has been debounced, decoded, and properly stored. Signaling occurs at a rate determined by externally connected components, allowing the dialing rate to be adjusted for any system.

The flexibility of the dialer makes possible a variety of applications, such as "scratchpad" number storage. In "scratchpad" applications, the MK5375 inhibits signaling during entry, without interrupting a conversation.

Privacy is also an important feature. The MK5375 allows the LND (Last-Number-Dialed) buffer to be cleared following a call, without affecting data stored in other permanent memory locations. The memory in the permanent locations may be easily protected from inadvertent key entries with the addition of a simple "memory lock" switch to the application.

All of these options plus additional features are discussed in more detail in the following sections. The first section contains a brief detailed description of each pin function. The second section describes the device operation. This is followed by the DC and AC Electrical Specifications, and a few application suggestions.

FUNCTIONAL PIN DESCRIPTION

V+
(Pin 1)

Pin 1 is the positive supply for the circuit and must meet the maximum and minimum voltage requirements as stated in the electrical specifications.

MODE SELECT
(Pin 2)

In normal operations, Pin 2 determines the signaling mode used; a logic level 1 (V+) selects Tone Mode operation, while a logic level 0 (V–) selects Pulse Mode operation. This input must be tied to one of the supplies to guarantee proper dialing.

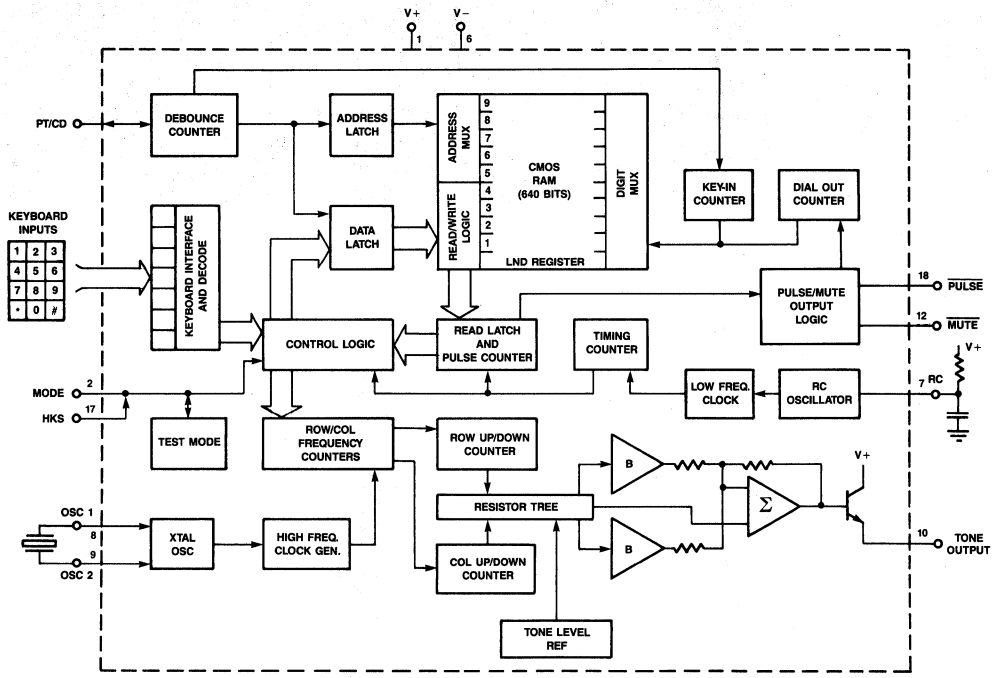


Figure 2. MK5375 Functional Block Diagram

KEYBOARD INPUT: $\overline{COL1}$, $\overline{COL2}$, $\overline{COL3}$, $\overline{ROW4}$, $\overline{ROW3}$, $\overline{ROW2}$, $\overline{ROW1}$ (Pins 3,4,5,13,14,15,16)

The MK5375 keypad interface allows either the standard 2-of-7 keyboard with negative common or the inexpensive single-contact (FORM-A) keyboard to be used (Figure 3). A valid key entry is defined by either a single Row being connected to a single Column or by V− being presented to both a single Row and Column. In standby mode either all the rows will be a logic 1 (V+) and all the columns will be a logic 0 (V−), or vice versa.

The keyboard interface logic detects when an input is pulled low and enables the RC (Rate Control) oscillator and keypad scan. Scanning consists of alternately strobing the rows and columns high through on-chip pullups. After both valid row and column key closures have been detected, the debounce counter is enabled. Breaks in contact continuity (bouncing contacts, etc.) are ignored for a debounce period (T_{db}) of 32 ms. At this time the keypad is sampled, and if both row and column information is valid, this information is buffered into the LND location.

RATE CONTROL (Pin 7)

The Rate Control input is a single-pin RC oscillator. An external resistor and capacitor determine the rate at which signaling occurs in both Tone and Pulse modes. An 8 kHz oscillation provides the nominal signaling rates of 10 PPS (Pulses per second) in Pulse Mode and 5 TPS (Tones per second) in Tone Mode; the Tone duty cycle is 98 ms on, 102 ms off. The RC values on this input can be adjusted to a maximum oscillation frequency of 16 kHz resulting in an effective Pulse rate of 20 PPS and a Tone rate of 10 TPS.

The frequency of oscillation is approximated by the following equation:

$$Fosc = 1/(1.49RC). \quad (1.0)$$

The value suggested for the capacitor (C) should be a maximum of 410 pF to guarantee the accuracy of the oscillator. The resistor is then selected for the desired signaling rate. Nominal frequency (8 kHz) is achieved with component values of 390 pF and 220 kohms. Parasitics must be taken into account.

OSCIN, OSCOUT
(Pins 8,9)

Pins 8 and 9 are the input and output, respectively, of an on-chip inverter with sufficient loop gain to oscillate when used in conjunction with a low-cost television color-burst crystal. The nominal crystal frequency is 3.579545 MHz, and any deviaton from this standard is directly reflected in the Tone Output frequencies.

This oscillator is under direct control of the repertory dialer and is enabled only when a tone signal is to be transmitted. During all other times it remains off, and the input has high impedance. The input OSCIN may be driven by an external source.

DTMF OUTPUT
(Pin 10)

The DTMF Output pin is connected internally to the emitter of an NPN transistor, which has its collector tied to V+, as shown on the functional block diagram (Figure 2). The base of this transistor is the output of an on-chip operational amplifier that mixes the Row and Column Tones together.

The level of the DTMF Output is the sum of a single row frequency and a single column frequency. A typical single-tone sine wave is shown in Figure 4. This waveform is synthesized using a resistor tree with sinusoidally weighted taps.

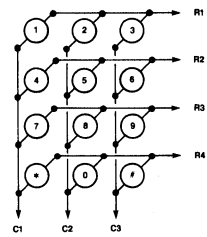
The tone level of the MK5375 is a function of the supply voltage. The voltage to the device may be regulated to achieve the desired tone level, which is related to the supply by either of the following equations:

$$T(O) = 20 \text{ LOG } [(0.078V+)/0.775] \text{ dBm.} \quad (2.0)$$
$$T(O) = 0.078(V+) \text{ VRMS. (Row tones)} \quad (2.1)$$

PACIFIER TONE OUTPUT / CHIP DISABLE
(Pin 11)

This pin normally has high impedance. Upon acceptance of a valid key input, and after the 32 ms debounce time, a 500 Hz square-wave will be output on this pin. The square-wave terminates after a maximum of 30 ms or when the valid key is no longer present. The purpose of this pacifier tone is to provide to the user audible feedback that a valid key has been entered. This feature is useful particularly for on-hook storage and pulse-mode signaling.

3A. Calculator-Type Keypad



3B. Standard Telephone-Type Keypad

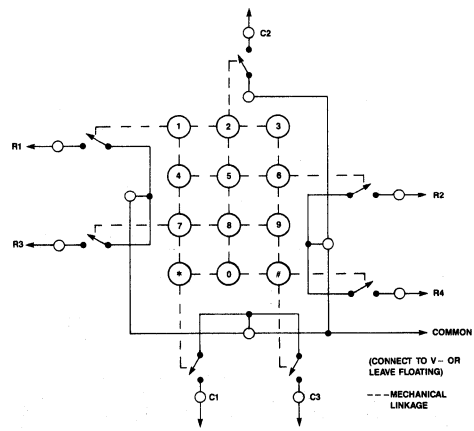


Figure 3. Keypad Schematics

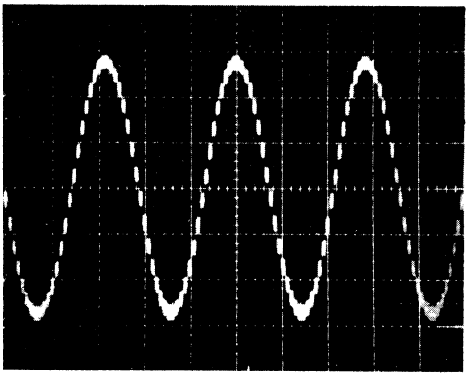


Figure 4A. Typical Sine Wave Output - Single Tone

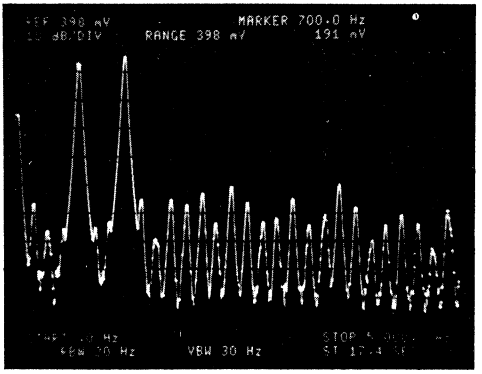


Figure 4C. Spectral Analysis of Waveform in Fig. 7 (Vert-10 dB/div. Horizontal - 600 Hz/div.)

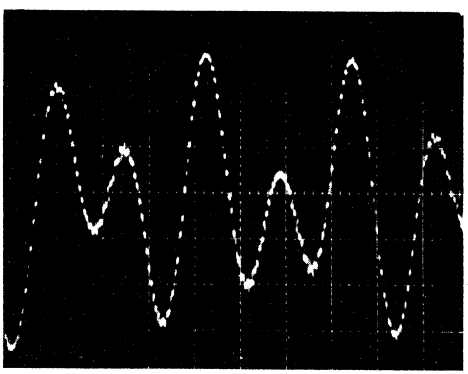


Figure 4B. Typical Dual-Tone Waveform (Row 1, Col 1)

Table 1. Output Frequency

KEY INPUT	STANDARD FREQUENCY	ACTUAL FREQUENCY	% DEVIATION
ROW 1	697	699.1	+0.31
2	770	766.2	−0.49
3	852	847.4	−0.54
4	941	948.0	+0.74
COL 1	1209	1215.9	+0.57
2	1336	1331.7	−0.32
3	1477	1471.9	−0.35

The pacifier tone is not enabled when manually dialing in tone mode. This eliminates any confusion between the audible DTMF feedback and the pacifier tone, and prevents distortion of the DTMF signal by any of the pacifier tone frequency components. In both cases, the tone confirms that the key has been properly entered and accepted; whereas, without the tone, the user will not know if the keys have been properly entered.

IMPORTANT: This pin also serves as a chip-disable pin. Pulling this input high through a resistor will disable the keypad (high impedance) and initialize all counters and flip-flops (memory remains undisturbed). Pulling the input low through the same resistor enables the circuit. For the device to function properly, the resistor to V– (Pin 6) is required.

This feature is useful in several applications, as described in the application notes section.

MUTE OUTPUT
(Pin 12)

This pin is the Mute output for both Tone and Pulse modes of operation. The timing is dependent upon which mode is being used. The output consists of an open-drain, N-channel device. During standby, the output has high impedance and generally requires an external pullup resistor to the positive supply.

In Tone Mode, the Mute output is used to remove the transmitter and the receiver from the network during DTMF signaling. The output will mute continuously while auto-dialing and during manual DTMF signaling until each digit entered has been signaled.

In Pulse Mode of operation, the Mute output is used to remove the receiver or even the entire network from the line. These timing relationships are shown in Figure 5.

HKS INPUT
(Pin 17)

This pin is a high-impedance input and must be switched high for on-hook operation or low for off-hook operation. A transition on this input will cause the on-chip logic to initialize, terminating any operation in progress at the time. Signaling is inhibited while on-hook, but key inputs will be accepted and stored in the LND register. The information stored in the LND register may be copied into an alternate location only while on-hook. A logic level may be presented to this input, independent of the position of the hook-switch, allowing on-hook operations, such as storage, to be performed off-hook.

PULSE
(Pin 18)

This is an output driven by an open-drain, N-channel device. In Pulse Mode operation, the timing at this output meets Bell Telephone and EIA specifications for loop-disconnect signaling. The Make/Brake ratio is set to 40/60 on the standard MK5375. The pulse rate is determined by the RC values selected for the Rate Control, Pin 7. Note: The standard make/break ratio may not be suitable if the Pulse dialing rate is accelerated.

DEVICE OPERATION

The MK5375 can be used in low-priced phones with basic 3×4 matrix keypads. The block diagram in Figure 2 shows the data and control signal flow between the various functional blocks. The keypad entries are decoded, debounced, and if valid, they are stored into the LND (Last-Number-Dialed) buffer, which acts much like a FIFO (First-In-First-Out) register. Each subsequent entry is stacked in the buffer. Typically, the dialing sequence begins 172 ms after the first digit is accepted in Pulse Mode operation and 132 ms in Tone Mode operation. Each digit buffered into the RAM is dialed out with a 98 ms burst of DTMF and an inter-signal time of 102 ms.

Buffering the data into the RAM prior to signaling is an important feature of the repertory dialer. It allows for the use of less expensive keypads, since the user cannot enter the digits too quickly for the system, and the pacifier tone can be used to provide audible feedback following each key entry not generating a DTMF signal. It also guarantees that the data stored in the RAM matches exactly the digits actually dialed.

Manual dialing and auto-dialing can be executed in any order, consecutively or cascaded. The dialer must complete auto-dialing the previous entry before another key is entered. Digits should not be entered while the device is auto-dialing. Most digits would be ignored unless preceded by a control key; in which case, an error in dialing may occur.

1	2	3
4	5	6
7	8	9
*	0	#

STORE DIAL LND PAUSE

Figure 6. Keypad Configuration

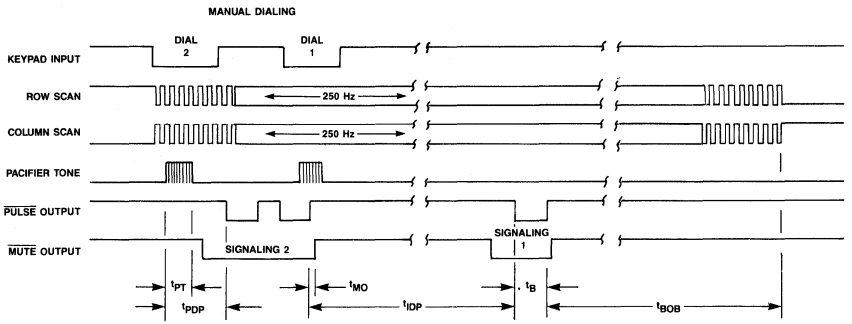


Figure 5A. MK5375 Timing Diagram — Pulse Mode Off-Hook Operation

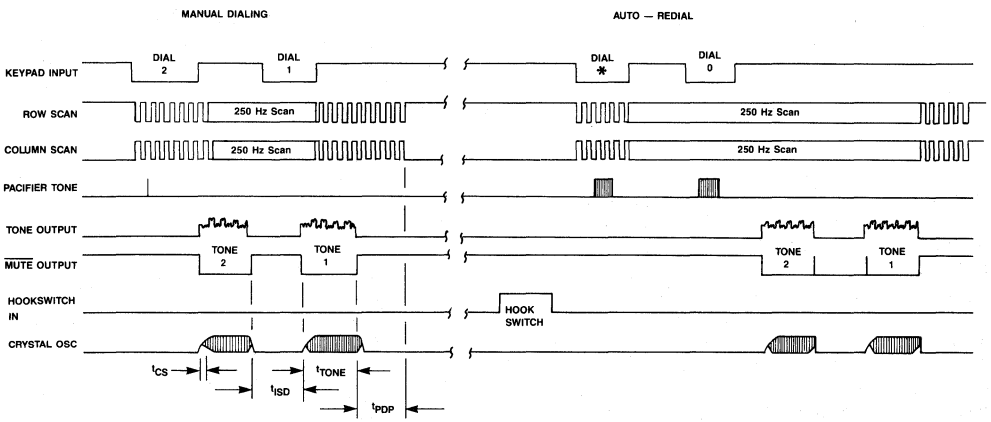
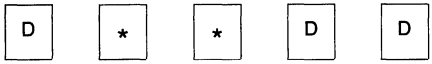


Figure 5B. MK5375 Timing Diagram — Tone Mode

NORMAL DIALING

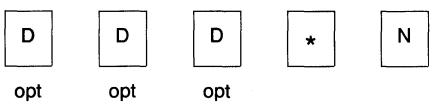


The "*" (STAR) key is used as the modifier to control repertory functions. All numeric keys will signal normally unless preceded by a modifier. To signal either a "*" or "#", these keys must be entered twice in succession. The first entry is not signaled or stored.

LND PRIVACY

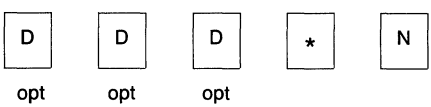
A single "*" input prior to going on-hook or prior to coming off-hook will erase the information stored in the LND buffer.

AUTO DIALING (Off-Hook)



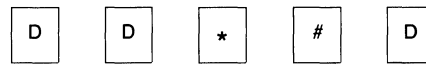
The key sequence "*", followed by any digit, will autodial the number sequence stored in the designated address location while off-hook.

STORAGE (On-Hook)



D is any data (telephone numbers) being entered or dialed. N is the address (memory location) in which numbers are stored. The number sequence stored in the LND buffer can be transferred to one of the other nine permanent locations with the simple sequence "*" followed by the address. New digits may be written into the LND buffer while on-hook. To enter either a "*" or "#" signal the digit must be entered twice in succession.

PABX PAUSE (Off-Hook and On-Hook)



An indefinite pause is stored in a number sequence by entering the "*" key modifier, followed by a "#" key input. When the number sequence is redialed, the dialer will pause when it encounters the "#" entry. A key input will cause it to continue.

PULSE DIALING

Most of the Pulse key operations are the same as they were in Tone Mode; PABX Pause is the only exception. In Pulse Mode, the pause may be stored as in tone mode, "* #", or with a single "#" input. Two "#" inputs will store two pauses.

The "*" key exercises the control function; two "*" inputs will be the same as a single input (multiple inputs are not accepted.)

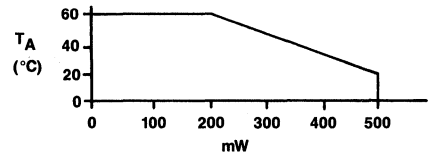
ABSOLUTE MAXIMUM RATINGS*

DC Supply Voltage V+ . . . . . 6.5 Volts
Operating Temperature . . . . . −30°C to +60°C
Storage Temperature . . . . . −55°C to +85°C
Maximum Power Dissipation (25°C) . . . . . 500 mW
Maximum Voltage on any Pin . . . . . (V+) + 0.3; (V−) − 0.3 Volts

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

POWER DISSIPATION DERATING CURVE



DERATE AT 9 mW/°C WHEN SOLDERED INTO PC BOARD.

ELECTRICAL SPECIFICATIONS

DC CHARACTERISTICS

$-30°C \leq T_A \leq 60°C$

SYM	CHARACTERISTIC	MIN	TYP	MAX	UNIT	NOTES
V+	DC Operating Voltage	2.5		6.0	V	
I_{SB}	Standby Current		0.3	.75	μA	1
V_{MR}	Memory Retention Voltage	1.5	1.3		V	2
I_{MR}	Memory Retention Current	750	200		nA	2
I_T	Operating Current (Tone)		0.5	1.0	mA	3
I_P	Operating Current (Pulse)		50	150	μA	3
I_{ML}	Mute Output Sink Current	1.0	3.0		mA	4
I_{PL}	Pulse Output Sink Current	1.0	3.0		mA	4
I_{PC}	Pacifier Tone Sink/Source	250	500		μA	5
K_{RU}	Keypad Pullup Resistance		100		kOHMS	
K_{RD}	Keypad Pulldown Resistance		500		OHMS	

NOTES:

(All specifications are for 2.5 volt operation, unless otherwise stated. Typical values are representative values at room temperature and are not tested or guaranteed parameters.)

1. All inputs unloaded, Quiescent Mode (Oscillator off)
2. Meeting these minimum supply requirements will guarantee the rentention of data stored in memory.
3. All outputs unloaded, single key input
4. V_{OUT}=0.5 Volts
5. Sink current for V_{OUT}=0.5; source current for V_{OUT}=2.0 VOLTS

AC CHARACTERISTICS -- KEYPAD INPUTS, PACIFIER TONE

SYM	CHARACTERISTIC	MIN	TYP	MAX	UNIT	NOTES
T_{KD}	Keypad Debounce Time		32		mSEC	1
F_{KS}	Keypad Scan Frequency		250		Hz	1
T_{RL}	Two Key Rollover Time		4		mSEC	1
F_{PT}	Frequency Pacifier Tone		500		Hz	1
T_{PT}	Pacifier Tone		30		mSEC	1
F_{RC}	Frequency RC Oscillator	−7.0	±2.5	+7.0	%	2

NOTES:

1. Times based upon 8 kHz RC input for Rate Control
2. Deviation of oscillator frequency takes into account all voltage (2.5 to 6.0 volts), temperature (−30° to +60°C), and unit-to-unit variations. The tolerance of the external RC components or parasitic capacitance is not included.

AC CHARACTERISTICS -- TONE MODE

SYM	CHARACTERISTIC	MIN	TYP	MAX	UNIT	NOTES
T_{NK}	Tone Output No Key Down			−80	dBm	1
T_O	Tone Output (Row Tones)	−13 173	−12 194	−11 218	dBm mV (RMS)	1
PE	Pre-emphasis, High Band	2.2	2.7	3.2	dB	1
V_{DC}	Average DC Bias Tone Out		1.7		VOLTS	
DIS	Output Distortion		5.0	8.0	%	1
TR	Tone Signaling Rate		5	10	1/SEC	2
PSD	Pre-signal Delay		132		mSEC	2
ISD	Inter-signal Delay		100		mSEC	2

NOTES:
1. Load=10 kΩ
2. These values are directly related to the RC input to Pin 7, nominally 8 kHz.

AC CHARACTERISTICS -- PULSE MODE OPERATION

SYM	CHARACTERISTIC	MIN	TYP	MAX	UNIT	NOTES
P_R	Pulse Rate		10		PPS	1
PDP	Predigital Pause		172		mSEC	1
IDP	Interdigital Pause		940		mSEC	1
T_{MO}	Mute Overlap Time		2		mSEC	1

NOTES:
1. Typical times assume nominal RC input frequency of 8 kHz. An increase in frequency results in an equal decrease in time values and an equal increase in rate values.

APPLICATION CIRCUIT

The MK5375 integrated circuit provides the ability to convert keypad inputs into either DTMF or loop-disconnect signals compatible with most telephone systems. Both modes of signaling utilize loop currents to transmit the desired signaling information to the central office.

The circuit schematic in Figure 7 illustrates a typical implementation of the MK5375 dialer IC along with the necessary components required to interface with the telephone line in a tone/pulse application.

In loop-disconnect signaling, each digit dialed consists of a series of momentary interruptions of loop current called "breaks" (i.e., a digit "1" consists of a single break, a digit "2" consists of two breaks, and so on. The Pulse output is dedicated to loop-disconnect signaling and controls the flow of loop current through the speech network switching transistors, Q4 and Q5. The Mute output, through transistors Q2 and Q3, removes the receiver and transmitter to eliminate loud pops in the receiver caused by switching current through the network. The Pulse and Mute output signals, as shown in Figure 5A, consist of make, break, and interdigital time intervals.

DTMF signaling requires that the loop current be modulated, producing an analog signal on the telephone line. Transistor Q1 modulates the loop current by amplifying the DTMF signal coupled to its base from the Tone Output. The Mute output removes the receiver and transmitter by switching transistors Q2 and Q3. This eliminates any interference with the DTMF signal from the transmitter and cuts down on the amplitude of the DTMF tone heard at the receiver. The timing diagram in Figure 5B illustrates the time relationship between key entries, Tone Output, and -Mute- Output.

The voltage regulator circuit comprising resistor R2, zener diode Z2, and transistor Q6 serves several purposes. In tone mode operation, it provides the regulated supply voltage to the MK5375 which determines the DTMF signal amplitude at the Tone Output. Varying the supply voltage will vary the DTMF output signal. In pulse mode, it helps provide some isolation from the transients caused by switching the speech network in and out.

During normal off-hook dialing, the MK5375 operates using current from the telephone line. On-hook number storage and memory retention current are supplied by the battery shown in Figure 7. Transistor Q6 prevents the flow of battery current to the speech network.

The rate at which dialing occurs is determined by the values chosen for resistor R1 and capacitor C1. These values can be predetermined using equation (1.0) described above. The 3.5795 MHz crystal is used as a reference for synthesizing the DTMF signals and is activated only for the short periods during which these tones are being generated.

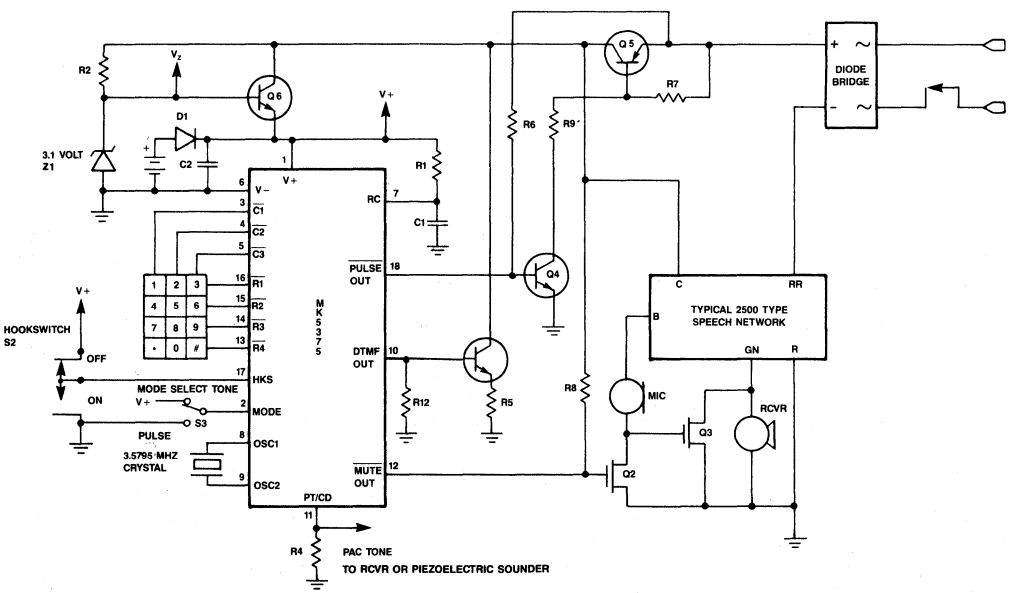
The application circuit schematic in Figure 8 gives an example of the various features which can be utilized with the addition of several switches. The example also shows that multiple devices may be used to increase the effective storage capability of the telephone design.

Much of the circuitry used to modulate and pulse the line, mute the speech network, and regulate the supply voltage is unchanged from the basic tone/pulse switchable telephone described above.

The two devices in Figure 8 are hooked up in parallel with one another except for their oscillator pins and the Chip Disable inputs. A DPDT switch is used to select between the two dialers through the Chip Disable pin; one device is activated while the other is put on standby.

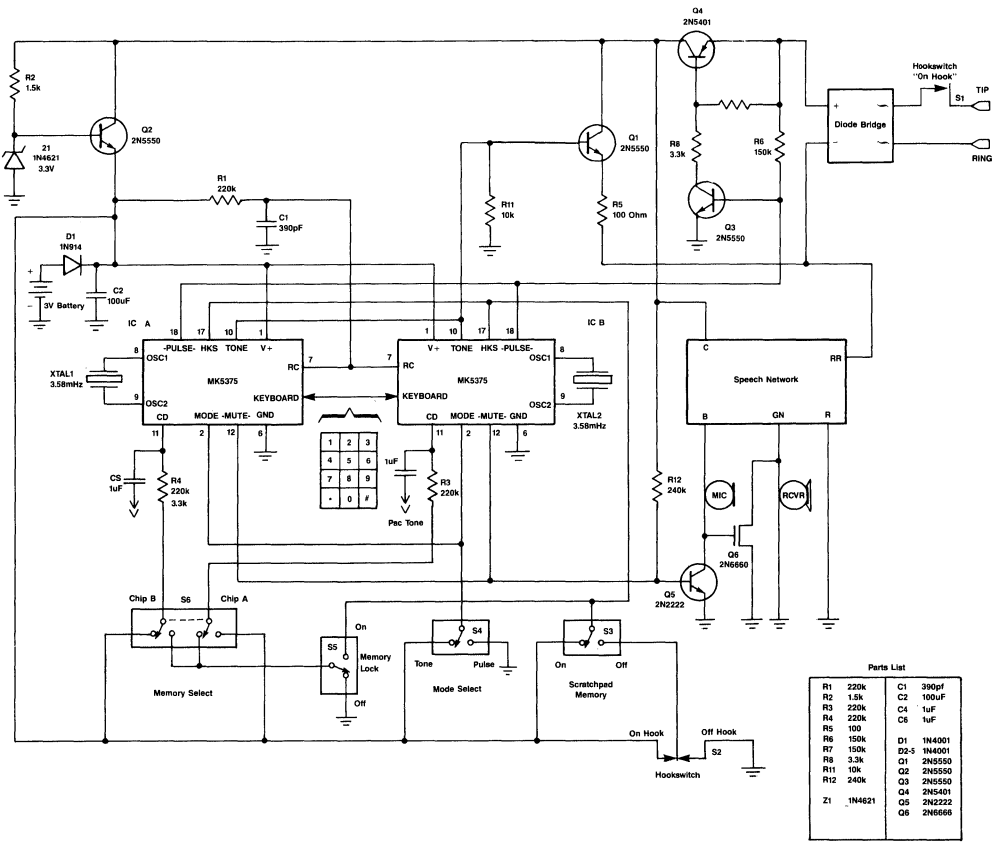
Some applications may include a memory lock switch to prevent any of the data stored to be changed inadvertently. This memory lock switch can take the form of a locking key switch, which would allow only the person with the key to alter data stored in memory.

A scratchpad feature may be implemented to allow off-hook programming of the memory while inhibiting dialing. A switch is added in series with the telephone hook-switch to allow the dialer to be forced into its on-hook key entry mode while the telephone set is off-hook.



R1	220K	Q1	2N5550	C1	390 PF
R2	1.6K	Q2	2N6660	C2	68μF
		Q3	2N6660		
R4	220K	Q4	2N5550	BATTERY 3 VOLT CELL	
R5	100Ω	Q5	2N5401	BRIDGE	
R6	160K	Q6	2N5550		
R7	150K	D1	1N914		
R8	240K	Z1	10K920		
R9	3.3K				
R12	10K				

Figure 7. MK5375 Circuit Schematic



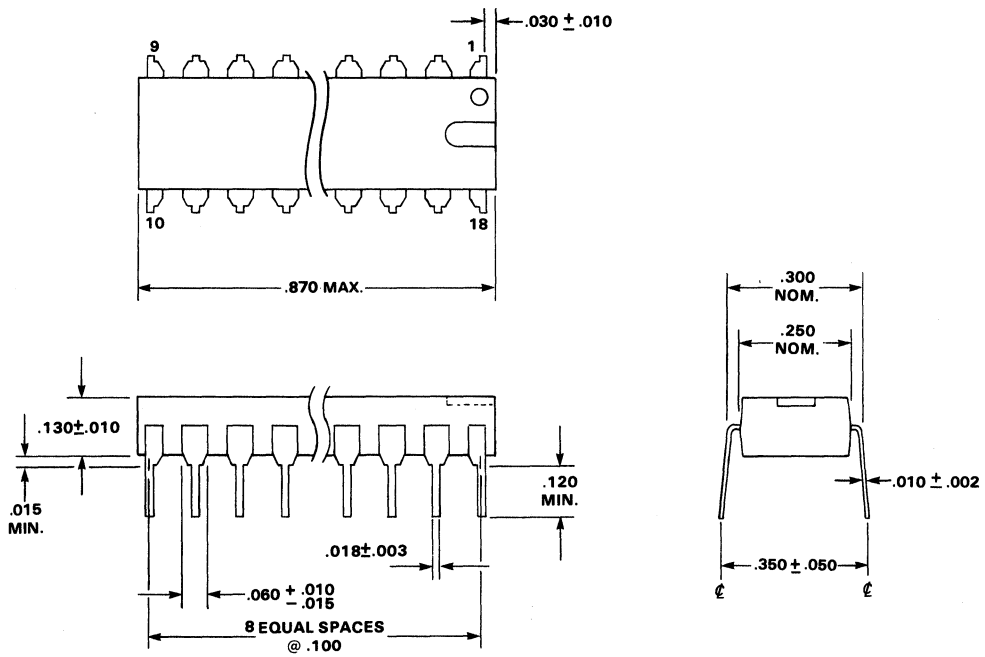
Parts List

R1	220k	C1	390pf
R2	1.5k	C2	100uF
R3	220k	C4	1uF
R4	220k	C6	1uF
R5	100		
R6	150k	D1	1N4001
R7	150k	D2-5	1N4001
R8	3.3k	Q1	2N5550
R11	10k	Q2	2N5550
R12	240k	Q3	2N5550
		Q4	2N5401
Z1	1N4621	Q5	2N2222
		Q6	2N6666

Figure 8. MK5375 Application Circuit Schematic

PACKAGE DESCRIPTION

18-Pin DIP (N) (.300)
Plastic



NOTE: Overall length includes .010 flash on either end of package

THOMSON COMPONENTS
MOSTEK

MK5376

10-NUMBER REPERTORY TONE/ PULSE DIALER

COMMUNICATIONS PRODUCTS

FEATURES

- ☐ Converts push-button inputs to both DTMF and pulse signals
- ☐ Stores ten 16-digit telephone numbers including last number dialed
- ☐ Pacifier tone and PBX pause
- ☐ Last number dialed (LND) privacy
- ☐ Manual and auto-dialed digits may be cascaded
- ☐ Ability to store and dial both * and # DTMF signals

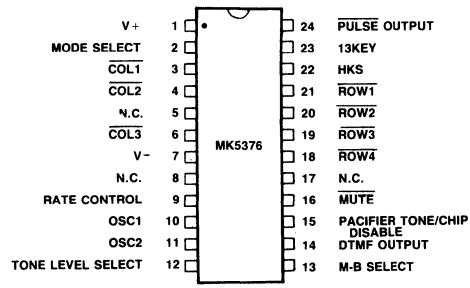


Figure 1. Pin Connection

DESCRIPTION

The MK5376 (see Figure 1) is a monolithic, integrated circuit manufactured using Mostek's Silicon Gate CMOS process. This circuit provides the necessary signals for either DTMF or loop disconnect dialing. Ten telephone numbers of up to 16 digits each may be stored in the on-chip RAM. Manual and auto-dialed numbers may be cascaded in any order.

Additional functions available are a Pacifier Tone output, PABX pause, external control of the signaling rate, and total functional control with either a standard 3x4 matrix keypad (FORM-A) or a 2-of-7 keyboard. A 13th key option allows control of the dialer's repertory features. The telephone keypad then functions for signaling purposes only, independent of the repertory functions. The 13th key mode and the M-B (Make/Break) Ratio is user selectable.

The dialer's flexibility provides for many applications, for example, off-hook programming, the use of additional chips in parallel for 10, 20, and 30 number repertory phones, permanent memory protection and the option of a supply-independent or supply-dependent tone level.

FUNCTIONAL PIN DESCRIPTION

V+
Pin 1. Pin 1 is the positive supply for the circuit and must meet the voltage requirements defined in the Electrical Specifications.

MODE SELECT
Input. Pin 2. In normal operation, Pin 2 determines the Signaling Mode; a logic level 1 (V+) selects Tone Mode, while a logic level 0 (V−) selects Pulse Mode operation. To guarantee proper dialing, this input must be tied to one of the supplies.

$\overline{\text{COL1}}$, $\overline{\text{COL2}}$, $\overline{\text{COL3}}$, $\overline{\text{ROW4}}$, $\overline{\text{ROW3}}$, $\overline{\text{ROW2}}$, $\overline{\text{ROW1}}$
Keyboard Input. Pins 3, 4, 6, 18, 19, 20, 21. The MK5376 keypad interface allows users to add either the standard 2-of-7 keyboard with negative common or the inexpensive single-contact (Form-A) keyboard (see Figure 2). A valid key entry is either a single Row connected to a single Column or V− presented to both a single Row and Column. In Standby Mode, either all the Rows pull to a logic 1 (V+) and all the Columns are a logic 0 or vice versa.

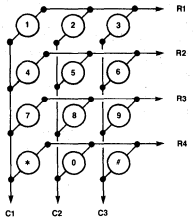


Figure 2A. Keyboard Schematics-Calculator-Type Keypad

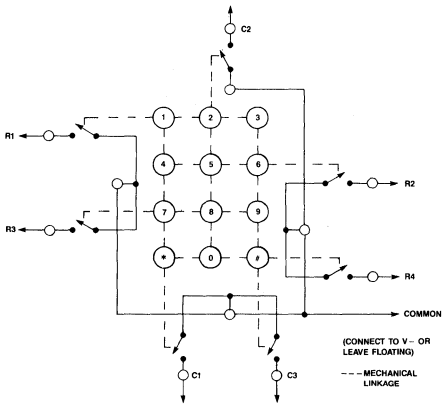


Figure 2B. Keyboard Schematics-Standard Telephone-Type Keypad

The keyboard interface logic detects an input being pulled low and enables the RC (RATE CONTROL) oscillator and keypad scan. Scanning consists of Rows and Columns alternately strobing high through on-chip pullups. After both a valid Row and Column key closure have been detected, the debounce counter is enabled. Breaks in contact continuity (bouncing contacts, etc.) are ignored for a debounce period (Tdb) of 32 ms. At this time, the keypad is sampled. If both Row and Column information is valid, this information is buffered into the LND.

V–

Input. Pin 7. This pin is the negative supply input to the device. This is the voltage reference for all specifications.

RATE CONTROL

Input. Pin 9. RATE CONTROL is a single-pin RC oscillator. An external resistor and capacitor determine signaling rates in both Tone and Pulse Modes. An 8 kHz oscillation provides nominal signaling rates of 10 PPS (pulses per second) in Pulse Mode and 5 TPS (tones per second) in Tone Mode; the tone duty cycle is 98 ms on, 102 ms off. RC values on this input can be adjusted to a maximum oscillation frequency of 16 kHz, resulting in an effective Pulse rate of 20 PPS and Tone rate of 10 TPS.

The following equation approximates the oscillation frequency:

$$Fosc = 1/(1.49RC)$$

The capacitor's (C) suggested value should be a maximum of 410 pF to guarantee accuracy of the oscillator. The resistor (R) is then selected for the desired signaling rate. The nominal frequency of 8 kHz is achieved with component values of 390 pF and 220K ohms.

OSC1, OSC2

Input/Output. Pins 10, 11. Pins 10 and 11 are the input and output, respectively, of an on-chip inverter. They have sufficient loop gain to oscillate when used with a low-cost television color-burst crystal. The nominal crystal frequency is 3.579545 MHz and any deviation is directly reflected in the Tone Output frequencies.

The repertory dialer directly controls the oscillator and is only enabled for tone signal transmission. It remains off at all other times and the input is high impedance. An external source may also drive the input.

TONE LEVEL SELECT

Input. Pin 12. The MK5376 has selectable tone levels with supply-independent or supply-dependent specifications. The tone levels available are similar to those provided on Mostek's industry standard MK5380 and MK5089 DTMF generators (see Table 1). The optimum tone scheme is application-dependent.

Table 1. Tone Level Select

Tone Level Select Input	Tone Reference	Compatible With
V– (Method 1)	Supply	MK5089
V+ (Method 2)	On-Chip Reference	MK5380

Method 1 operates from a regulated supply. The tone level is related to this supply by either of the following equations:

$$T_O = 20 \text{ LOG } [0.0776 (V+)/0.775] \text{ dBm}$$
$$T_O = 0.0776 (V+) \text{ Vrms}$$

Method 2 provides a constant tone output and modulates its own supply in a minimum parts count configuration. The tone level, when used in a subscriber set, is a function of the output resistor R_E and the telephone AC resistance R_L. The low-group single tone output amplitude is a function of R_E and R_L described by the equation:

$$V_O = \{1/[0.2+R_E)/R_L]\}T_O$$

where V_O is the tone amplitude at the phone line and T_O is the tone level at the DTMF OUTPUT pin. This version may also be operated on a regulated supply, but users must observe additional caution to prevent signal distortion (clipping) on longer loops.

M/B SELECT
Input. Pin 13. In Pulse Mode, this pin selects the Make/Break ratio, or the percentage Break time per Pulse period (see Table 2).

Table 2. Make/Break Ratio

M-B SELECT INPUT	BREAK TIME	MAKE TIME
V+	68	32
V−	60	40

DTMF OUTPUT
Output. Pin 14. The DTMF OUTPUT pin is connected internally to an NPN transistor's emitter with a collector tied to V+. The transistor base is the output of an on-chip operational amplifier that mixes the Row and Column Tones together.

The DTMF OUTPUT level is the sum of a single Row single tone sine wave is shown in Figure 3. This waveform is synthesized using a resistor tree with sinusoidally weighted taps. DTMF output frequencies are defined by Table 3.

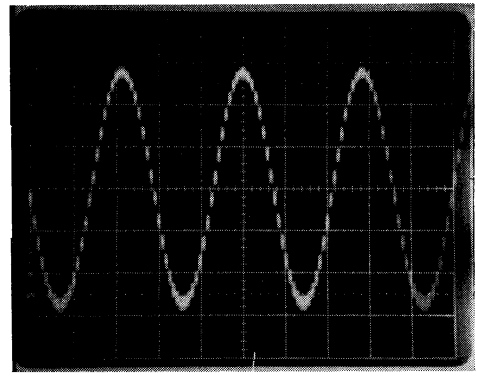


Figure 3. Typical Sine Wave Output - Single Tone

Table 3. Output Frequency

KEY INPUT	STANDARD FREQUENCY	ACTUAL FREQUENCY	% DEVIATION
ROW 1	697	699.1	+0.31
2	770	766.2	−0.49
3	852	847.4	−0.54
4	941	948.0	+0.74
COL 1	1209	1215.9	+0.57
2	1336	1331.7	−0.32
3	1477	1471.9	−0.35

PACIFIER TONE OUTPUT/CHIP DISABLE
Input/Output. Pin 15. A 500 Hz square wave is output on this pin after acceptance of a valid key input and after the 32 ms debounce time. The square wave terminates after a maximum of 30 ms or when the valid key is no longer present. The PACIFIER TONE audibly signals a valid key entry. This feature is particularly useful for on-hook storage and Pulse Mode signaling. The PACIFIER TONE is not enabled when users manually dial in Tone Mode. This eliminates any confusion between the audible DTMF feedback and the PACIFIER TONE. In both cases, the tone confirms that the key has been properly entered and accepted. Without the tone, users do not know if the keys have been properly entered.

This pin is normally high impedance until a key is entered. It also serves as a CHIP DISABLE pin. Pulling this input high through a resistor disables the keypad (high impedance) and initializes all counters and flip flops (memory remains undisturbed). Pulling the input low through the same resistor enables the circuit.

This feature is useful in several applications. It provides a convenient way to lock memory by connecting this input through a resistor to HKS. When it is on-hook, the device is then disabled and key inputs are not recogniz-

ed. The circuit will function normally off-hook. Information can only be entered into the permanent memory locations by switching to Program Mode. This requires that a switch and resistor be added to connect to V−.

$\overline{\text{MUTE}}$

Output. Pin 16. This pin is the mute output for both Tone and Pulse Modes. Timing depends on which mode is used.

The output consists of an open drain N-channel device and zener input protection. During standby, the output is high impedance and generally requires an external pullup resistor to the positive supply.

In Tone Mode, $\overline{\text{MUTE}}$ removes the transmitter and receiver from the network during DTMF signaling. The output then mutes continuously while auto-dialing and during manual DTMF signaling.

In Pulse Mode, the $\overline{\text{MUTE}}$ removes the receiver or even the entire network from the line. Timing is available both as a continuous mute (provided by the MK5376) or a mute that is active only when actually pulsing the line. Figure 4 depicts these timing relationships.

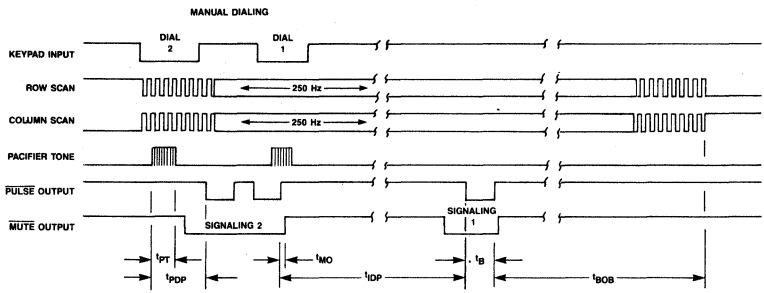


Figure 4A. MK5376 Timing Diagram — Pulse Mode Off-Hook Operation

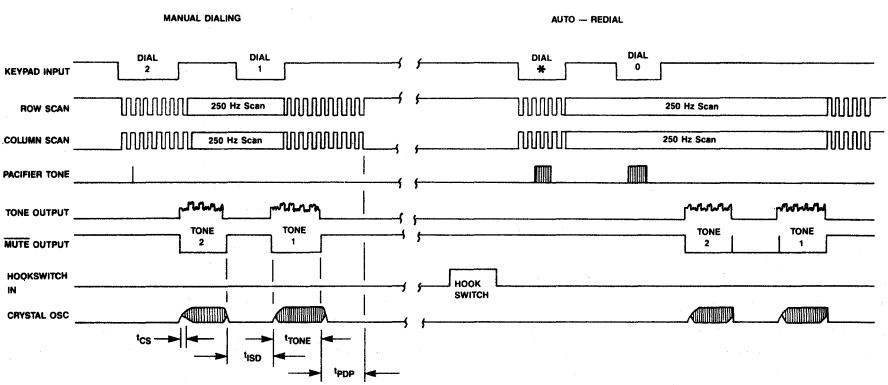


Figure 4B. MK5376 Timing Diagram — Tone Mode

HKS
Input. Pin 22. This pin is a high impedance input and must be switched high for on-hook operation or low for off-hook operation. A transition on this input initializes the on-chip logic. This stops the current operation. A logic level independent of the hookswitch position may be presented to this input, which allows on-hook operations, such as storage, to be performed off-hook.

13KEY
Input. Pin 23. This pin is a high impedance input. When it is tied permanently low, it indicates 12KEY Mode. If users desire 13KEY operation, a switch to the negative supply is attached to this pin, along with an external pullup. This forces the repertory dialer into 13KEY Mode. The dialer switches to 12KEY mode if users depress the 13th key switch while simultaneously entering information through the keypad. The differences between these modes are presented in the Device Operation section.

$\overline{\text{PULSE}}$ OUTPUT
Output. Pin 24. An open drain N-channel device drives this pin. In Pulse Mode, the timing meets Bell Telephone and EIA specifications for loop disconnect signaling. The Make/Break ratio is user-selectable. RATE CONTROL regulates the dialing rate.

DEVICE OPERATION

The MK5376 interfaces to two keypad configurations - the 12KEY and 13KEY Modes (see Figures 5 and 6). This flexibility simplifies interfacing to existing keypads and products. The MK5376 can be used in inexpensive telephones with basic 3x4 matrix keypads to give them repertory dialer features. In 13KEY Mode, the MK5376 allows the keypad to be used for standard signaling and the special repertory functions are only activated by using the "control" (13th) key.

In both modes, keypad entries are decoded, debounced, and (if valid) stored in the LND (Last Number Dialed) buffer that acts much like a FIFO (First-In-First-Out) register. Each subsequent entry is stacked in the buffer. The dialing sequence begins 100 ms after the first digit is accepted. Each digit buffered into the RAM is dialed out with a 98 ms burst of DTMF and a 102 ms intersignal time.

Buffering data into the RAM before signaling is an important feature. This allows less expensive keypads to be used since users cannot enter digits too quickly for the system and the PACIFIER TONE can provide audible feedback after each non-toned key entry. It also guarantees that data stored in the RAM exactly matches the digits actually dialed.

Users can perform consecutive manual and auto-dialing, if auto-dialing is used to accomplish only a part of the desired number sequence. However, manual and auto-dialing cannot be performed simultaneously.

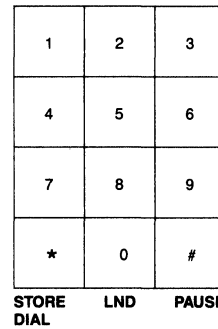
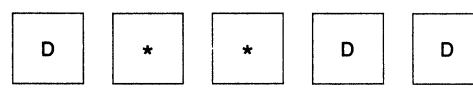


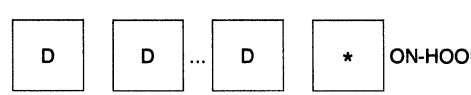
Figure 5. Keypad Configuration 12KEY Mode (Tone Mode)

NORMAL DIALING



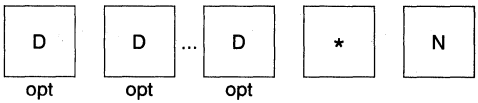
In 12KEY Mode, the " * " (Star) key is the modifier used to control repertory functions. All numeric keys signal normally unless a modifier precedes them. To signal either a " * " or "#," users must enter these keys twice in succession. The first entry is not signaled or stored.

LND PRIVACY



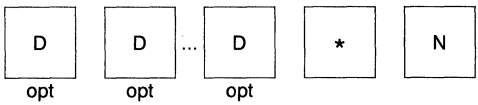
A " * " input prior to going on-hook erases information in the LND buffer.

AUTO-DIALING (Off-Hook)



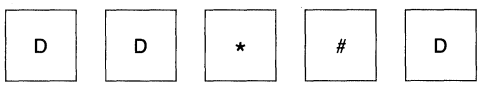
The key sequence "*" followed by any digit auto-dials the number sequence stored in the designated address location. Note auto-dial can take place following manual key inputs.

STORAGE (On-Hook)



The number sequence stored in the LND buffer can be transferred to one of the nine other "permanent" locations with the simple sequence "*" followed by the address. New digits may be written into the LND buffer while on-hook. To enter a "*" signal, users enter the "*" key twice in succession as when dialed off-hook.

PABX PAUSE (Off-Hook and On-Hook)



When users input "*" key followed by a "#", an indefinite pause is stored in a number sequence. Upon redialing the number sequence, the dialer will pause when it encounters "#." A key input makes it continue.

KEYPAD CONFIGURATION 12KEY MODE (PULSE MODE)

Most of the Pulse key operations are identical to those in the 12KEY Tone Mode; PABX Pause is the only exception. In Pulse Mode, the pause is stored with a single "#" input. Two "#" inputs store two pauses.

The "*" key exercises the control function; two "*" inputs are the same as a single input (multiple inputs are not accepted).

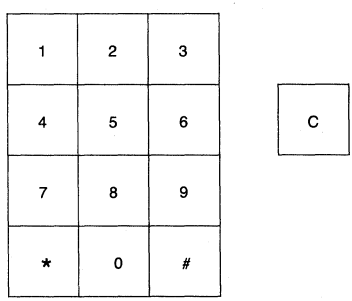
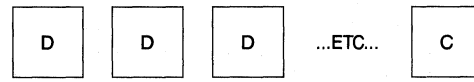


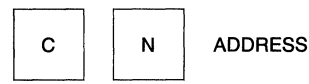
Figure 6. Keypad Sequence 13KEY Configuration

NORMAL DIALING AND LND PRIVACY OPTION (Off-Hook)



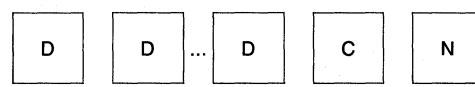
Normal dialing is straightforward; all keypad entries are stored in the LND (Last Number Dialed) buffer and signaled as each is entered. All digits in the LND register are maintained unless the final key prior to going on-hook is "C." In the metal mask version, the LND buffer is cleared unless users make a Control entry before going on-hook.

AUTO-DIALING (Off-Hook)



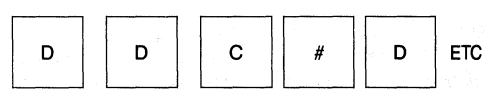
To auto-dial, users enter the control key "C," followed by the address key, (shown here as "N," representing memory location N). As soon as the address key is decoded and debounced, auto-dialing begins. Address zero is used to auto-dial LND.

STORAGE (On-Hook)



To store data in a given location (LOC N) users simply enter digits into the LND buffer and copy them to "N" by entering a control key "C" followed by the desired address. Users can copy the last number dialed before going on-hook to another location if they make no entries before the copy operation.

PABX PAUSE



Users may inject a pause at any point in the dialed sequences by keying in "C" followed by "#." When this number sequence is redialed, the dialer pauses indefinitely and continues to dial when another key input is received.

ABSOLUTE MAXIMUM RATINGS*

DC Supply Voltage ..... 6.5 Volts
Operating Temperature ..... −30°C to +60°C
Storage Temperature ..... −55°C to +85°C
Maximum Power Dissipation (25°C) ..... 500 mW
Maximum Voltage on any Pin ..... (V+) +0.3 Volts; (V−) −0.3 Volts

*All specifications are for 2.5 volt operation and full operating temperature range unless otherwise stated.

ELECTRICAL SPECIFICATIONS

DC CHARACTERISTICS

$-30°C \leq TA \leq 60°C$

SYM	PARAMETER	MIN	TYP	MAX	UNIT	NOTES
V+	DC Operating Voltage	2.5		6.0	V	
I_{SB}	Standby Current		0.3	1.0	μA	1
V_{MR}	Memory Retention Voltage	1.5			V	5
I_{MR}	Memory Retention Current	750	200		nA	5
I_T	Operating Current (Tone)		0.5	1.0	mA	2
I_P	Operating Current (Pulse)		50	150	μA	2
I_{ML}	Mute Output Sink Current	1.0	3.0		mA	3
I_{PL}	Pulse Output Sink Current	1.0	3.0		mA	3
I_{PC}	Pacifier Tone Sink/Source	250	500		μA	4
K_{RU}	Keypad Pullup Resistance		100		kΩ	
K_{RD}	Keypad Pulldown Resistance		500		kΩ	

NOTES:
1. All inputs unloaded, Quiescent Mode (oscillator off)
2. All inputs unloaded, single key input
3. V_{OUT} = 0.5 Volts
4. Sink Current for V_{OUT} = 0.5, Source Current for V_{OUT} = 2.0 Volts
5. Meeting these minimum supply requirements guarantees the retention of data stored in memory.

CHARACTERISTICS — KEYPAD INPUTS, PACIFIER TONE

SYM	PARAMETERS	MIN	TYP	MAX	UNITS	NOTES
T_{KD}	Keypad Debounce Time		32		ms	1
F_{KS}	Keypad Scan Frequency		250		Hz	1
T_{RL}	Two Key Rollover Time		4		ms	1
F_{PT}	Frequency Pacifier Tone		500		Hz	1
T_{PT}	Pacifier Tone		30		ms	1
F_{RC}	Frequency RC Oscillator	−7.0	+2.5	+7.0	%	2

NOTES:
1. Times based upon 8 kHz RC input for RATE CONTROL
2. Deviation of oscillator frequency takes into account all voltage, temperature and unit-to-unit variations, but does not include the tolerance of external components.

CHARACTERISTICS — TONE MODE

SYM	PARAMETERS	MIN	TYP	MAX	UNITS	NOTES
T_{NK}	Tone Output No Key Down			−80	dBm	1
T_{Od}	Tone Output (dependent)	−13 173	−12 194	−11 218	dBm mV(rms)	1, 2
P_{Ed}	Pre-Emphasis, High Band		2.7		dB	
V_{DCd}	Average DC Bias Tone Out (V+ = 2.5 V)		1.2		Volts	
T_{Oi}	Tone Output (independent)		−12 194		dBm mV(rms)	2, 3
PE_i	Pre-Emphasis, High Band		2.0		dB	3
V_{DCi}	Average DC Bias Tone Out		1.5		Volts	
DIS	Output Distortion		5.0	8.0	%	3
R_E	Tone Output Load			10	kΩ	4
TR	Tone Signaling Rate		5	10	1/sec	5
PSD	Pre-Signal Delay		132		ms	5
ISD	Inter-Signal Delay		100		ms	5

NOTES:
1. ODBm equals 1 mWatt signal power into a 600 Ohm load or 775 mVolts
2. Single tone (low group) V+ = 2.5 V.
3. Supply voltage = 2.5 to 6 volts, R_E = 10K Ohms.
4. Maximum load which can be connected externally to pin 10 and maintain proper tone levels.
5. These values are directly related to the RC component values connected to Pin 7, the rate control frequency is nominally 8 kHz.

AC CHARACTERISTICS — PULSE MODE OPERATION

SYM	PARAMETERS	MIN	TYP	MAX	UNITS	NOTES
P_R	Pulse Rate		10		PPS	1
PDP	Predigital Pause		172		ms	1
IDP	Interdigital Pause		940		ms	1
T_{MO}	Mute Overlap Time		2		ms	1

NOTE:
1. Typical times assume nominal RC input frequency of 8 kHz. An increase in frequency results in an equal decrease in time values and increase in rate values.

FEATURES

- ☐ Single chip DTMF and pulse dialer.
- ☐ Softswitch changes signaling mode from pulse to tone.
- ☐ Nine number repertory plus recall of last number dialed (18 digits each).
- ☐ Flash key input initiates timed hook flash.
- ☐ 8 Tone Per Second dialing in tone mode and 10 PPS in pulse mode.
- ☐ DTMF active until key release.
- ☐ Minimum DTMF duration/separation guaranteed (74/54 ms).
- ☐ Pacifier tone provides audible indication of valid key input for non-DTMF key entries.
- ☐ Powered from telephone line, low operating voltage for long loop applications.

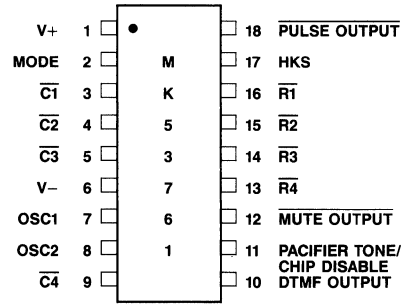


Figure 1. Pin Connection

DESCRIPTION

The MK53761 is a Mostek Silicon Gate CMOS IC that provides necessary signals for either DTMF or loop disconnect (pulse) dialing. The MK53761 buffers up to 18 digits into memory that can be later redialed with a single key input. Up to nine repertory numbers may be stored. Users can store all 12 signaling keys and access several unique functions with single key entries. These functions include: Last Number Dialed (LND), Softswitch, and Flash. Figure 2 shows the keypad configuration.

A LND key input automatically redials the last number dialed. The PROG key provides an easy way to program a number into any memory location (1-9) whether on-hook or off-hook. The MEM key allows easy redialing of the number stored in memory locations (1-9).

The FLASH key simulates a 560 ms hook flash to transfer calls or to activate other special features provided by the PABX or a central office.

1	2	3	FLASH
4	5	6	PROG
7	8	9	MEM
* SOFTSWITCH	0	#	LND

Figure 2. Keypad Configuration

FUNCTIONAL PIN DESCRIPTION

V+
Pin 1. V+ is the positive supply for the circuit and must meet the maximum and minimum voltage requirements. (See Electrical Specifications.)

MODE
Input. Pin 2. MODE determines the dialer's default operating mode. When the device is powered up or the hookswitch input is switched from on-hook, (V+), to off-hook, (V−), the default determines the signaling mode. A V+ connection defaults to tone mode operation and a V− connection defaults to pulse mode operation.

When dialing in the pulse mode, a softswitch feature will allow a change to the tone mode whenever the * key, or softswitch, is depressed. Subsequent * key inputs will cause the DTMF code for an * to be dialed. The softswitch will only switch from pulse to tone. After returning to on-hook and back to off-hook, the part will be in pulse mode. Redial by the LND key will repeat the softswitch.

$\overline{C1}$, $\overline{C2}$, $\overline{C3}$, $\overline{C4}$, $\overline{R4}$, $\overline{R3}$, $\overline{R2}$, $\overline{R1}$
Keyboard inputs. The MK53761 interfaces with either the standard 2-of-8 with negative common or the single-contact (Form A) keyboard.

A valid keypad entry is either a single Row connected to a single Column or V− simultaneously presented to both a single Row and Column. In its quiescent or standby state, during normal off-hook operation, either the Rows or the Columns are at a logic level 1 (V+). Pulling one input low enables the on-chip oscillator. Keyboard scanning then begins. Scanning consists of Rows and Columns alternately switching high through on-chip pullups. After both a Row and Column key have been detected, the debounce counter is enabled and any noise (bouncing contacts, etc.) is ignored for a debounce period (T_{KD}) of 32 ms. At this time, the keyboard is sampled and if both Row and Column information are valid, the information is buffered into the LND location. If switched on-hook (pin 17 to pin 1), the keyboard inputs all pull high through on-chip pull-up resistors.

In the tone mode, if 2 or more keys in the same row or if 2 or more keys in the same column are depressed a single tone will be output. The tone will correspond to the row or column for which the 2 keys were pushed. This feature is for test purposes, and single tones will not be redialed.

Also in the tone mode, the output tone is continuous in manual dialing as long as the key is pushed. The output tone duration follows the table below:

Table 1. Output Tone Duration

KEY-PUSH TIME, T*	TONE OUTPUT*
$T \leq 32$ ms	No output. Ignored by MK53761.
32 ms $\leq T \leq 75$ ms + T_{KD}	75 ms duration output.
$T \geq 75$ ms + T_{KD}	Output duration = $T - T_{KD}$

*NOTE: T_{KD} is the key pad debounce time which is typically 32 ms.

When redialing in the tone mode, each DTMF output is 75 ms duration, and the tone separation (intersignal delay) is 50 ms.

V−
Input. Pin 6 is the negative supply input to the device. This is the voltage reference for all specifications.

OSC1, OSC2
Pin 7 (input), pin 8 (output). OSC1 and OSC2 are connections to an on-chip inverter used as the timing reference for the circuit. It has sufficient loop gain to oscillate when used with a low-cost television color-burst crystal. The nominal crystal frequency is 3.579545 MHz and any deviation from this standard is directly reflected in the Tone output frequencies. The crystal oscillator provides the time reference for all circuit functions. A ceramic resonator with tolerance of ±0.25% may also be used.

DTMF OUTPUT
Output. Pin 10. An NPN transistor emitter with a collector tied to V+ drives the DTMF OUTPUT pin. The transistor base is connected to an on-chip operational amplifier that mixes the Row and Column tones. Figure 7 shows the timing at this pin.

The DTMF OUTPUT is the summation of a single Row frequency and a single Column frequency. A typical single tone sine wave is shown in Figure 4. This waveform is synthesized using a resistor tree with sinusoidally weighted taps.

The MK53761 is designed to operate from an unregulated supply; the TONE LEVEL is supply independent, and the single row tone output level will be typically:

$$T_{oi} = -12 \text{ dBm} \pm 1 \text{ dB}$$

The DC component of the DTMF output while active is described by the following equation:

$$V_{DC_1} = 0.3\ V+ + 0.5 \text{ Volts}$$

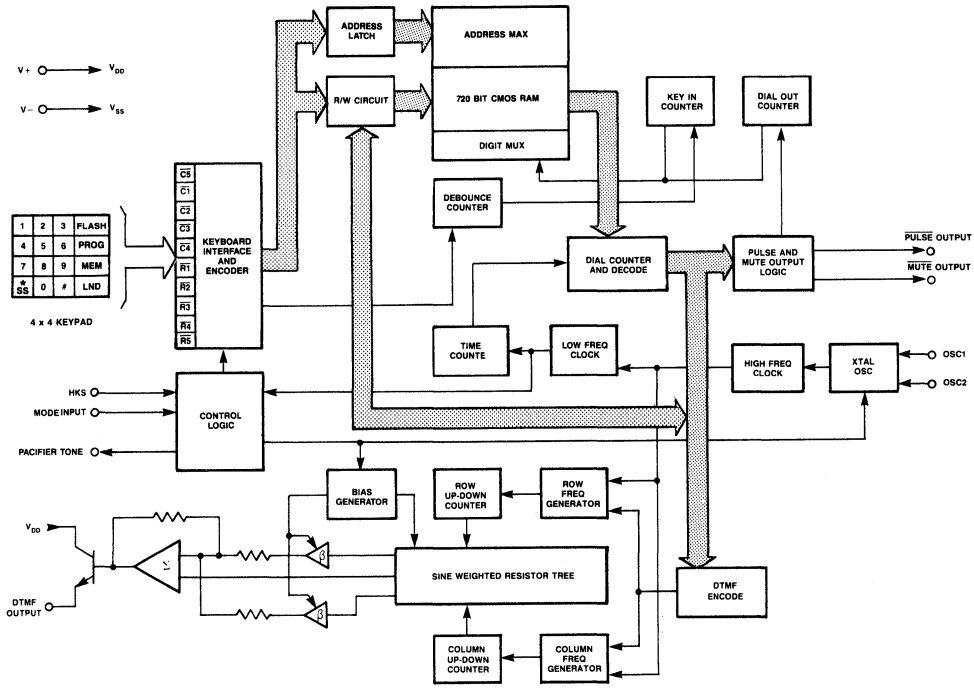


Figure 3. MK53761 Functional Block Diagram

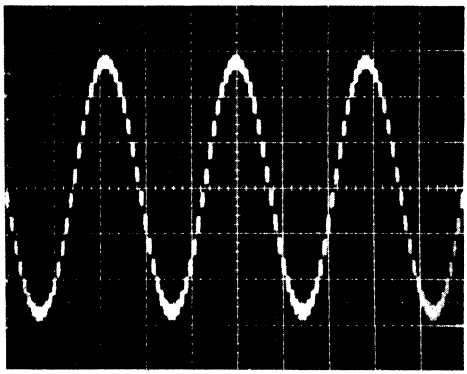


Figure 4. Typical Single Tone

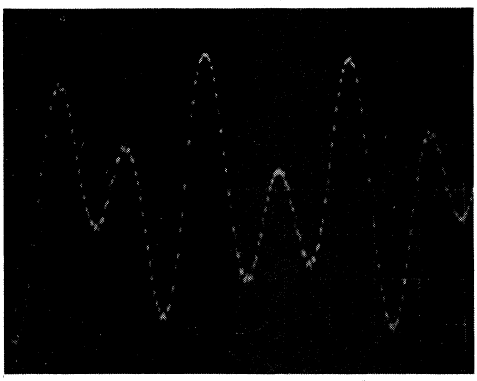


Figure 5. Typical Dual Tone

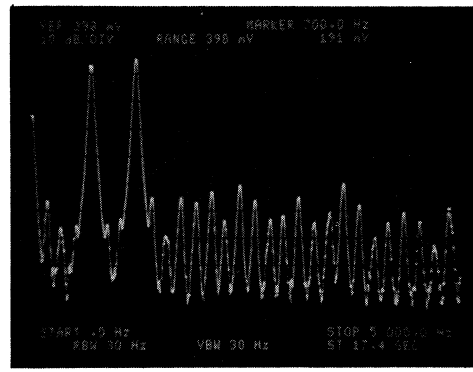


Figure 6. Typical Spectral Response

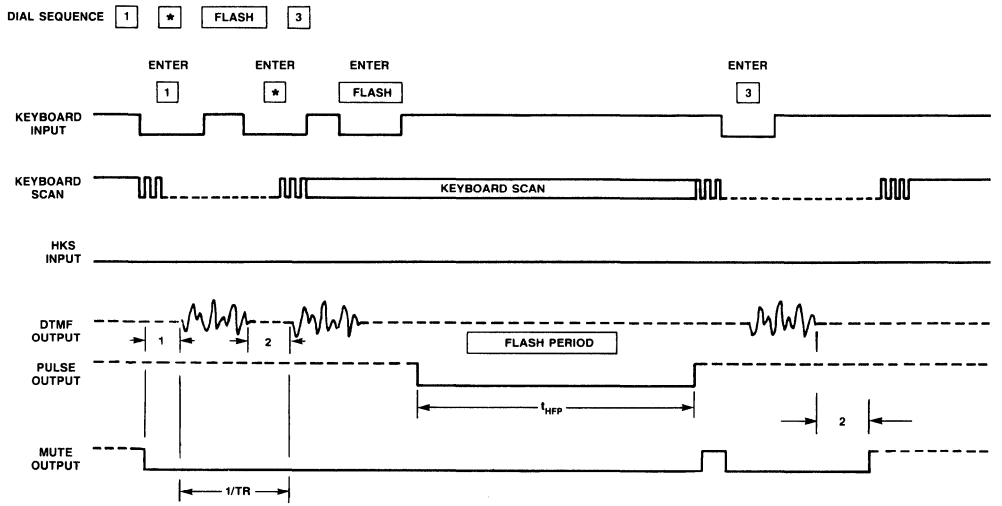
PACIFIER TONE OUTPUT/CHIP DISABLE INPUT

Output. Pin 11. The pacifier tone provides audible feedback, confirming that the key has been properly entered and accepted. A 500 Hz square wave is activated upon acceptance of a valid key input, after the 32 ms debounce time. The square wave terminates after a maximum of 30 ms or when the valid key is no longer present. In pulse mode, all key entries activate the pacifier tone. In tone mode, any non-DTMF key (LND, FLASH, MEM, PROG) entry activates the pacifier tone. When programming the chip, all valid key entries activate the pacifier tone in either pulse or tone mode.

The CHIP DISABLE is an input. When pin 11 is switched low through a resistor (10K to 100K), the MK53761 is enabled. When pin 11 is switched to V+ through the resistor, all keypad inputs are pulled high, and the MK53761 will ignore all keypad inputs. When the chip is disabled, it will not dial, and it cannot be programmed. The chip can only be disabled when the circuit is inactive (not dialing) and Pin 12 is switched high.

Table 2. DTMF Output Frequency

KEY INPUT		STANDARD FREQUENCY	ACTUAL FREQUENCY	% DEVIATION
ROW	1	697	699.1	+0.31
	2	770	766.2	−0.49
	3	852	847.4	−0.54
	4	941	948.0	+0.74
COL	1	1209	1215.9	+0.57
	2	1336	1331.7	−0.32
	3	1477	1471.9	−0.35



NOTE:

1. For this example, key entries are ≤75 ms, but ≥32 ms.
2. $\overline{\text{MUTE}}$ goes active after any key is depressed.

Figure 7. Tone Mode Timing

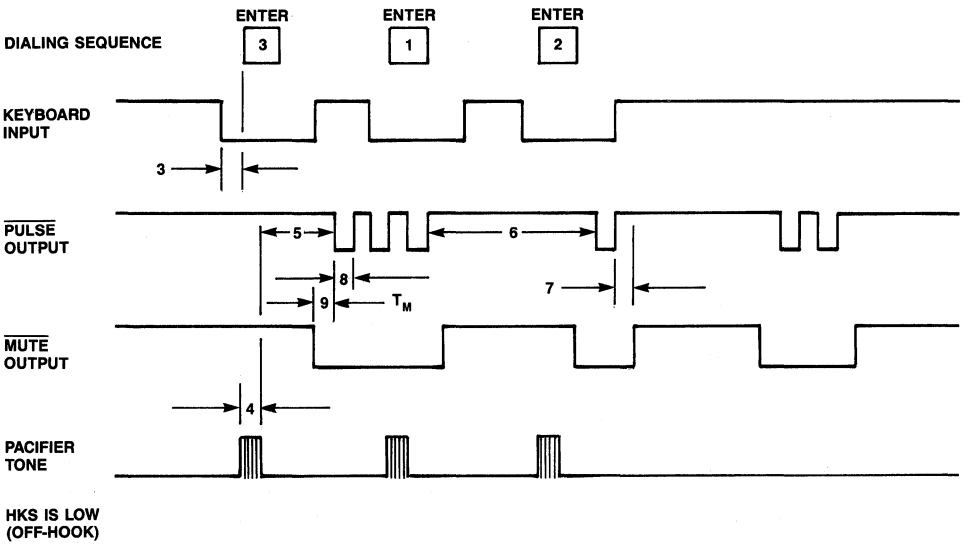


Figure 8. Pulse Mode Timing

MUTE OUTPUT
Output. Pin 12. This pin is the $\overline{\text{MUTE OUTPUT}}$ for both tone and pulse modes. Timing is dependent upon mode.

The $\overline{\text{MUTE OUTPUT}}$ consists of an open drain N-channel device. During standby, the output is high impedance and generally has an external pullup resistor to the positive supply.

In the tone mode, $\overline{\text{MUTE OUTPUT}}$ is used to remove the transmitter and the receiver from the network during DTMF signaling. During dialing, $\overline{\text{MUTE OUTPUT}}$ is active continuously until dialing is completed. $\overline{\text{MUTE OUTPUT}}$ goes active when any key is pushed.

In the pulse mode, $\overline{\text{MUTE OUTPUT}}$ is used to remove the receiver and the network from the line. Different circuitry is required for tone and pulse muting external to the IC and applications using both modes would not necessarily share circuitry. $\overline{\text{MUTE OUTPUT}}$ timing is shown in Figure 8 for pulse mode signaling and Figure 7 for tone mode signaling. $\overline{\text{MUTE OUTPUT}}$ is active during each digit, and not active during the interdigit time. In both tone and pulse modes, $\overline{\text{MUTE OUTPUT}}$ goes active 40 ms before $\overline{\text{PULSE OUTPUT}}$ for a FLASH. Figure 8 illustrates the timing for this pin.

HKS
Input. Pin 17. Pin 17 is the hookswitch input to the MK53761. This is a high-impedance input and must be switched high for on-hook operation or low for off-hook operation. A transition on this input causes the on-chip logic to initialize, terminating any operation in progress at the time. The signaling mode defaults to the mode selected at pin 2.

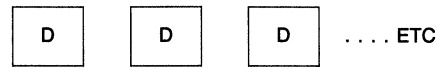
$\overline{\text{PULSE OUTPUT}}$
Output. Pin 18. This is an output consisting of an open drain N-channel device. In either pulse or tone mode, the FLASH key will cause a 560 ms output pulse at pin 18.

DEVICE OPERATION

When the MK53761 is not actively dialing, it consumes very little current. Row and Column inputs assume opposite states off-hook. The circuit verifies that a valid key has been entered by alternately scanning the Row and Column inputs. If the input is still valid following 32ms of debounce, the digit is stored into memory, and dialing begins after a pre-signal delay of approximately 40 ms (measured from initial key closure). Output tone duration is shown in Table 1.

The MK53761 allows manual dialing of an indefinite number of digits, but if more than 18 digits are dialed per number, the 53761 will "wrap around". That is, the extra digits beyond 18 will be stored at the beginning of the LND buffer, and the first 18 digits will no longer be available for redial. During autodial from LND or any memory location, key inputs are not accepted, but they will suspend dialing until released.

NORMAL DIALING (Off-Hook)

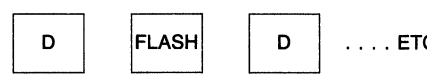


Normal dialing is straightforward, all keyboard entries will be stored in the buffer and signaled in succession.

LAST NUMBER DIALED (LND)

Last number dialing is accomplished by entering the LND key.

HOOK FLASH



Hook flash may be entered into the dialed sequence at any point by keying in the function key, FLASH. Flash consists of a timed Break of 560 ms. The FLASH function is stored in memory, but it will not be redialed as such. When a FLASH key is pressed, no further key inputs will be accepted until the hookflash function (560 ms break) has been dialed. The key input following a FLASH will be stored as the initial digit of a new number (overwriting the number dialed prior to the FLASH) unless it is another FLASH. Consecutive FLASH entries after a number is dialed will be stored sequentially in the LND memory and a subsequent LND entry will cause the redial of that number with a delay, but not hookflash breaks, at the end of the redialing sequence. When redialing in tone mode, $\overline{\text{MUTE OUTPUT}}$ will remain active during the flash delay period.

SOFTSWITCH

When dialing in the pulse mode, a softswitch feature will allow a change to the tone mode whenever the * key is depressed. Subsequent * key inputs will cause the DTMF code for an * to be dialed. The softswitch will only switch from pulse to tone. After returning to on-hook and back to off-hook, the part will be in pulse mode. Redial by the LND key will repeat the softswitch.

PROGRAMMING AND REPERTORY DIALING

Programming is independent of HKS (pin 17) and MODE (pin 2).

To program, enter the following:
PROG, Digit 1, Digit 2, ... , MEM, Location (1-9).
When programming, dialing is inhibited.

To dial a number from repertory memory (HKS must be low) enter the following:
MEM, Location (1-9)

To save the last number dialed: PROG, MEM, Location (1-9).

Table 3. Special Function Delays

Each delay shown below represents the time required from after the special function key is depressed until a new digit can be dialed.

The time is considered "FIRST" key is all previous inputs have been completed dialed. The time is considered "AUTO" if in redial, or if previous dialing is still in progress.

FUNCTION	FIRST/AUTO	DELAY (seconds)	
		PULSE	TONE
SOFTSWITCH	FIRST	0.40	—
	AUTO	1.10	—

Absolute Maximum Ratings*

DC Supply Voltage . . . . . 6.5 Volt
Operating Temperature . . . . . 0°C to +60°C
Storage Temperature . . . . . −55°C to +125°C
Maximum Power Dissipation (25°C) . . . . . 500 mW
Maximum Voltage on any Pin . . . . . (V+)+.3, (V−)−.3

* All specifications are for 2.5 Volt operation and full operating temperature range unless otherwise stated.

ELECTRICAL CHARACTERISTICS
DC Characteristics

SYM	PARAMETER	MIN	TYP	MAX	UNIT	NOTES
V+ TONE	DC Operating Voltage (Tone Mode)	2.5		6.0	Volts	
V_{MR}	Memory Retention Voltage	1.5	1.3		Volts	1, 6
I_S	Standby Current		0.4	1.0	μA	1
I_{MR}	Memory Retention Current		0.15	0.75	μA	5, 6
V_{MUTE}	Mute Output Operating Voltage	1.8			Volts	7
I_T	Operating Current (Tone)		300	600	μA	2
I_P	Operating Current (Pulse)		150	250	μA	2
	Operating Current On-Hook Program Mode Key Operated No-Key Operated			 200 1	 μA μA	
I_{ML}	Mute Output (2.5 Volts) Sink Current (4.0 Volts)	1.0 3.0			mA mA	3
I_{PL}	Pulse Output Sink Current	1.0	2.0		mA	3
I_{PC}	Pacifier Tone Sink/Source	250	500		μA	4
K_{RU}	Keypad Pullup Resistance		100		kohm	
K_{RD}	Keypad Pulldown Resistance		500		ohm	
V_{IL}	Keypad Input Level-Low	0		0.3V+	Volt	
V_{IH}	Keypad Input Level-High	0.7V+		V+	Volt	
V_{PULSE}	Operating Voltage (Pulse Mode)	1.8		6.0	Volts	

NOTES
1. All inputs unloaded, Quiescent Mode (oscillator off)
2. All outputs unloaded, single key input
3. V_{OUT} = 0.4 Volts
4. Sink Current for V_{OUT} = 0.5 volts, Source Current for V_{OUT} = 2.0 Volts
5. Memory Retention Voltage is the point where memory is guaranteed but circuit operation is not.
6. Proper memory retention is guaranteed if either the minimum I_{MR} is provided or the minimum V_{MR}. The design does not have to provide both the minimum current or voltage simultaneously.
7. Minimum voltage where activation of mute output with key entry is ensured.

AC Characteristics - Tone Mode

NO.	SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
—	T_{NK}	Tone Output No Key Down			−80	dBm	1
—	T_{Oi}	Tone Output (independent)	−13 173	−12 194	−11 218	dBm mV_{rms}	1, 2 3
—	PE_i	Pre-Emphasis, High Band	1.6	2.0	2.4	dB	
—	DC_i	Tone Output DC Bias (V+ = 2.5) (V+ = 3.5)	 1.2	1.0		Volts Volts	
—	R_E	Tone Output Load		10		kohm	4
—	T_{RIS}	Tone Output Rise Time		1.0		ms	5
—	DIS	Output Distortion		5.0	8.0	%	3
—	TR	Tone Signaling Rate		8.0		1/sec	
1	T_{PSD}	Pre-Signal Delay	40			ms	6
2	T_{ISD}	Inter-Signal Delay (repertory)		54		ms	
	T_{DUR}	Tone Output Duration (repertory)		74		ms	

NOTES

1. O dBm equals 1 mW power into 600 ohms or 775 mVolts.
   Important Note: The MK53761 is designed to drive a 10 kohm load. The 600 ohm load is only for reference.
2. Single tone (low group), as measured at pin 10, T_A = 25°C.
3. Supply voltage = 2.5 to 6 Volts, R_E=10 kohms.
4. Supply voltage = 2.5 Volts.
5. Time from beginning of tone output waveform to 90% of final magnitude of either frequency. Crystal parameters suggested for proper operation are R_s<100 ohms, L_m=96 mH, C_m=0.02 pF, C_h=5pF, f=3.579545 MHz, and C_L=18 pF.
6. Time from initial key input until beginning of signaling.

AC Characteristics - Keypad Inputs, Pacifier Tone

(Numbers in left hand column refer to the timing diagrams.)

NO.	SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
3	T_{KD}	Keypad Debounce Time		32		ms	1
—	F_{KS}	Keypad Scan Frequency		250		Hz	1
—	F_{PT}	Frequency Pacifier Tone		500		Hz	1
4	T_{PT}	Pacifier Tone Duration		30		ms	1
—	T_{HFP}	Hookflash Timing		560		ms	1

NOTES
1. Crystal oscillator accuracy directly affects these times.

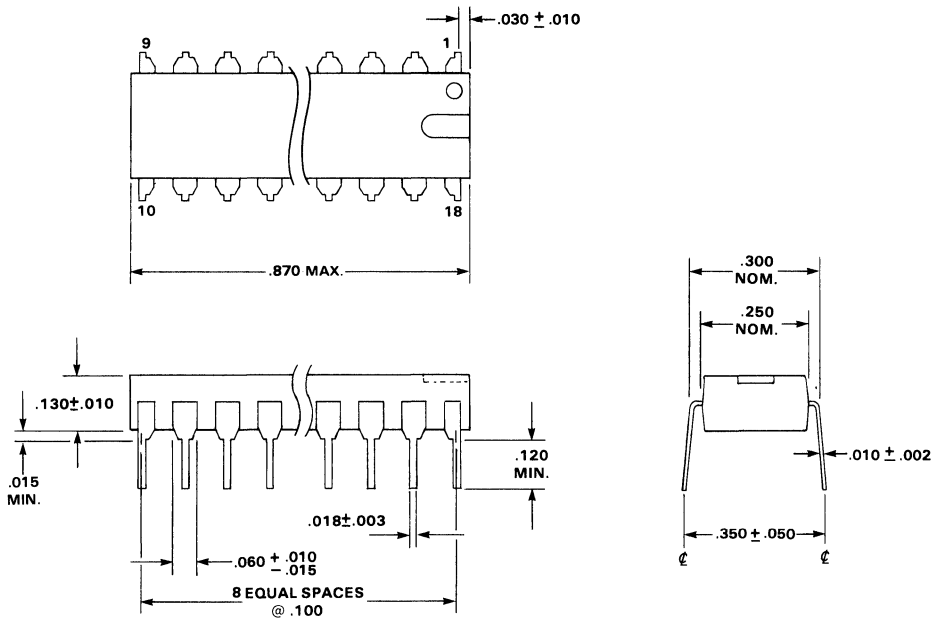
AC Characteristics - Pulse Mode Operation

NO.	SYM	PARAMETERS	MIN	TYP	MAX	UNITS	NOTES
—	P_R	Pulse Rate		10		PPS	1
5	PDP	Predigital Pause		48		ms	2
6	IDP	Interdigital Pause		740		ms	2
7	T_{MO}	Mute Overlap Time		2		ms	2
8	T_B	Break Time		60		ms	2
9	T_M	Make Time		40		ms	2

NOTES
1. 10 PPS is the nominal rate.
2. Figure 8 illustrates this relationship.

PACKAGE DESCRIPTION

18-Pin DIP (N) (.300)
Plastic



NOTE: Overall length includes .010 flash on either end of package

FEATURES

- ☐ Single chip DTMF and pulse dialer.
- ☐ Stores 10 18-digit telephone numbers, including last number dialed.
- ☐ Softswitch changes signaling mode from pulse to tone.
- ☐ Single button redial of all ten memories.
- ☐ Flash key input initiates timed hook flash.
- ☐ 8 Tones Per Second dialing in Tone Mode and 10 PPS in Pulse Mode.
- ☐ DTMF active until key release.
- ☐ Minimum DTMF duration/separation guaranteed (74/54 ms).
- ☐ Pacifier tone provides audible indication of a valid key input for non-DTMF key entries.
- ☐ Powered from telephone line, low operating voltage for long loop applications.

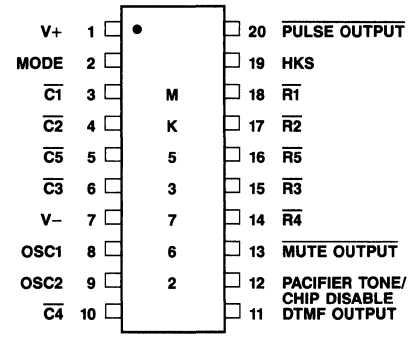


Figure 1. Pin Connection

1	2	3	FLASH	MEM 9
4	5	6	PROG	MEM 8
7	8	9	PAUSE	MEM 7
* SOFTSWITCH	0	#	LND	MEM 6
MEM 1	MEM 2	MEM 3	MEM 4	MEM 5

Figure 2. Keypad Configuration

DESCRIPTION

The MK53762 is a Mostek Silicon Gate CMOS IC that provides necessary signals for either DTMF or loop disconnect (pulse) dialing. The MK53762 buffers up to 18 digits into memory that can be later redialed with a single key input. Up to nine repertory numbers may be stored. Users can store all 12 signaling keys and access several unique functions with single key entries. These functions include: Last Number Dialed (LND), Softswitch, Flash, and 9 memories. Figure 2 shows the keypad configuration.

A LND key input automatically redials the last number dialed, and the MEM keys provide single key access to all memory locations for auto-dialing.

The FLASH key simulates a 560 ms hook flash to transfer calls or to activate other special features provided by the PABX or a central office.

The PAUSE key allows the user to insert a delay in dialing for functions such as the pause in accessing an outside line when redialing from a PABX.

The PROG key provides an easy way to program a number into any memory location (MEM 1 - MEM 9) whether on-hook or off-hook.

FUNCTIONAL PIN DESCRIPTION

V+
Pin 1. V+ is the positive supply for the circuit and must meet the maximum and minimum voltage requirements. (See Electrical Specifications.)

MODE
Input. Pin 2. MODE determines the dialer's default operating mode. When the device is powered up or the hookswitch input is switched from on-hook, (V+), to off-hook, (V−), the default determines the signaling mode. A V+ connection defaults to tone mode operation and a V− connection defaults to pulse mode operation.

When dialing in the pulse mode, a softswitch feature will allow a change to the tone mode whenever the * key, or softswitch, is depressed. Subsequent * key inputs will cause the DTMF code for an * to be dialed. The softswitch will only switch from pulse to tone. After returning to on-hook and back to off-hook, the part will be in pulse mode. Redial by the LND key will repeat the softswitch.

$\overline{C1}$, $\overline{C2}$, $\overline{C3}$, $\overline{C4}$, $\overline{C5}$, $\overline{R5}$, $\overline{R4}$, $\overline{R3}$, $\overline{R2}$, $\overline{R1}$
Keyboard inputs. The MK53762 interfaces with either the standard 2-of-10 with negative common or the single-contact (Form A) keyboard.

A valid keypad entry is either a single Row connected to a single Column or V− simultaneously presented to both a single Row and Column. In its quiescent or standby state, during normal off-hook operation, either the Rows or the Columns are at a logic level 1 (V+). Pulling one input low enables the on-chip oscillator. Keyboard scanning then begins. Scanning consists of Rows and Columns alternately switching high through on-chip pullups. After both a Row and Column key have been detected, the debounce counter is enabled and any noise (bouncing contacts, etc.) is ignored for a debounce period (T_{KD}) of 32 ms. At this time, the keyboard is sampled and if both Row and Column information are valid, the information is buffered into the LND location. If switched on-hook (pin 19 to pin 1), the keyboard inputs all pull high through on-chip pullup resistors.

In the tone mode, if 2 or more keys in the same row or column are depressed a single tone will be output. The tone will correspond to the row or column for which the 2 keys were pushed. This feature is for test purposes.
Single tones will not be redialed.

Also in the tone mode, the output tone is continuous in manual dialing as long as the key is pushed. The output tone duration follows the table below:

Table 1. Output Tone Duration

KEY-PUSH TIME, T*	TONE OUTPUT*
$T \leq 32$ ms	No output. Ignored by MK53762.
32 ms $\leq T \leq 75$ ms $+T_{KD}$	75 ms duration output.
$T \geq 75$ ms + T_{KD}	Output duration = T − T_{KD}

*NOTE: T_{KD} is the key pad debounce time which is typically 32 ms.

When redialing in the tone mode, each DTMF output is 75 ms duration, and the tone separation (intersignal delay) is 50 ms.

V−
Input. Pin 7 is the negative supply input to the device. This is the voltage reference for all specifications.

OSC1, OSC2
Pin 8 (input), pin 9 (output). OSC1 and OSC2 are connections to an on-chip inverter used as the timing reference for the circuit. It has have sufficient loop gain to oscillate when used with a low-cost television color-burst crystal. The nominal crystal frequency is 3.579545 MHz and any deviation from this standard is directly reflected in the Tone output frequencies. The crystal oscillator provides the time reference for all circuit functions. A ceramic resonator with tolerance of ±0.25% may also be used.

DTMF OUTPUT
Output. Pin 11. An NPN transistor emitter with a collector tied to V+ drives the DTMF OUTPUT pin. The transistor base is connected to an on-chip operational amplifier that mixes the Row and Column tones. Figure 7 shows the timing at this pin.

The DTMF OUTPUT is the summation of a single Row frequency and a single Column frequency. A typical single tone sine wave is shown in Figure 4. This waveform is synthesized using a resistor tree with sinusoidally weighted taps.

The MK53762 is designed to operate from an unregulated supply; the TONE LEVEL is supply independent, and the single row tone output level will be typically:

$$T_{oi} = -12 \text{ dBm} \pm 1 \text{ dB}$$

The DC component of the DTMF output while active is described by the following equation:

$$V_{DC_1} = 0.3\ V+ + 0.5 \text{ Volts}$$

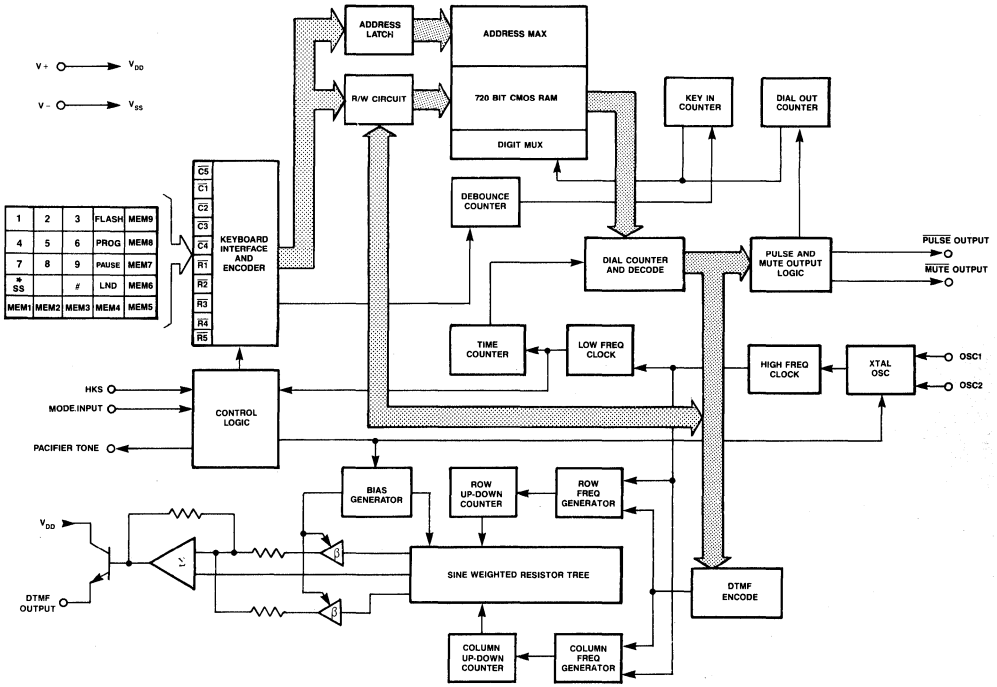


Figure 3. MK53762 Functional Block Diagram

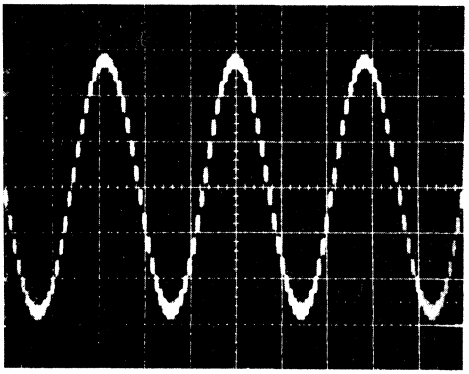


Figure 4. Typical Single Tone

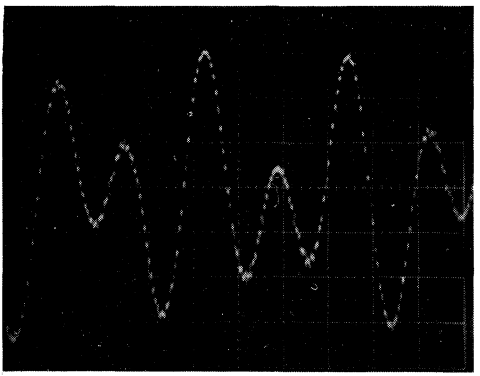


Figure 5. Typical Dual Tone

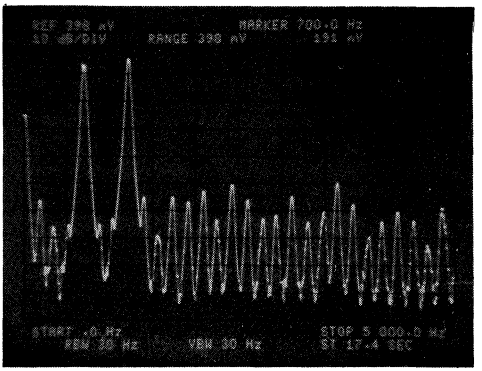


Figure 6. Typical Spectral Response

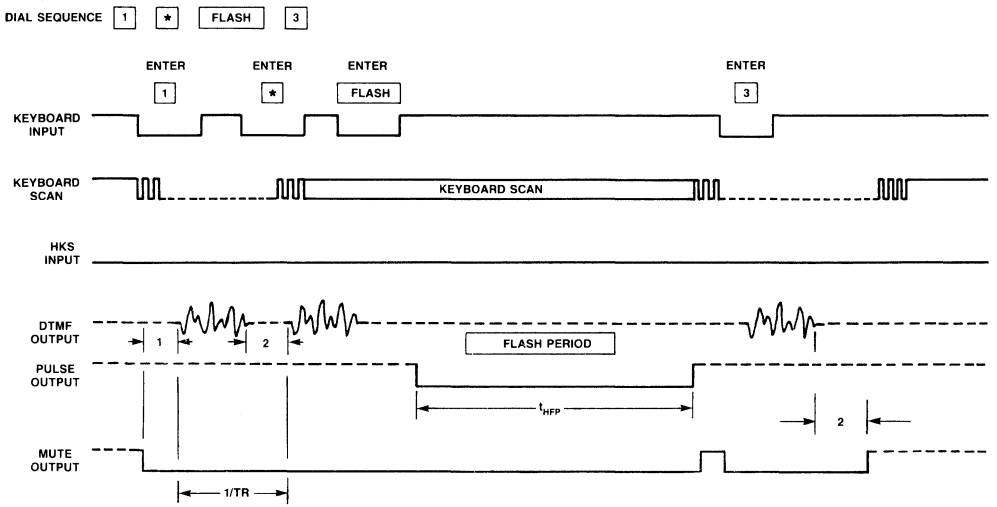
PACIFIER TONE OUTPUT/CHIP DISABLE INPUT

Pin 12. PAC tone is an output. The pacifier tone provides audible feedback, confirming that the key has been properly entered and accepted. A 500 Hz square wave is activated upon acceptance of a valid key input, after the 32 ms debounce time. The square wave terminates after a maximum of 30 ms or when the valid key is no longer present. In pulse mode, all key entries activate the pacifier tone. In tone mode, any non-DTMF key (LND, FLASH, MEM, PROG) entry activates the pacifier tone. When programming the chip, all valid key entries activate the pacifier tone in either pullse or tone mode.

The CHIP DISABLE is an input. When pin 12 is switched low through a resistor (10K to 100K), the MK53762 is enabled. When pin 12 is switched to V+ through the resistor, all keypad inputs are pulled high, and the MK53762 will ignore all keypad inputs. When the chip is disabled, it will not dial, and it cannot be programmed. The chip will only be disabled when the circuit is inactive (not dialing) and Pin 12 is switched high.

Table 2. DTMF Output Frequency

KEY INPUT		STANDARD FREQUENCY	ACTUAL FREQUENCY	% DEVIATION
ROW	1	697	699.1	+0.31
	2	770	766.2	−0.49
	3	852	847.4	−0.54
	4	941	948.0	+0.74
COL	1	1209	1215.9	+0.57
	2	1336	1331.7	−0.32
	3	1477	1471.9	−0.35



NOTE:

1. For this example, key entries are ≤75 ms, but ≥32 ms.
2. $\overline{\text{MUTE}}$ goes active after any key is depressed.

Figure 7. Tone Mode Timing

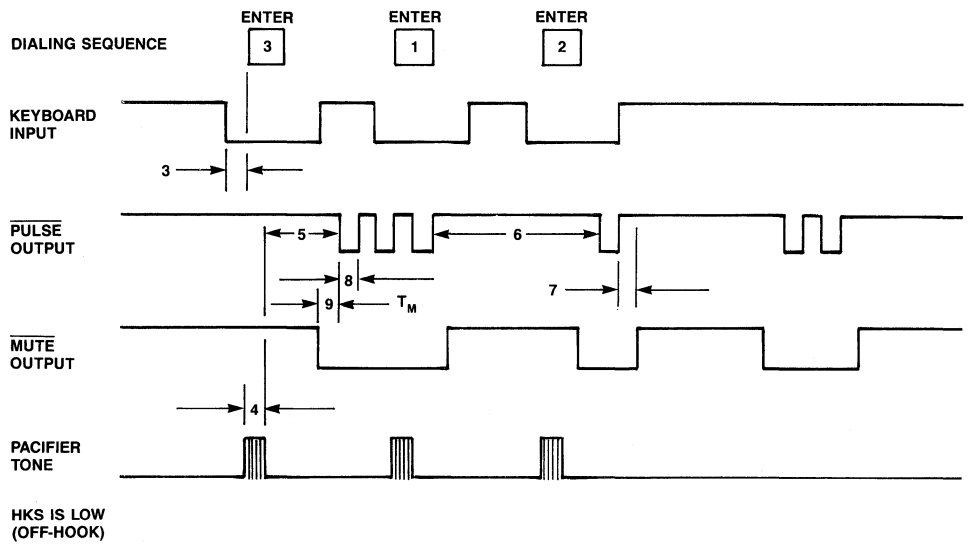


Figure 8. Pulse Mode Timing

MUTE OUTPUT

Output. Pin 13. This pin is the $\overline{\text{MUTE OUTPUT}}$ for both tone and pulse modes. Timing is dependent upon mode.

The $\overline{\text{MUTE OUTPUT}}$ consists of an open drain N-channel device. During standby, the output is high impedance and generally has an external pullup resistor to the positive supply.

In the tone mode, $\overline{\text{MUTE OUTPUT}}$ is used to remove the transmitter and the receiver from the network during DTMF signaling. During dialing, $\overline{\text{MUTE OUTPUT}}$ is active continuously until dialing is completed. $\overline{\text{MUTE OUTPUT}}$ goes active when any key is pushed.

In the pulse mode, $\overline{\text{MUTE OUTPUT}}$ is used to remove the receiver and the network from the line. Different circuitry is required for tone and pulse muting external to the IC and applications using both modes would not necessarily share circuitry. $\overline{\text{MUTE OUTPUT}}$ timing is shown in Figure 8 for pulse mode signaling and Figure 7 for tone mode signaling. $\overline{\text{MUTE OUTPUT}}$ is active during each digit, and not active during the interdigit time. In both tone and pulse modes, $\overline{\text{MUTE OUTPUT}}$ goes active 40 ms before $\overline{\text{PULSE OUTPUT}}$ for a FLASH.

HKS

Input. Pin 19. Pin 19 is the hookswitch input to the MK53762. This is a high-impedance input and must be switched high for on-hook operation or low for off-hook operation. A transition on this input causes the on-chip logic to initialize, terminating any operation in progress at the time. The signaling mode defaults to the mode selected at pin 2. Figure 8 illustrates the timing for this pin.

$\overline{\text{PULSE OUTPUT}}$

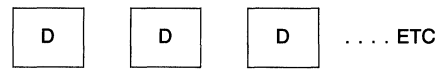
Output. Pin 20. This is an output consisting of an open drain N-channel device. In either pulse or tone mode, the FLASH key will cause a 560 ms output pulse at pin 20.

DEVICE OPERATION

When the MK53762 is not actively dialing, it consumes very little current. Row and Column inputs assume opposite states off-hook. The circuit verifies that a valid key has been entered by alternately scanning the Row and Column inputs. If the input is still valid following 32ms of debounce, the digit is stored into memory, and dialing begins after a pre-signal delay of approximately 40 ms (measured from initial key closure). Output tone duration is shown in Table 1.

The MK53762 allows manual dialing of an indefinite number of digits, but if more than 18 digits are dialed per number, the 53762 will "wrap around". That is, the extra digits beyond 18 will be stored at the beginning of the LND buffer, and the first 18 digits will no longer be available for redial. During autodial from LND or any MEM location, key inputs are not accepted, but they will suspend dialing until released.

NORMAL DIALING (Off-Hook)

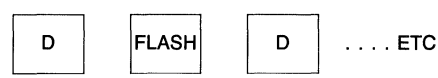


Normal dialing is straightforward, all keyboard entries will be stored in the buffer and signaled in succession.

LAST NUMBER DIALED (LND)

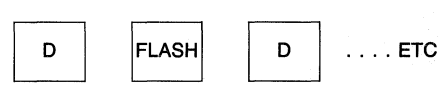
Last number dialing is accomplished by entering the LND key.

HOOK FLASH



Hook flash may be entered into the dialed sequence at any point by keying in the function key, FLASH. Flash consists of a timed Break of 560ms. The FLASH function is stored in memory, but it will not be redialed as such. When a FLASH key is pressed, no further key inputs will be accepted until the hookflash function (560 ms break) has been dialed. The key input following a FLASH will be stored as the initial digit of a new number (overwriting the number dialed prior to the FLASH) unless it is another FLASH. Consecutive FLASH entries after a number is dialed will be stored sequentially in the LND memory and a subsequent LND entry will cause the redial of that number with a delay, but not hookflash breaks, at the end of the redialing sequence. When redialing in tone mode, $\overline{\text{MUTE OUTPUT}}$ will remain active during the flash delay period.

PAUSE



A Pause may be entered into the dialed sequence at any point by keying in the special function key, PAUSE. Pause inserts a 1.1-second delay into the dialing sequence. The total delay, including pre-digital and post-digital pauses is shown in Table 3.

SOFTSWITCH

When dialing in the pulse mode, a softswitch feature will allow a change to the tone mode whenever the * key is depressed. Subsequent * inputs will cause the DTMF code for an * to be dialed. The softswitch will only switch from pulse to tone. After returning to on-hook and back to off-hook, the part will be in pulse mode. Redial by the LND key will repeat the softswitch.

PROGRAMMING AND REPERTORY DIALING

Programming is independent of HKS (pin 19) and MODE (pin 2).

To program, enter the following:
PROG, Digit 1, Digit 2, ... , MEM (Location 1-9).
When programming, dialing is inhibited.

To dial a number from repertory memory (HKS must be low) enter the single key:
MEM (Location 1-9)

To save the last number dialed: PROG, MEM (Location 1-9).

Table 3. Special Function Delays

Each delay shown below represents the time required from after the special function key is depressed until a new digit can be dialed.

The time is considered "FIRST" key is all previous inputs have been completed dialed. The time is considered "AUTO" if in redial, or if previous dialing is still in progress.

FUNCTION	FIRST/AUTO	DELAY (seconds)	
		PULSE	TONE
SOFTSWITCH	FIRST	0.40	—
	AUTO	1.10	—
PAUSE	FIRST	1.84	1.15
	AUTO	2.50	1.20

Absolute Maximum Ratings*

DC Supply Voltage ..... 6.5 Volt
Operating Temperature ..... 0°C to +60°C
Storage Temperature ..... −55°C to +125°C
Maximum Power Dissipation (25°C) ..... 500 mW
Maximum Voltage on any Pin ..... (V+)+.3, (V−)−.3

* All specifications are for 2.5 Volt operation and full operating temperature range unless otherwise stated.

ELECTRICAL CHARACTERISTICS
DC Characteristics

SYM	PARAMETER	MIN	TYP	MAX	UNIT	NOTES
V+ TONE	DC Operating Voltage (Tone Mode)	2.5		6.0	Volts	
V_{MR}	Memory Retention Voltage	1.5	1.3		Volts	1, 6
I_s	Standby Current		0.4	1.0	μA	1
I_{MR}	Memory Retention Current		0.15	0.75	μA	5, 6
V_{MUTE}	Mute Output Operating Voltage	1.8			Volts	7
I_T	Operating Current (Tone)		300	600	μA	2
I_P	Operating Current (Pulse)		150	250	μA	2
	Operating Current On-Hook Program Mode Key Operated No-Key Operated			 200 1	 μA μA	
I_{ML}	Mute Output (2.5 Volts) Sink Current (4.0 Volts)	1.0 3.0			mA mA	3
I_{PL}	Pulse Output Sink Current	1.0	2.0		mA	3
I_{PC}	Pacifier Tone Sink/Source	250	500		μA	4
K_{RU}	Keypad Pullup Resistance		100		kohm	
K_{RD}	Keypad Pulldown Resistance		500		ohm	
V_{IL}	Keypad Input Level-Low	0		0.3V+	Volt	
V_{IH}	Keypad Input Level-High	0.7V+		V+	Volt	
V_{PULSE}	Operating Voltage (Pulse Mode)	1.8		6.0	Volts	

NOTES
1. All inputs unloaded, Quiescent Mode (oscillator off)
2. All outputs unloaded, single key input
3. V_{OUT} = 0.4 Volts
4. Sink Current for V_{OUT} = 0.5 volts, Source Current for V_{OUT} = 2.0 Volts
5. Memory Retention Voltage is the point where memory is guaranteed but circuit operation is not.
6. Proper memory retention is guaranteed if either the minimum I_{MR} is provided or the minimum V_{MR}. The design does not have to provide both the minimum current or voltage simultaneously.
7. Minimum voltage where activation of mute output with key entry is ensured.

AC Characteristics - Tone Mode

NO.	SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
—	T_{NK}	Tone Output No Key Down			−80	dBm	1
—	T_{Oi}	Tone Output (independent)	−13 173	−12 194	−11 218	dBm mV_{rms}	1, 2 3
—	PE_i	Pre-Emphasis, High Band	1.6	2.0	2.4	dB	
—	DC_i	Tone Output DC Bias (V+ = 2.5) (V+ = 3.5)	 1.2	1.0		Volts Volts	
—	R_E	Tone Output Load		10		kohm	4
—	T_{RIS}	Tone Output Rise Time		1.0		ms	5
—	DIS	Output Distortion		5.0	8.0	%	3
—	TR	Tone Signaling Rate		8.0		1/sec	
1	T_{PSD}	Pre-Signal Delay	40			ms	6
2	T_{ISD}	Inter-Signal Delay (repertory)		54		ms	
	T_{DUR}	Tone Output Duration (repertory)		74		ms	

NOTES

1. O dBm equals 1 mW power into 600 ohms or 775 mVolts.
   Important Note: The MK53762 is designed to drive a 10 kohm load. The 600 ohm load is only for reference.
2. Single tone (low group), as measured at pin 10, T_A = 25°C.
3. Supply voltage = 2.5 to 6 Volts, R_E=10 kohms.
4. Supply voltage = 2.5 Volts. These specifications are supply-dependent.
5. Time from beginning of tone output waveform to 90% of final magnitude of either frequency. Crystal parameters suggested for proper operation are R_s<100 ohms, L_m=96 mH, C_m=0.02 pF, C_h=5pF, f=3.579545 MHz, and C_L=18 pF.
6. Time from initial key input until beginning of signaling.

AC Characteristics - Keypad Inputs, Pacifier Tone

(Numbers in left hand column refer to the timing diagrams.)

NO.	SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
3	T_{KD}	Keypad Debounce Time		32		ms	1
—	F_{KS}	Keypad Scan Frequency		250		Hz	1
—	F_{PT}	Frequency Pacifier Tone		500		Hz	1
4	T_{PT}	Pacifier Tone Duration		30		ms	1
—	T_{HFP}	Hookflash Timing		560		ms	1

NOTES
1. Crystal oscillator accuracy directly affects these times.

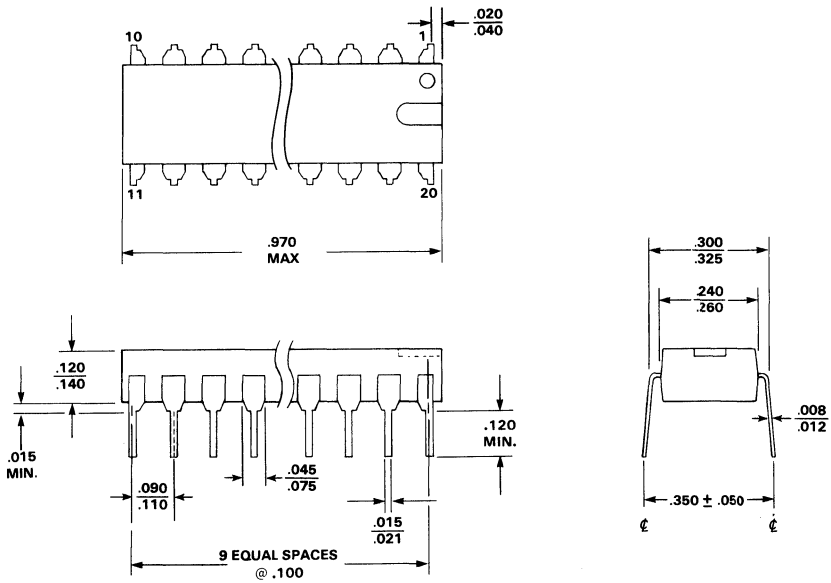
AC Characteristics - Pulse Mode Operation

NO.	SYM	PARAMETERS	MIN	TYP	MAX	UNITS	NOTES
—	P_R	Pulse Rate		10		PPS	1
5	PDP	Predigital Pause		48		ms	2
6	IDP	Interdigital Pause		740		ms	2
7	T_{MO}	Mute Overlap Time		2		ms	2
8	T_B	Break Time		60		ms	2
9	T_M	Make Time		40		ms	2

NOTES
1. 10 PPS is the nominal rate.
2. Figure 8 illustrates this relationship.

PACKAGE DESCRIPTION

20-Pin DIP (N) (.300)
Plastic



NOTE: Overall length includes .010 flash on either end of package

FEATURES

- ☐ Storage of thirteen 18-digit numbers: 3 EMERGENCY locations, and 10 additional locations including LNR (Last Number Redial).
- ☐ All locations can be accessed with single key inputs although the option is available to access 3 EMERGENCY locations plus LNR directly and two keys (MEM key plus key 1-9) to access the 9 other memories.
- ☐ Two select pins allow user to select 16 different country options.
- ☐ Single chip, mixed mode dialer allows dialing in either tone or pulse modes. A * or "SOFT-SWITCH" key input can also be used to switch from Pulse to Tone mode operation and is stored in memory.
- ☐ P.I.N. (Personal identity number) protection method
- ☐ Sliding cursor method to simplify PABX dialing.
- ☐ Hookswitch debounce, transients due to line reversals and drop-outs can be masked for a period determined by external RC.
- ☐ Powered from telephone line, low standby current and operating voltage.
- ☐ DTMF signal consistent with key entry period.
- ☐ Minimum DTMF signal duration/separation guaranteed.
- ☐ Timed PABX pause may be stored in Memory.
- ☐ Timed FLASH for extended timed Break.

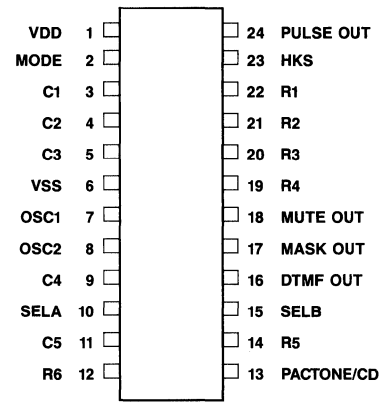


Figure 1. MK53763 Pinout

1	2	3	FLASH	M9
4	5	6	PROG	M8
7	8	9	PAUSE	M7
*	0	#	LNR	M6

M1	M2	M3	M4	M5
E1	E2	E3	MEM	SS

Figure 2. MK53763 Keypad Configuration

MK53761 TYPICAL APPLICATION

The MK53761 is a single chip TonePulse™ repertory dialer with nine 18-digit memories plus redial, which provides the necessary signals for DTMF (tone) or loop disconnect (pulse) dialing. When manually dialing, the MK53761 buffers up to 18 digits into memory for later redial with a single LND key input. The user can dial and store all 12 signaling digits plus access several unique functions. These functions include: Last Number Dialed (LND), Softswitch, Flash, and 9 memories (MEM 1 - 9).

The typical application circuit shown in Figure 1 illustrates one way the MK53761 TonePulse™ dialer can be used in a typical telephone. The circuit is connected to the telephone line through a diode bridge to assure proper voltage polarity to the circuit regardless of the polarity of the telephone line. Transistor Q2, resistor R2, and zener diode Z1 are used to regulate the voltage supplied to the MK53761 to provide proper device operation regardless of the voltage at the telephone line. The 2-to-4 wire conversion and interface to transmitter and receiver is accomplished using a 2500 type speech network.

In this circuit, Pulse dialing (which consists of a series of momentary interruptions of loop current) is achieved by the Pulse output controlling transistors Q3 and Q4 to break and make the loop current through the speech network. The Mute output, controlling transistors Q5 and Q7, mutes the transmitter and receiver to eliminate the loud pops which would otherwise be heard in the receiver due to the pulsing of the loop current through the speech network.

Tone signaling requires that the loop current be modulated with the appropriate DTMF signal. The DTMF output of the MK53761 drives transistor Q8 to modulate the telephone loop current through resistor R4. The signal level present at the telephone line can be varied by changing the value of R4. The Mute output controls transistors Q5 and Q7 to remove the transmitter and mute the receiver. This is done to eliminate any interference of the DTMF signal from the transmitter, and to reduce to an acceptable level the tone heard at the receiver.

The mode of operation (Tone or Pulse) is controlled by switch S1. In Pulse Mode, the Softswitch key (* key) can be used to change from Pulse to Tone Mode. Hanging-up and going back off-hook will cause the MK53761 to revert back to the mode selected by the S1, but the Softswitch function can be redialed. The signalling mode may be changed at any time, so as to allow mixed Pulse and Tone dialing. This feature is very useful when trying to access special services requiring tones, from a pulse-only system.

Resistor R1 provides a small memory-retention bias current to prevent the device from losing power while on hook. The current required for long term memory retention is less than 1 μA. A 3V lithium battery is used to supply power for on-hook programming, and to assure long term memory retention regardless of whether or not the circuit is connected to the telphone line. A battery is not required if programming is restricted to occurring only when off-hook. On-hook programming can be disabled by simply connecting R13 from pin 11 to pin 17 (instead of from pin 11 to pin 6) to cause the MK53761 to be disabled when hanging up.

A ceramic sounder can be interfaced to Pin 11 (Pacifier Tone) of the device. A pacifier tone signal is activated for each key entry which would not otherwise produce a tone (pulse dialing, redial commands, etc.). This audible feedback confirms proper key entry.

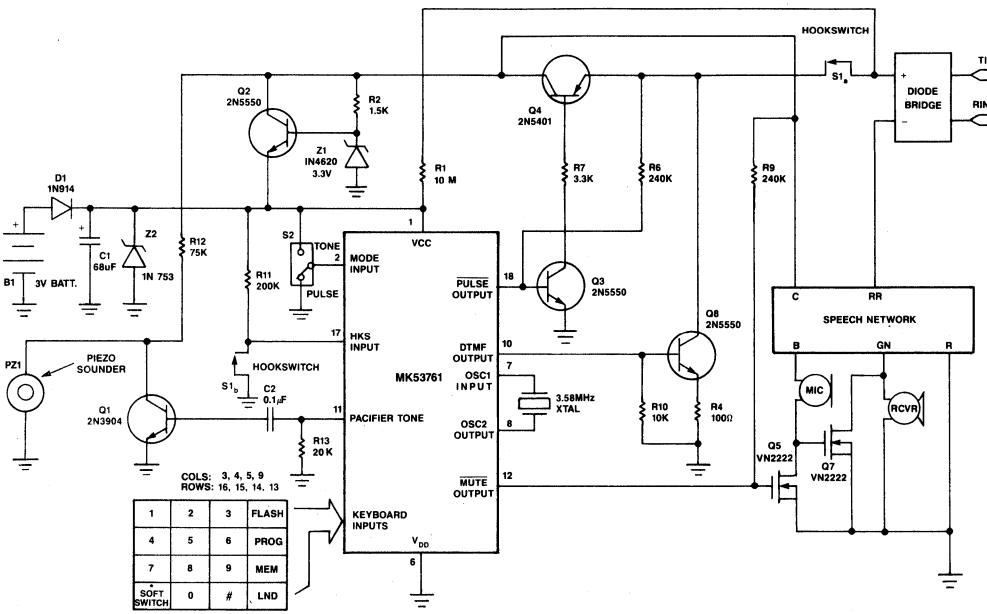

HOOKSWITCH
TIP
RING
DIODE BRIDGE
Q2 2N5550
R2 1.5K
Z1 IN4620 3.3V
Q4 2N5401
R1 10 M
R7 3.3K
R6 240K
R9 240K
D1 1N914
B1 3V BATT.
C1 68uF
Z2 1N 753
R12 75K
R11 200K
S2
TONE
PULSE
VCC
MODE INPUT
HKS INPUT
PULSE OUTPUT
DTMF OUTPUT
OSC1 INPUT
OSC2 OUTPUT
MUTE OUTPUT
KEYBOARD INPUTS
MK53761
Q3 2N5550
Q8 2N5550
C
RR
SPEECH NETWORK
B
GN
R
MIC
RCVR
PZ1
PIEZO SOUNDER
HOOKSWITCH
C2 0.1μF
Q1 2N3904
PACIFIER TONE
R13 20 K
3.58MHz XTAL
R10 10K
R4 100Ω
Q5 VN2222
Q7 VN2222
COLS: 3, 4, 5, 9
ROWS: 16, 15, 14, 13
1 2 3 FLASH
4 5 6 PROG
7 8 9 MEM
SOFT SWITCH 0 # LND

Figure 1.

MK53762 TYPICAL APPLICATION

The MK53762 is a single chip TonePulse™ repertory dialer with nine 18-digit memories plus redial, which provides the necessary signals for DTMF (tone) or loop disconnect (pulse) dialing. When manually dialing, the MK53762 buffers up to 18 digits into memory for later redial with a single LND key input. The user can store all 12 signaling digits plus access several unique functions with single key entries. These functions include: Last Number Dialed (LND), Softswitch, Flash, and 9 memories (MEM 1 - 9).

The typical application circuit shown in Figure 1 illustrates one way the MK53762 TonePulse™ dialer can be used in a typical telephone. The circuit is connected to the telephone line through a diode bridge to assure proper voltage polarity to the circuit regardless of the polarity of the telephone line. Transistor Q2, resistor R2, and zener diode Z1 are used to regulate the voltage supplied to the MK53762 to provide proper device operation regardless of the voltage at the telephone line. The 2-to-4 wire conversion and interface to transmitter and receiver is accomplished using a 2500 type speech network.

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The mode of operation (Tone or Pulse) is controlled by switch S1. In Pulse Mode, the Softswitch key (* key) can be used to change from Pulse to Tone Mode. Hanging-up and going back off-hook will cause the MK53762 to revert back to the mode selected by the S1, but the Softswitch function can be redialed. The signalling mode may be changed at any time, so as to allow mixed Pulse and Tone dialing. This feature is very useful when trying to access special services requiring tones, from a pulse-only system.

Resistor R1 provides a small memory-retention bias current to prevent the device from losing power while on hook. The current required for long term memory retention is less than 1 μA. A 3V lithium battery is used to supply power for on-hook programming, and to assure long term memory retention regardless of whether or not the circuit is connected to the telphone line. A battery is not required if programming is restricted to occurring only when off-hook. On-hook programming can be disabled by simply connecting R13 from pin 12 to pin 19 (instead of from pin 12 to pin 7 to cause the MK53762 to be disabled when hanging up.

A ceramic sounder can be interfaced to Pin 12(Pacifier Tone) of the device. A pacifier tone signal is activated for each key entry which would not otherwise produce a tone (pulse dialing, redial commands, etc.). This audible feedback confirms proper key entry.

For further information and specifications on the MK53762 please consult the MK53762 Data Sheet.

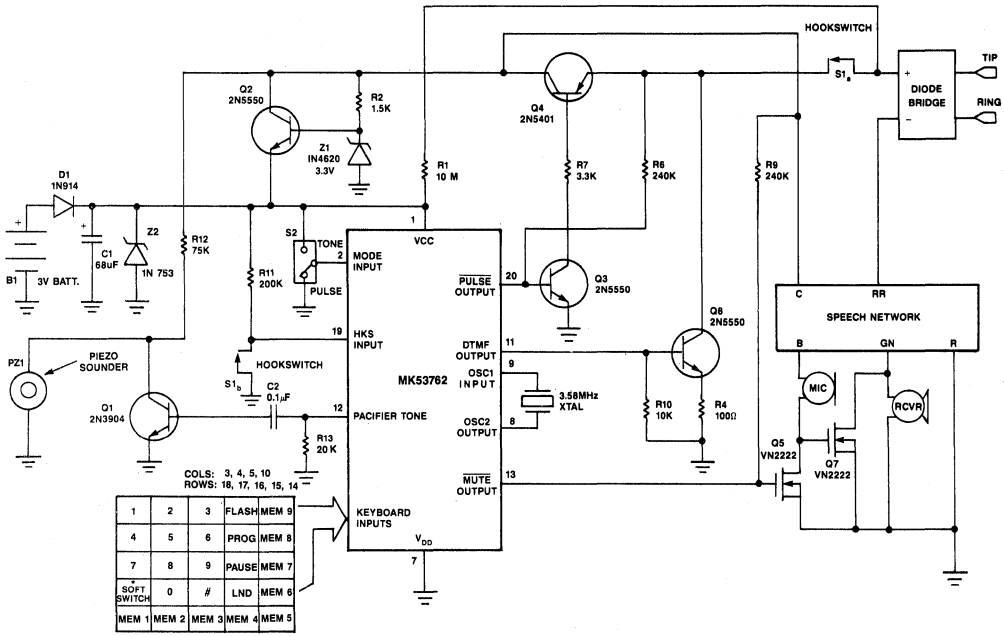

HOOKSWITCH
TIP
RING
DIODE BRIDGE
Q2 2N5550
R2 1.5K
Z1 IN4620 3.3V
Q4 2N5401
R1 10 M
R7 3.3K
R6 240K
R9 240K
D1 1N914
B1 3V BATT.
C1 68uF
Z2 1N 753
R12 75K
R11 200K
S2
TONE
PULSE
VCC
MODE INPUT
PULSE OUTPUT
Q3 2N5550
SPEECH NETWORK
C
RR
B
GN
R
Q8 2N5550
PZ1
PIEZO SOUNDER
HOOKSWITCH
HKS INPUT
DTMF OUTPUT
OSC1 INPUT
MK53762
3.58MHz XTAL
MIC
RCVR
Q1 2N3904
C2 0.1µF
PACIFIER TONE
OSC2 OUTPUT
R10 10K
R4 100Ω
R13 20 K
Q5 VN2222
Q7 VN2222
COLS: 3, 4, 5, 10
ROWS: 18, 17, 16, 15, 14
MUTE OUTPUT
KEYBOARD INPUTS
VDD
1 2 3 FLASH MEM 9
4 5 6 PROG MEM 8
7 8 9 PAUSE MEM 7
SOFT SWITCH 0 # LND MEM 6
MEM 1 MEM 2 MEM 3 MEM 4 MEM 5

Figure 1.

APPLICATION NOTE

MK5375 TYPICAL APPLICATIONS

MK5375 TYPICAL APPLICATIONS
NO BATTERY BACK-UP & CONTINUOUS TONE

The MK5375 is a very versatile TonePulse™ dialer product which can be used in a wide variety of applications. There are however two applications questions which arise very frequently.

1) Is a battery necessary for memory retention and on-hook storage operations?
2) Is it possible to make the MK5375 generate continuous tone for the length of a key depression?

This application note will discuss how an MK5375 application circuit can be designed to operate without a battery for storage operations and memory retention, as well as generate a continuous tone for the length of the key closure.

The MK5375 was designed so that normal dialing and auto-dialing should take place while off hook, and programming operations should take place while on-hook. This, as well as long term memory retention, typically requires a battery, which is objectionable to some telephone circuit manufacturers. There are however methods for accomplishing off-hook programming by placing the MK5375 in its on-hook mode (HKS, pin 17, to V+) while the telephone circuit is still off hook and drawing telephone line current. The minimal memory retention current required by the MK5375 (200 nA typ.) can also be supplied from the telephone line through a very large resistor, and with a large capacitor to maintain the memory for the time that the telphone may be disconnected.

In the application circuit shown in Figure 1, a Program/Normal switch (S4) is used to place the MK5375 in the "Program" mode by taking HKS (pin 17) to V+ (pin 1), to allow for programming numbers into the 9 memory locations while off-hook. The Pacifier Tone/Chip Disable (pin 11) is connected to hookswitch S2 (through load resistor R4) so that the MK5375 will be disabled (pin 11 to V+) when on hook. This is done so that the memory will not be lost due to the increased current consumption of trying to program with the limited on-hook current supply. In this application circuit, memory retention current is supplied from the telephone line through a diode bridge (to insure correct polarity) and a 15 M Ω resistor, with a 5.1 V zener diode (Z2) to limit the voltage across the MK5375. A 100 μF capacitor is used to maintain the MK5375 memory during any small amounts of time (30 minutes typ.) that the telephone may be disconnected. Therefore, by adding a switch and a resistor, and by increasing the value of a capacitor, the need for a battery can be eliminated.

An important feature of the MK5375 is that all of timing pulse dialing and tone output rate is controlled by an RC oscillator whose values may be varied to achieve a wide variety of signalling rates. It is this RC oscillator that determines the length and interdigit time for each output tone burst. Therefore to achieve a continuous tone, the RC oscillator must be stopped while that tone is being output. The tone will then remain until the RC oscillator is allowed to continue running and complete the burst time. The solution to getting a continuous tone for the length of a key closure requires some method of stopping the RC oscillator for the duration of the key closure, once the key entry has been debounced and decoded.

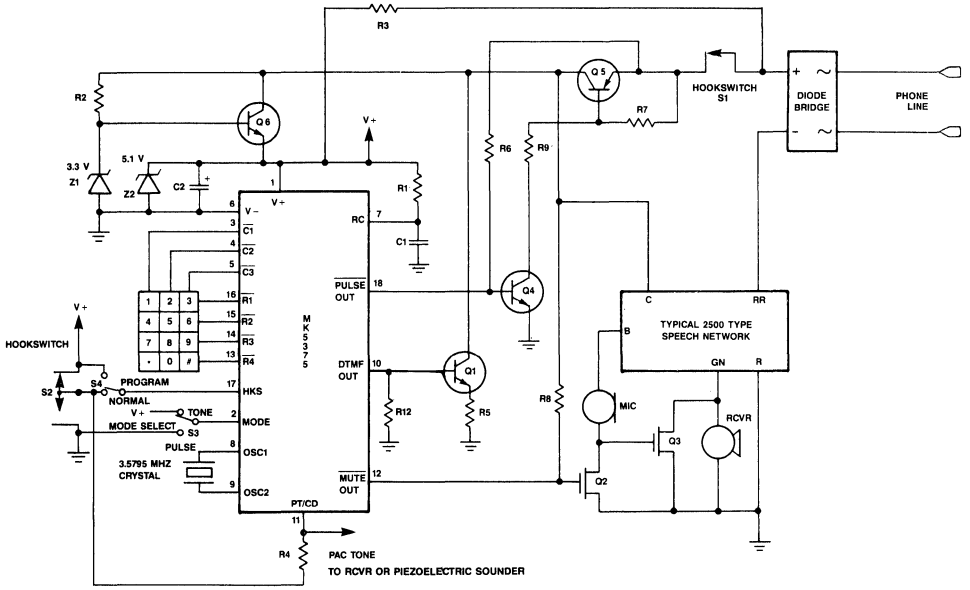
In the Figure 2 application circuit, a single transistor circuit (Q7, R14, R15 & C3) is used to stop the RC oscillator once a key entry has been debounced, decoded, and the output tone burst has begun. A keyboard with a common connection is used because whenever a row is connected to a column, that node is pulled low through the MK5375 keyboard input circuitry, so that the keyboard common will be normally open and go low when any key is pressed. Once a key entry has been debounced and decoded, the DTMF output will go high (to a DC level about which the output signal will be generated), thus turning on transistor Q7 and pulling the RC oscillator input (pin 7) low through the keyboard common. This will stop the RC oscillator, which will cause the DTMF signal to remain until the key is released. When the key is released, the keyboard common will be open and the RC oscillator will resume running until the remainder of the tone burst time is completed. Since the RC determined tone burst time (100 ms using standard values) is added on to the time that the key is held low after debounce, the RC period must be decreased to allow for rapid key entry. To do this, an extra resistor (R13) is added in parallel to R1, and another pole of Mode Switch S3 is used to revert to the standard RC values for the nominal 10 PPS pulse dialing rate.

Aside from the minor circuit additions discussed, both application circuits are standard MK5375 TonePulse™ switchable, 10-number repertory dialer circuits. Both circuits are telephone line powered, using a diode bridge to insure proper line polarity, and a voltage regulator circuit comprised of transistor Q6, resistor R2, and zener diode Z1. The rate at which dialing occurs is determined by the values of resistor R1 and capacitor C1, which are the timing components for the RC oscillator. The 3.5795 MHz crystal is used as a reference for synthesizing the DTMF signals and is activated only for the short periods during which these tones are being generated.

Pulse dialing (which consists of a series of momentary interruptions of loop current) is achieved by the Pulse output controlling transistors Q4 and Q5 to break and make the loop current through the speech network.The Mute output, controlling transistors Q2 and Q3, mutes the transmitter and receiver to eliminate the loud pops which would otherwise be heard in the receiver due to the pulsing of the loop current through the speech network.

Tone signalling requires that the loop current be modulated with the appropriate DTMF signal. The DTMF output of the MK5375 drives transistor Q1 to modulate the telephone loop current through resistor R5. The signal level present at the telephone line can be varied by changing the value of R5. The Mute output controls transistors Q2 and Q3 to remove the transmiter and mute the receiver. This is done to eliminate any interference of the DTMF signal from the transmitter, and to reduce the level of tone heard at the receiver.

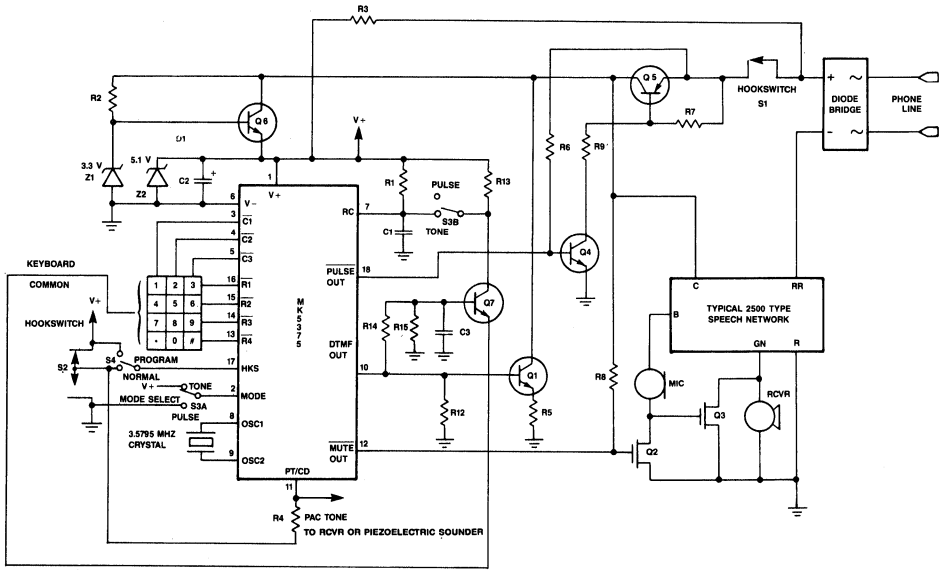
The two application circuits discussed in this application note are examples of just a few ways in which the MK5375 TonePulse™ Repertory Dialer may be used to meet a wide variety of requirements. For additional applications information and further details on the operation of the MK5375 and its specifications, please consult the MK5375 data sheet.



HOOKSWITCHES S1 AND S2 SHOWN IN ON-HOOK POSITION
(TELEPHONE TURNED OFF, NOT IN USE)

R1	220K	Q1	2N5550	C1	390 PF
R2	1.6K	Q4	2N5550	C2	100μF
R3	15M	Q2	VN10KM		
R4	220K	Q3	VN10KM		
R5	100Ω	Q5	2N5401		
R6	160K	Q6	2N5550		
R7	150K				
R8	240K	Z1	1N4620		
R9	3.3K	Z2	1N751		
R10	110K				
R11	560K				
R12	10K				

Figure 1. MK5375 Typical Application Without Battery Back-Up



HOOKSWITCHES S1 AND S2 SHOWN IN ON-HOOK POSITION (TELEPHONE TURNED OFF, NOT IS USE)

R1	220K	Q1	2N5550	C1	390 PF
R2	1.6K	Q4	2N5550	C2	100 μF
R3	15M	Q2	VN10KM	C3	0.01 μF
R4	220K	Q3	VN10KM		
R5	100Ω	Q5	2N5401		
R6	160K	Q6	2N5550		
R7	150K	Q7	2N3904		
R8	240K	Z1	1N4620		
R9	3.3K	Z2	1N751		
R10	110K	R13	560K		
R11	560K	R14	200K		
R12	10K	R15	240K		

Figure 2. MK5375 Typical Application Continuous Tone

THOMSON COMPONENTS MOSTEK

MK5370

SINGLE NUMBER PULSE TONE SWITCHABLE DIALER

COMMUNICATIONS PRODUCTS

FEATURES

- ☐ Stand-alone DTMF and pulse signaling
- ☐ Recall of last number dialed (up to 28 digits long)
- ☐ Form-A and 2-of-7 keyboard interface
- ☐ Pacifier tone
- ☐ Powered from telephone line, low operating voltage for long loop applications

DESCRIPTION

The MK5370 is a Mostek Silicon Gate CMOS IC that provides necessary signals for either DTMF or loop disconnect (pulse) dialing. The MK5370 buffers up to 28 digits into memory that can be later redialed with a single key input. This memory capacity is sufficient for local, long distance, overseas, and even computerized long-haul networks. Users can store all 12 signaling keys and redial them using either the * or # as the first key entry after going off-hook. Figure 2 shows the keypad configuration.

A * or # key input automatically redials the last number dialed if it is the first key entered after a transition from on-hook to off-hook (HKS input switched from a high to low logic level). Auto-dialing is momentarily interrupted (during interdigital pause period or intersignal period) while manual keys are depressed, however these inputs are not stored into memory.

FUNCTIONAL PIN DESCRIPTION

V+
Pin 1. V+ is the positive supply for the circuit and must meet the maximum and minimum voltage requirements. (See Electrical Specifications.)

MODE/TEST
Input. Pin 2. MODE/TEST determines the dialer's default operating mode. When the device is powered up or the hookswitch input is switched from on-hook (V+) to off-hook (V−) the default determines the signaling mode. A V+ connection selects to tone mode operation and a V− connection selects to pulse mode operation.

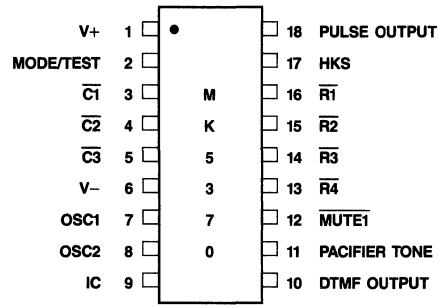


Figure 1. Pin Connection

1	2	3
4	5	6
7	8	9
* LND	0	# LND

Figure 2. Keypad Configuration

Pin 2 also forces the device into test mode. Further information on this operation can be obtained from Mostek.

C1, C2, C3, R4, R3, R2, R1
Keyboard Input. Pins 3, 4, 5, 13, 14, 15, 16. The MK5370 interfaces with either the standard 2-of-7 with negative common or the inexpensive single-contract (Form A) keyboard.

A valid keypad entry is either a single Row connected to a single Column or V- simultaneously presented to both a single Row and Column. In its quiescent or standby state, during normal off-hook operation, either the Rows or the Columns are at a logic level 1 (V+). Pulling one input low enables the on-chip oscillator to begin scanning the keypad. Scanning consists of Rows and Columns alternately switching high through on-chip pull-ups.

After both a Row and Column key have been detected, the debounce counter is enabled and any noise (bouncing contacts, etc.) is ignored for a debounce period (Tdb) of 32 ms. At this time, the keyboard is sampled and if both Row and Column information are valid, the information is buffered into the LND location. If switched on-hook (pin 17 to pin 1), the keyboard inputs all pull high through on-chip pull-up resistors.

IC

Input. Pin 9. Internal connection. This pin should be left floating for normal operation.

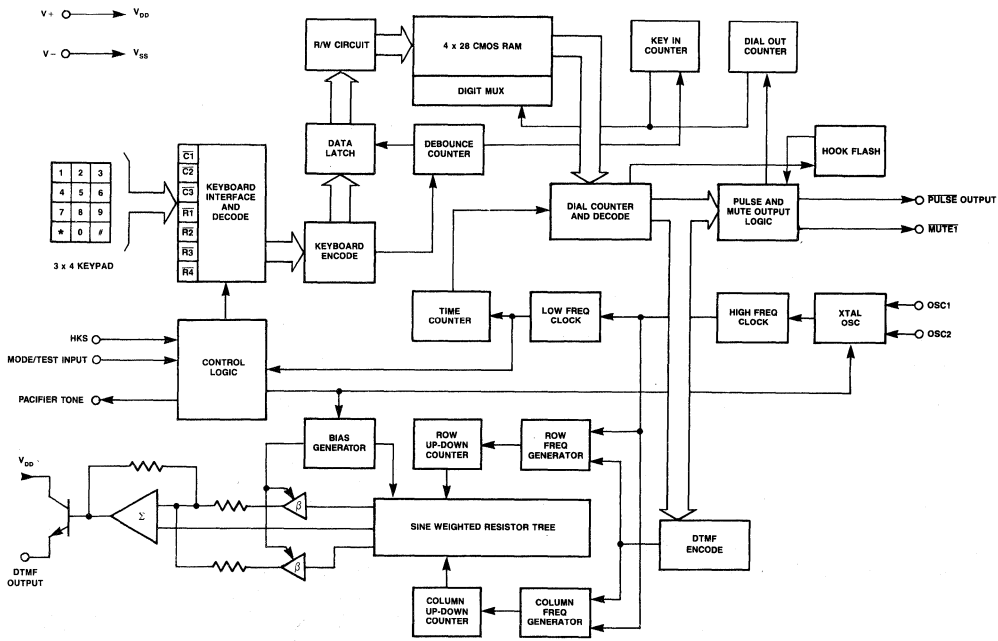


Figure 3. MK5370 Functional Block Diagram

V–
Input. Pin 6 is the negative supply input to the device. This is the voltage reference for all specifications.

OSC1, OSC2
Input/Output. Pins 7, 8. OSC1 and OSC2 are inputs to an on-chip inverter used as the timing reference for the circuit. It has sufficient loop gain to oscillate when used with a low-cost television color-burst crystal. The nominal crystal frequency is 3.579545 MHz and any deviation from this standard is directly reflected in the Tone output frequencies. The crystal oscillator provides the time reference for all circuit functions.

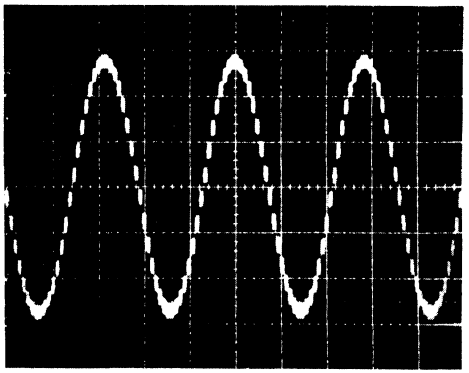


Figure 4. Single Tone

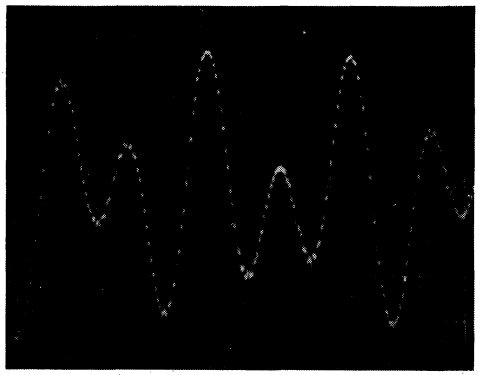


Figure 5. Dual Tone

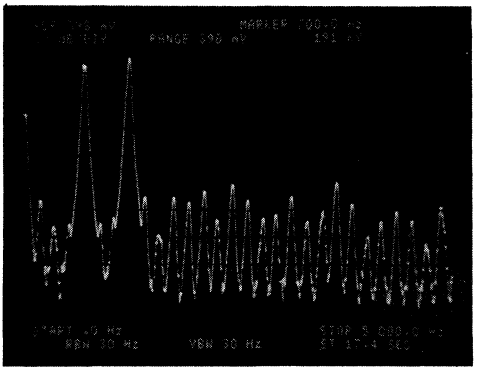


Figure 6. Spectral Response

DTMF OUTPUT
Output. Pin 10. An NPN transistor emitter with a collector tied to V+ drives the DTMF OUTPUT pin. The transistor base is connected to an on-chip operational amplifier that mixes the Row and Column tones. Figure 7 shows the timing at this pin.

The DTMF OUTPUT is the summation of a single Row frequency and a single Column frequency. A typical single tone sine wave is shown in Figure 4. This waveform is synthesized using a resistor tree with sinusoidally weighted taps.

The MK5370 is designed to operate from a regulated supply and the row (low group) TONE LEVEL is related to this supply by either of the following equations:

$$T_{O1} = 20 \text{ LOG } [(0.0776V+)/0.775] \text{ dBm}$$

$$T_{O1} = 0.0776(V+) \text{ VRMS}$$

The DC component of the DTMF output while active is described by the following equation:

$$V_{DC_1} = 0.66\ V+ - 0.6 \text{ Volts}$$

PACIFIER TONE OUTPUT
Output. Pin 11. A 500 Hz square wave is activated on pin 11 upon acceptance of a valid key input, after the 32 ms debounce time. The square wave terminates after a maximum of 30 ms or when the valid key is no longer present. In pulse mode, all key entries activate the pacifier tone. In tone mode, only a redial entry activates the pacifier tone. The pacifier tone provides audible feedback, confirming that the key has been properly entered and accepted.

Table 1. DTMF Output Frequency

KEY INPUT	STANDARD FREQUENCY	ACTUAL FREQUENCY	% DEVIATION
ROW 1	697	699.1	+0.31
2	770	766.2	−0.49
3	852	847.4	−0.54
4	941	948.0	+0.74
COL 1	1209	1215.9	+0.57
2	1336	1331.7	−0.32
3	1477	1471.9	−0.35

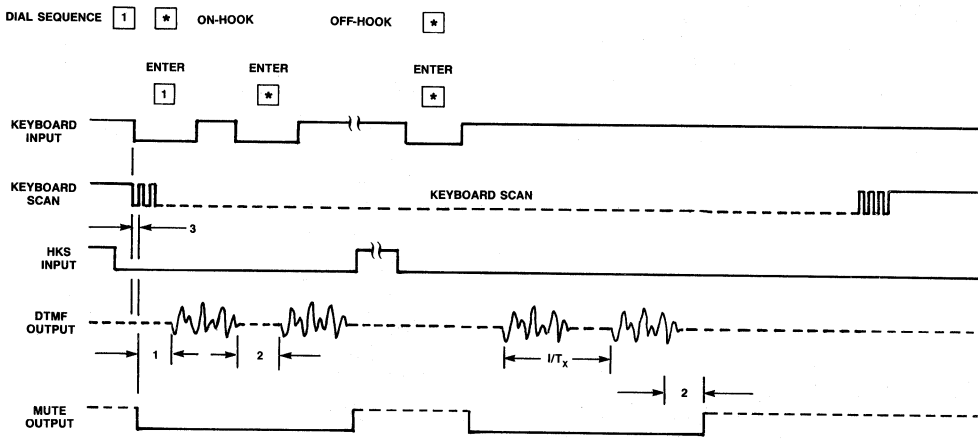


Figure 7. Tone Mode Timing

MUTE1
Output. Pin 12. This pin is the Mute Output for both tone and pulse modes. Timing is dependent upon mode.

The output consists of an open drain N-channel device. During standby, the output is high impedance and generally has an external pull-up resistor to the positive supply.

In tone mode, $\overline{\text{MUTE1}}$ removes the transmitter and the receiver from the network during DTMF signaling. During dialing, $\overline{\text{MUTE1}}$ is active continuously until dialing is completed.

In pulse mode, $\overline{\text{MUTE1}}$ removes the receiver or the network from the line. Different circuitry is required for tone and pulse muting external to the IC and applications using both modes would not necessarily share circuitry. $\overline{\text{MUTE1}}$ timing is shown in Figure 8 for pulse mode signaling and Figure 7 for tone mode signaling.

HKS
Input. Pin 17. Pin 17 is the hookswitch input to the MK5370. This is a high-impedance input and must be switched high for on-hook operation or low for off-hook operation. A transition on this input causes the on-chip logic to initialize, terminating any operation in progress at the time. The signaling mode defaults to the mode selected at pin 2.

$\overline{\text{PULSE}}$ OUTPUT
Output. Pin 18. This pin has a dual function determined by the dialing mode selected. In Pulse Mode, the pin is an output consisting of an open drain N-channel device with zener protection. The break timing at this output meets Bell Telephone and EIA specifications for loop disconnect signaling. Figure 8 shows this timing.

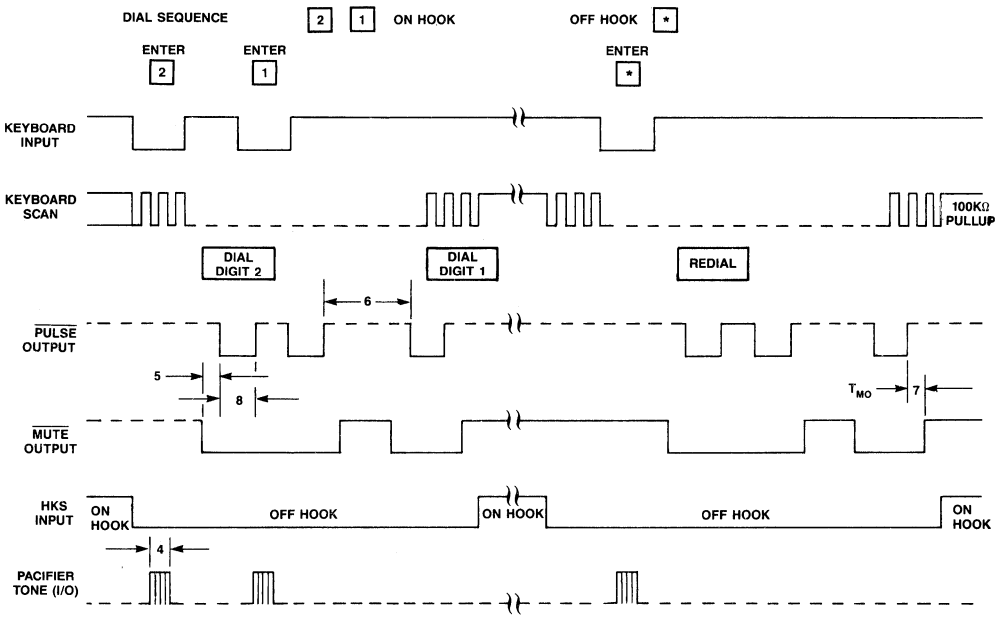


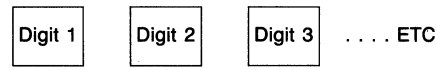
Figure 8. Pulse Mode Timing

DEVICE OPERATION (Tone Mode)

When the MK5370 is not actively dialing, it consumes very little current. While on-hook, all keypad input pins are pulled high. Key entries are not recognized unless they utilize a keypad common connection to force the respective Row and Column inputs low. These inputs assume opposite states off-hook. The circuit verifies that a valid key has been entered by alternately scanning the Row and Column inputs. If the input is still valid following 32 ms of debounce, the digit is stored into memory, and dialing begins after a pre-signal delay of 100 ms. Each digit buffered into the RAM is dialed out with a 98 ms burst of DTMF and an intersignal time of 102 ms.

One important feature of the dialer is its ability to buffer data into the RAM before signaling. This feature allows less expensive keyboards to be used because signal distortion and double digit entry caused by bouncing and bounding of the keypad are eliminated. This design also ensures that data stored in the buffer exactly matches the digits actually dialed.

NORMAL DIALING (Off-Hook)



Normal dialing is straightforward, all keyboard entries will be stored in the buffer and signaled in succession.

LAST NUMBER DIALED (LND)

Last number dialing is accomplished by entering the * or # key as the first entry after coming off-hook..

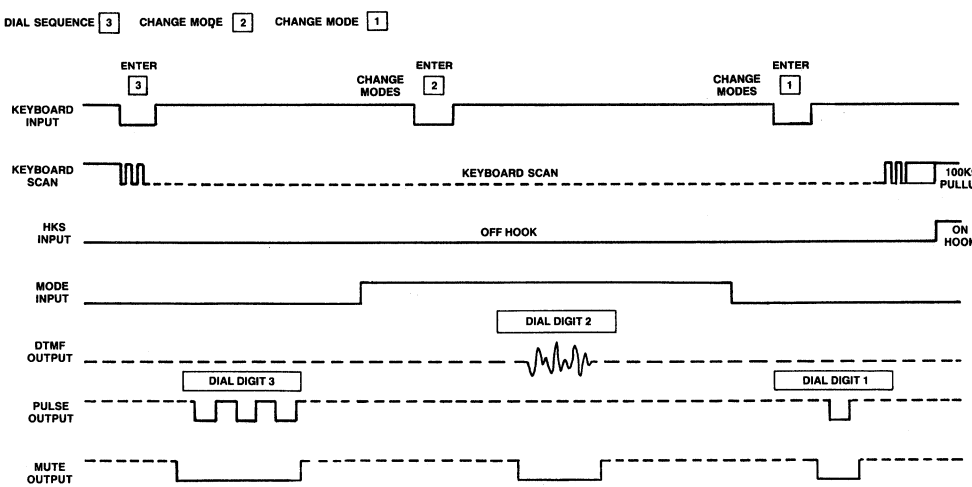


Figure 9. Pulse and Tone Mode Timing

Absolute Maximum Ratings*

DC Supply Voltage ..... 6.5 Volt
Operating Temperature ..... −30°C to +60°C
Storage Temperature ..... −55°C to +125°C
Maximum Power Dissipation (25°C) ..... 500 mW
Maximum Voltage on any Pin ..... (V+)+.3, (V−)−.3

Electrical Characteristics

* All specifications are for 2.5 Volt operation and full operating temperature range unless otherwise stated.

DC Characteristics

SYM	PARAMETER	MIN	TYP	MAX	UNIT	NOTES
V+	DC Operating Voltage (all functions)	2.5		6.0	Volts	
V_{MR}	Memory Retention Voltage	1.5	1.3		Volts	1, 6
I_s	Standby Current		0.2	1.0	μA	1
I_{MR}	Memory Retention Current		0.1	0.75	μA	5, 6
V_{MUTE}	Mute Output Operating Voltage	1.8			Volts	7
I_T	Operating Current (Tone)		300	600	μA	2
I_P	Operating Current (Pulse)		225	350	μA	2
I_{ML}	Mute Output Sink Current (V+ = 2.5 V)	1.0	2.0		mA	3
I_{PL}	Pulse Output Sink Current	1.0	2.0		mA	3
I_{PC}	Pacifier Tone Sink/Source	250	500		μA	4
K_{RU}	Keypad Pull-up Resistance		100		kohm	
K_{RD}	Keypad Pull-down Resistance		750		ohm	
V_{IL}	Keypad Input Level-Low	0		0.3V+	Volt	
V_{IH}	Keypad Input Level-High	0.7V+		V+	Volt	

NOTES

1. All inputs unloaded, Quiescent Mode (oscillator off)
2. All outputs unloaded, single key input
3. V_{OUT} = 0.4 Volts
4. Sink Current for V_{OUT} = 0.5 volts, Source Current for V_{OUT} = 2.0 Volts
5. Memory Retention Voltage is the point where memory is guaranteed but circuit operation is not.
6. Proper memory retention is guaranteed if either the minimum I_{MR} is provided or the minimum V_{MR}. The design does not have to provide both the minimum current or voltage simultaneously.
7. Minimum supply voltage where activation of mute output with key entry is ensured.

AC Characteristics—Keypad Inputs, Pacifier Tone

NO.	SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
3	T_{KD}	Keypad Debounce Time		32		ms	1
—	F_{KS}	Keypad Scan Frequency		250		Hz	1
—	T_{RL}	Two Key Rollover Time		4		ms	1
—	F_{PT}	Frequency Pacifier Tone		500		Hz	1
4	T_{PT}	Pacifier Tone Duration		30		ms	1

NOTES
1. Crystal oscillator accuracy directly affects these times.

AC Characteristics—Pulse Mode Operation

NO.	SYM	PARAMETERS	MIN	TYP	MAX	UNITS	NOTES
—	P_R	Pulse Rate		10		PPS	1
5	PDP	Predigital Pause		40		ms	2
6	IDP	Interdigital Pause		940		ms	2
7	T_{MO}	Mute Overlap Time		2		ms	2
8	T_B	Break Time		60		ms	2

NOTES
1. 10 PPS is the nominal rate.
2. Figure 8 illustrates this relationship.

AC Characteristics—Tone Mode

NO.	SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
—	T_{NK}	Tone Output No Key Down			−80	dBm	1
—	T_{Od}	Tone Output (dependent)	−13 173	−12 194	−11 218	dBm mV_{rms}	1, 2 5
—	PE_d	Pre-Emphasis, High Band	2.3	2.7	3.1	dB	
—	DC_d	Tone Output DC Bias (V+ = 2.5)	1.0	1.2		Volts	
—	R_E	Tone Output Load			10	kohm	5
—	T_{RIS}	Tone Output Rise Time		0.1	1.0	ms	6
—	DIS	Output Distortion		5.0	8.0	%	3
—	T_X	Tone Signaling Rate		5.0		1/sec	
1	T_{PSD}	Pre-Signal Delay		100		ms	7
2	T_{ISD}	Inter-Signal Delay		100		ms	

NOTES

1. O dBm equals 1 mW power into 600 ohms or 775 mVolts.
   Important Note: The MK5370 is designed to drive a 10 kohm load. The 600 ohm load is only for reference.
2. Single tone (low group), varies when used in subscriber set.
3. Supply voltage = 2.5 to 6 Volts, R_E=10 kohms.
4. R_E=10 Kohms
5. Supply voltage = 2.5 Volts. These specifications are supply-dependent
6. Time from beginning of tone output waveform to 90% of final magnitude of either frequency. Crystal parameters suggested for proper operation are R_s<100 Ω, L_m=96 mH, C_m=0.02 pF, C_h=5 pF, f=3.579545 MHz, and C_L=18 pF.
7. Time from initial key input until beginning of signaling.

TYPICAL APPLICATION

The MK5370 Mostek Pulse Tone dialer provides both cost-effective telephone-line interface and the logic required for DTMF (Tone) and Loop Disconnect (Pulse) signaling.

Pulse dialing originated with the rotary dial telephone. The Mostek Pulse Tone dialer provides the same capability as the rotary dial telephone and the convenience of pushbutton entry. The subscriber set (telephone) is powered by loop current supplied by the telephone company. Signaling, in Pulse Mode, is accomplished by repeatedly interrupting the loop current. The central office senses, times, and counts each line "break"; the number of breaks corresponds to the digit dialed. The duration of the break period, the dialing rate, and the separation between consecutive digits (IDP time) are controlled by the Pulse Tone dialer IC. Loop disconnect dialing is nearly a world-standard concept.

DTMF signaling consists of modulating the telephone line with a signal comprised of two fundamental frequencies. Each frequency pair represents one of sixteen possible digit (or key) entries. Twelve of these frequency pairs are commonly used (0, 1, 2, ..., *, #). The Mostek Pulse Tone dialer provides DTMF signalling capability controlling signal duration, separation, level, and rate.

The typical application circuit in Figure 10 illustrates one way the Pulse Tone dialer can be used. The pulse output provides the signal to break the line to transistor Q3. Q3 switches off, eliminating the base current to Q4, which also switches off. The majority of the loop current is then eliminated, resulting in a break condition. The IC dialer must be protected from large voltage fluctuations, such as that caused by interrupting the loop current. Transistor Q1 along with R2, C1, and Z1 regulate the voltage to the dialer. The Mute Output signal is active while signalling each digit to mute popping noises at the receiver (earpiece or speaker).

The DTMF tone output drives the base of Q8, which modulates the line. The tone level at tip and ring is determined by the effective impedance of the telephone line and the speech network.

Mode of operation is controlled by switch S1 (which sets the default dialing mode).

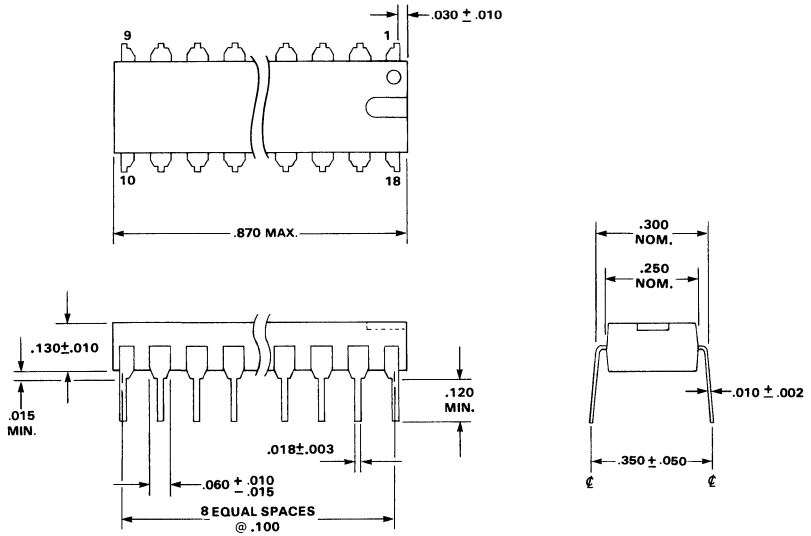
Resistor R1 provides a small memory-retention bias current to prevent the device from powering down while on hook. The current required for long term memory retention is less than 1μA.

A ceramic sounder can also be interfaced to pin 11 (PACIFIER TONE) of the device. A pacifier tone signal is activated for each key entry in pulse mode. This feature provides an audible indication for each valid key entry. Keys may be entered faster than the maximum signalling rate allows. Audible feedback confirms proper key entry.

PACKAGE DESCRIPTION

18-Pin DIP (N) (.300)

Plastic



NOTE: Overall length includes .010 flash on either end of package

THOMSON COMPONENTS MOSTEK

MK5371/MK5372

SINGLE NUMBER PULSE TONE SWITCHABLE DIALER

COMMUNICATIONS PRODUCTS

FEATURES

- ☐ Stand-alone DTMF and pulse signaling
- ☐ Softswitch automatically switches signaling mode
- ☐ Recall of last number dialed (up to 28 digits long)
- ☐ Flash key input initiates timed hook flash
- ☐ Microprocessor interface (BCD inputs) for smart telephones
- ☐ Timed PABX pause
- ☐ 10/20 PPS select option
- ☐ Form-A and 2-of-8 keyboard interface
- ☐ Pacifier tone
- ☐ Powered from telephone line, low operating voltage for long loop applications

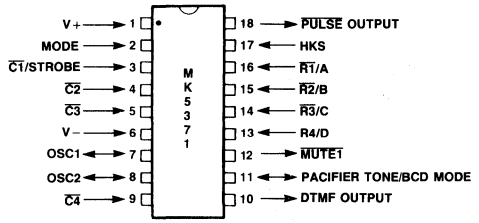


Figure 1. Pin Connection

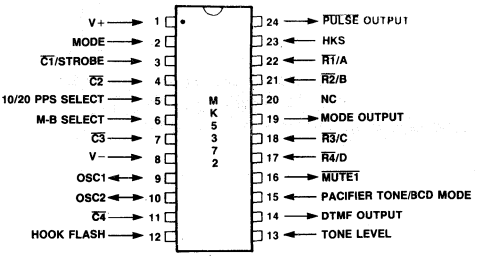


Figure 2. Pin Connection

DESCRIPTION

The MK5371 is a monolithic, integrated circuit manufactured using Mostek's Silicon Gate CMOS process. These circuits provide necessary signals for either DTMF or loop disconnect (Pulse) dialing. The MK5371 buffers up to 28 digits into memory that can be later redialed with a single key input. This memory capacity is sufficient for local, long distance, overseas, and even computerized long-haul networks. Users can store all 12 signaling keys and access several unique special functions with single key entries. These functions include: Last Number Dialed (LND), Softswitch (Mode), Flash, and Pause. Figure 3 shows the keypad configuration.

1	2	3	FLASH
4	5	6	MODE
7	8	9	PAUSE
*	0	#	LND

Figure 3. Keypad Configuration

A LND key input automatically redials the last number dialed. Keys entered during auto-dialing sequence will not be stored or dialed. However, auto-dialing is momentarily interrupted (during interdigital pause period or intersignal period) while manual keys are depressed.

The Mode key simplifies the process of alternating dialing modes. This input automatically toggles the immediate dialing mode. The function is also stored in memory. During auto-redial, the signaling mode is toggled each time the Mode code appears in the digit sequence. The signaling mode always defaults to the mode selected (hardwire or switch) at Pin 2 (MODE) after a Power-Up-Clear initialization or a transition from on-hook to off-hook (HKS input switched from a high to low logic level). Switching modes through Pin 2 toggles the immediate dialing mode and changes the default, but it is not stored in memory.

Two features simplify PABX dialing. The pause key stores a timed pause in the number sequence. Redial is then delayed until an outside line can be accessed or some other activity occurs before normal signaling resumes. The Flash key simulates a hook flash to transfer calls or to activate other special features provided by the PABX or a central office. The MK5371 ensures exact timing for the hook flash.

In addition to interfacing with standard keypads, the MK5371 also accepts parallel BCD inputs. This feature simplifies interfacing a microprocessor-based design to the telephone line. The MK5371 buffers 28 bytes of information, including special functions.

All of the preceeding features are provided by the MK5371 in an 18-pin package. The same features are provided by the MK5372 in a more versatile 24-pin version. Additionally, the MK5372 includes RC programmable hook-flash timing, selectable tone levels, and both Make-Break (M-B) and 10/20 pulses-per-second selection in the pulse mode.

FUNCTIONAL PIN DESCRIPTION

The following pin descriptions are numbered according to the 24-pin package. Pin numbers for the 18-pin version are listed in parenthesis under each pin name.

V+
Pin 1 (1). V+ is the positive supply for the circuit and must meet the maximum and minimum voltage requirements. (See Electrical Specifications.)

MODE
Input. Pin 2 (2). MODE determines the dialer's default operating mode. When the device is powered up or the hookswitch input is switched from on-hook, (V+), to off-hook, (V−), the default determines the signaling mode. A V+ connection defaults to Tone Mode operation and a V− connection defaults to Pulse Mode operation.

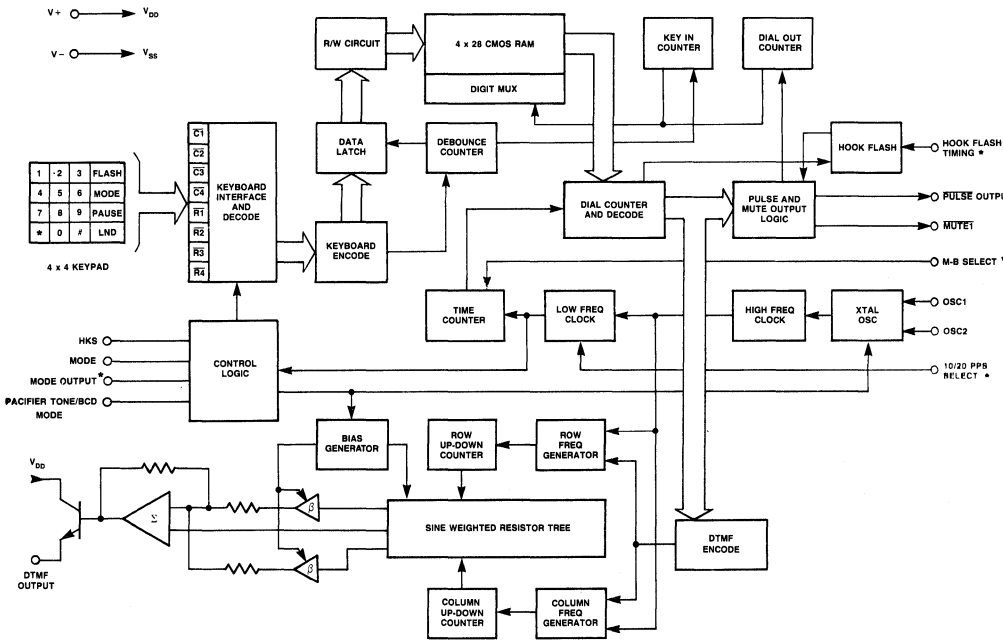
A Softswitch (Mode) code entered in a number sequence can temporarily modify the signaling mode. After encountering a first Softswitch code in a number sequence, the Signaling Mode toggles and is opposite the default determined by Pin 2. A second Softswitch code toggles the Signaling Mode a second time, returning the mode back to the default condition. Note that the Softswitch code performs a toggle function on the default state; switching the state of Pin 2 while dialing changes the default state as well as the immediate signaling mode.

$\overline{C1}$/STROBE, $\overline{C2}$, $\overline{C3}$, $\overline{C4}$, $\overline{R4}$, $\overline{R3}$, $\overline{R2}$, $\overline{R1}$
Keyboard Input. Pins, 3, 4, 7, 11, 17, 18, 21, 22 (3, 4, 5, 9, 13, 14, 15, 16). The MK5371 interfaces with standard keypads as well as a microprocessor-driven 4-bit bus.

A valid keypad entry is either a single Row connected to a single Column or V- simultaneously presented to both a single Row and Column. In its quiescent or standby state, during normal off-hook operation, either the Rows or the Columns are at a logic level 1 (V+). Pulling one input low enables the on-chip oscillator. Keyboard scanning then begins. Scanning consists of Rows and Columns alternately switching high through on-chip pullups. After both a Row and Column key have been detected, the debounce counter is enabled and any noise (bouncing contacts, etc.) is ignored for a debounce period (Tdb) of 32 ms. At this time, the keyboard is sampled and if both Row and Column information is valid, the information is buffered into the LND location. If switched on-hook, the keyboard inputs all pull high through on-chip pull-up resistors. Information may still be entered into memory but it is not signaled and the keyboard scan is disabled. If users desire to enter data while on-hook, a 2-of-8 keypad with negative common is required.

A key entry during LND interrupts the sequence when it reaches the redial period until the key is released. Dialing then resumes. The key entered is not stored or dialed.

The keyboard inputs become high impedance when the Binary Input Mode is selected. As shown in Table 1, Row pins become inputs for the Binary codes from a microprocessor in this mode. Table 1 equates the Binary Codes to the keyboard digits and special functions. The $\overline{C1}$ input pin now provides an input for a strobe



NOTE:

* indicates MK5372 only.

Figure 4. MK5371/MK5372 Functional Block Diagram

strobe used to clock the valid codes into the LND buffer. Dialing proceeds at the specified rates. The strobe duration must be active for at least 2 μs to ensure proper acceptance of the information. If the strobe remains high for longer than 96 ms false dialing may occur. A minimum of 8 ms must separate each strobe. Figure 5 illustrates the required strobe/data timing. Valid encoded signaling information must be present until the strobe goes low. Information entered during an on-hook operation is stored but signaling is inhibited. Changing between BCD and keyboard mode can only occur when the HKS input is high, or upon power-up. Caution, a power supply transient may be interpreted as a power-up condition, and the logic level on pin 15 (11) at that time will be interpreted as a valid BCD/Keyboard selection.

Table 1. Binary Input Codes

D	C	B	A	KEYBOARD FUNCTION	D	C	B	A	KEYBOARD FUNCTION
0	0	0	0	0	1	0	0	0	8
0	0	0	1	1	1	0	0	1	9
0	0	1	0	2	1	0	1	0	*
0	0	1	1	3	1	0	1	1	#
0	1	0	0	4	1	1	0	0	MODE
0	1	0	1	5	1	1	0	1	PAUSE
0	1	1	0	6	1	1	1	0	FLASH
0	1	1	1	7	1	1	1	1	LND

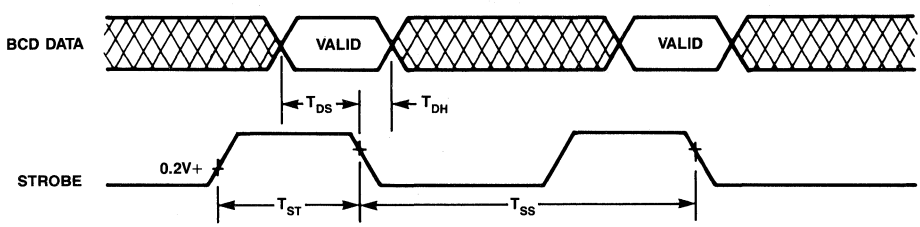


Figure 5. BCD Mode Strobe Interface Timing

10/20 PPS SELECT
Input. Pin 5. In Pulse Mode, 10/20 PPS (pulses per second) SELECT allows users to double the dialing rate (20 PPS) by tying this pin high. If this input is left floating or is tied low, the dialing rate is 10 PPS. This input has no effect in Tone Mode.

M-B SELECT
Input. Pin 6. This pin is used to select the Make-Break ratio for pulse dialing. Table 2 shows the make and break timings obtained with either a logic 1 or logic 0 on this input. The 18-pin package has a predetermined Make-Break ratio of 40 to 60.

Table 2. Make-Break Select

PIN 6 INPUT	MAKE TIME	BREAK TIME
V+	32	68
V–	40	60

V–
Input. Pin 8 (6). Pin 6 is the negative supply input to the device. This is the voltage reference for all specifications.

OSC1, OSC2
Input/Output. Pins 9, 10 (7, 8). OSC1 and OSC2 are inputs to an on-chip inverter used as the timing reference for the circuit. It has sufficient loop gain to oscillate when used with a low-cost television color-burst crystal. The nominal crystal frequency is 3.579545 MHz and any deviation from this standard is directly reflected in the Tone output frequencies. The crystal oscillator provides the time reference for all circuit functions.

HOOK FLASH
Input. Pin 12. HOOK FLASH lets users control the Flash signal duration. An external resistor and capacitor determine the exact duration of the Flash. Tying this input low results in a default Flash time period (600 ms), eliminating the need for an external RC. The RC values may be fixed or variable components may be used to ensure compatibility with all systems.

The component values required may be calculated using the following equation:

$$T_{FLASH} = 1.45\ RC$$

The capacitor should be no larger than 1μF. The time period may be made long enough to disconnect the telephone from the line. This may prove particularlly useful in microprocessor applications. The recommended range for the T_{FLASH} period is from 100 ms minimum to a maximum of two seconds.

TONE LEVEL

Input. Pin 13. The DTMF OUTPUT is the summation of a single Row frequency and a single Column frequency. A typical single tone sine wave is shown in Figure 6. This waveform is synthesized using a resistor tree with sinusoidally weighted taps.

The MK5372 is programmable between two methods for referencing the TONE LEVEL. The first method, selected by tying this pin low, is the supply-dependent TONE LEVEL where the TONE LEVEL is a linear function of the supply voltage (compatible with the MK5089). The second method, selected by tying this pin high, is the independent TONE LEVEL determined by an on-chip reference independent of the supply voltage (compatible with the MK5380). See Table 3.

Method 1 is designed to operate from a regulated supply and the TONE LEVEL is related to this supply by either of the following equations:

$$T_{O1} = 20\ LOG\ [(0.0776V+)/0.775]\ dBm$$

$$T_{O1} = 0.0776(V+)\ VRMS$$

Table 3. Tone Level Select

TONE LEVEL SELECT INPUT	TONE REFERENCE	COMPATIBLE WITH
V– (Method 1)	Supply	MK5089
V+ (Method 2)	On-Chip Reference	MK5380

The DC component of the DTMF (Method 1) output while active is described by the following equation:

$$V_{DC_1} = 0.66\ V+ - 0.6\ Volts$$

Method 2 provides a constant tone output and modulates its own supply in a minimum parts count configuration. The minimum instantaneous voltage level required for proper operation is 2.5 volts with the device modulating its own supply. This version may also be operated on a regulated supply, but users should be aware that operation below 3.0 volts could cause excessive distortion.

The TONE LEVEL, when used in a subscriber set without a regulated supply, is a function of the output resistor R_E and the telephone AC impedance Z_L. The low-group single tone output amplitude is a function of R_E and Z_L by the relationship:

$$V_O / T_O = 1/[0.2 + R_E/Z_L]$$

where V_O is the tone output amplitude at the phone line, and Z_L is the equivalent AC impedance in shunt with the tone generator. Z_L typically varies with loop current. R_E is the resistor value from DTMF OUTPUT to V–. In a 2500-type application, Z_L varies from 200 to 500 ohms. Thus, at the phone line, tone output levels range from 200 to 400 mVRMS, depending on loop current.

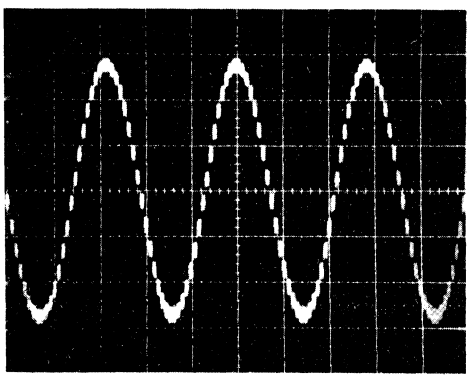


Figure 6. Single Tone

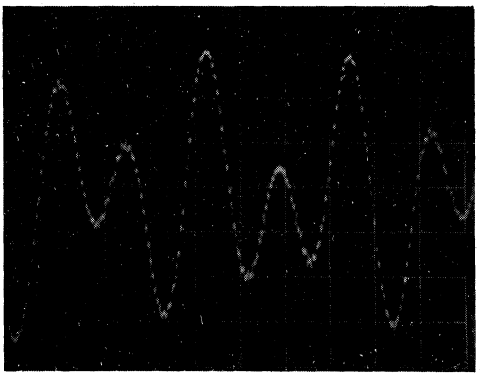


Figure 7. Dual Tone

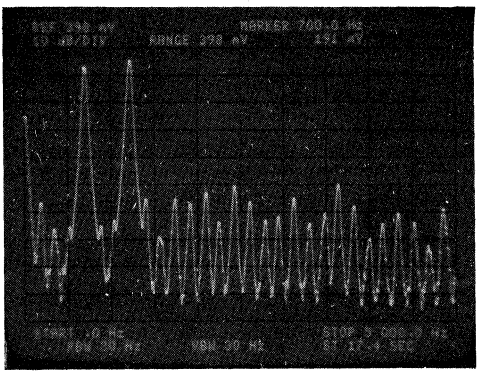


Figure 8. Spectral Response

The DC component of the DTMF output while active is described by the following equation:

$$V_{DC_2} = 0.3\ V+ + 0.5\ Volts$$

MODE OUTPUT

Output. Pin 19. MODE OUTPUT is driven by an open drain N-channel device. It provides an active low level in Pulse Mode only and is high impedence during Tone Mode and when the device is switched on-hook. It provides a means for indicating the active dialing mode.

DTMF OUTPUT
Output. Pin 14 (10). An NPN transistor emitter with a collector tied to V+ drives the DTMF OUTPUT pin. The transistor base is connected to an on-chip operational amplifier that mixes the Row and Column Tones together. Figure 8 shows the timing at this pin.

PACIFIER TONE OUTPUT/BCD MODE
Input/Output. Pin 15 (11). A 500 Hz square wave is activated at this pin upon acceptance of a valid key input, after the 32 ms debounce time. The square wave terminates after a maximum of 30 ms or when the valid key is no longer present. In the Pulse mode the PACIFIER TONE is activated for all key entries. The PACIFIER TONE provides audible feedback, confirming that the key has been properly entered and accepted. In Tone mode, only the LND key activates the PACIFIER TONE.

This pin is normally high impedance until a key is entered. Connecting this pin high through a resistor causes the circuit to accept BCD inputs through the ROW pins. In Binary Mode, as mentioned in the keyboard interface description, the keyboard inputs are all high impedance. Keypad inputs in this mode are not recognized. Connecting this pin low enables the keyboard scan circuitry, which allows entries. The mode of operation is selected upon power-up, and thereafter may only occur when HKS pin 23 (17) is high.

Table 4. DTMF Output Frequency

KEY INPUT	STANDARD FREQUENCY	ACTUAL FREQUENCY	% DEVIATION
ROW 1	697	699.1	+0.31
2	770	766.2	−0.49
3	852	847.4	−0.54
4	941	948.0	+0.74
COL 1	1209	1215.9	+0.57
2	1336	1331.7	−0.32
3	1477	1471.9	−0.35

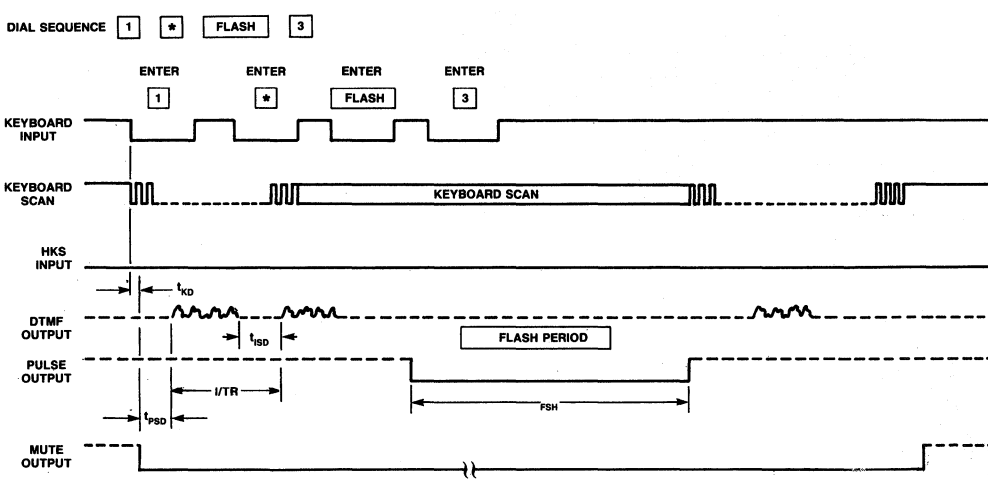


Figure 9. Tone Mode Timing

MUTE1
Output. Pin 16 (12). This pin is the Mute Output for both Tone and Pulse Modes. Timing is dependent upon mode.

The output consists of an open drain N-channel device. During standby, the output is high impedance and generally has an external pullup resistor to the positive supply.

In Tone Mode, $\overline{\text{MUTE1}}$ removes the transmitter and the receiver from the network during DTMF signaling. During dialing, $\overline{\text{MUTE1}}$ is active continuously until dialing is completed.

In Pulse Mode, $\overline{\text{MUTE1}}$ removes the receiver or the network from the line. Different circuitry is required for Tone and Pulse muting external to the IC and applications using both modes would not necessarily share circuitry. $\overline{\text{MUTE1}}$ timing is shown in Figure 10 for Pulse Mode signaling and Figure 9 for Tone Mode signaling.

HKS
Input. Pin 23 (17). Pin 23 is the hookswitch input to the MK5372. This is a high impedance input and must be switched high for on-hook operation or low for off-hook operation. A transition on this input causes the on-chip logic to initialize, terminating any operation in progress at the time. The signaling mode defaults to the mode selected at Pin 2.

$\overline{\text{PULSE}}$ OUTPUT
Output. Pin 24 (18). This pin has a dual function determined by the dialing mode selected. In Pulse Mode, the pin is an output consisting of an open drain N-channel device with zener protection. The break timing at this output meets Bell Telephone and EIA specifications for loop disconnect signaling. The Make/Break ratio is not user selectable in the 18-pin version. $\overline{\text{PULSE}}$ OUTPUT also provides the break timing for the hook flash function. Figure 10 shows this timing.

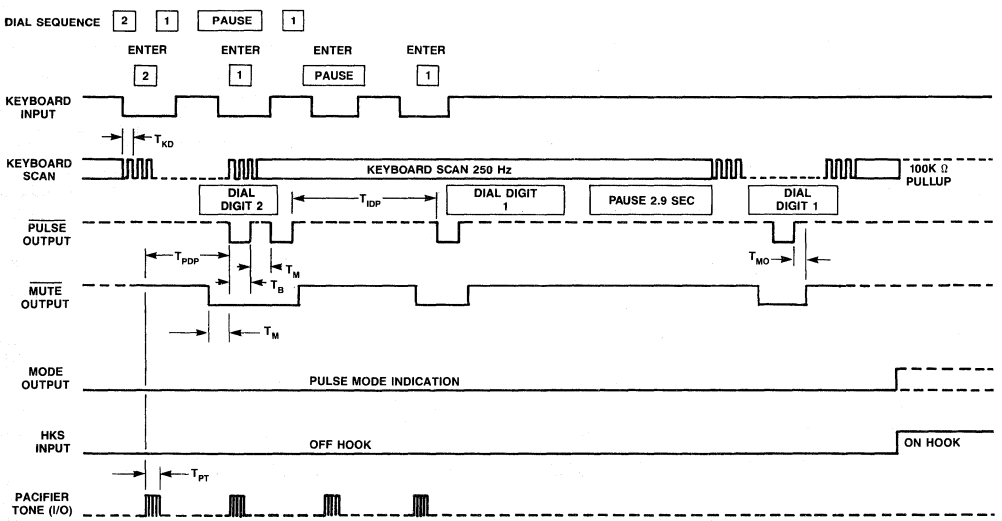


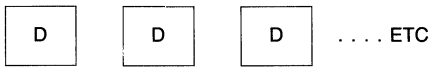
Figure 10. Pulse Mode Timing

DEVICE OPERATION (Tone Mode)

When the MK5371 is not actively dialing, it consumes very little current. While on-hook, all keypad input pins are pulled high. Key entries are not recognized unless they utilize a keypad common connection to force the respective Row and Column inputs low. These inputs assume opposite states off-hook. The circuit verifies that a valid key has been entered by alternately scanning the Row and Column inputs. If the input is still valid following 32 ms of debounce, the digit is stored into memory, the Mute Output is activated, and dialing begins after a pre-signal delay of 100 ms. Each digit buffered into the RAM is dialed out with a 98 ms burst of DTMF and an intersignal time of 102 ms.

One important feature of the dialer is its ability to buffer data into the RAM before signaling. This feature allows less expensive keyboards to be used because signal distortion and double digit entry caused by bouncing and bounding of the keypad are eliminated. This design also ensures that data stored in the buffer exactly matches the digits actually dialed.

NORMAL DIALING (Off-Hook)



Normal dialing is straightforward, all keyboard entries will be stored in the buffer and signaled in succession.

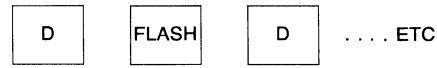
LAST NUMBER DIALED (LND)

Last Number Dialing is accomplished by entering the LND key.

PABX PAUSE

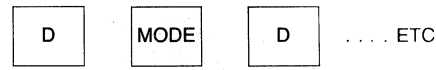
A pause may be entered into the dialed sequence at any point by keying in the special function key, Pause. Pause inserts a 1.1-second delay into the dialing sequence. The total delay, including pre-digital and post-digital pauses is shown in Table 5.

HOOK FLASH



HOOK FLASH may be entered into the dialed sequence at any point by keying in the function key, Flash. The flash function is stored in the LND buffer just like any other digit, but it will not be redialed, and acts much like Pause. Flash consists of a timed Break whose period is determined by the RC value used on Pin 12 (MK5372). Tying this input low will set HOOK FLASH to the chip default time of 600 ms. The MK5371 has a HOOK FLASH time of 600 ms.

SOFTSWITCH



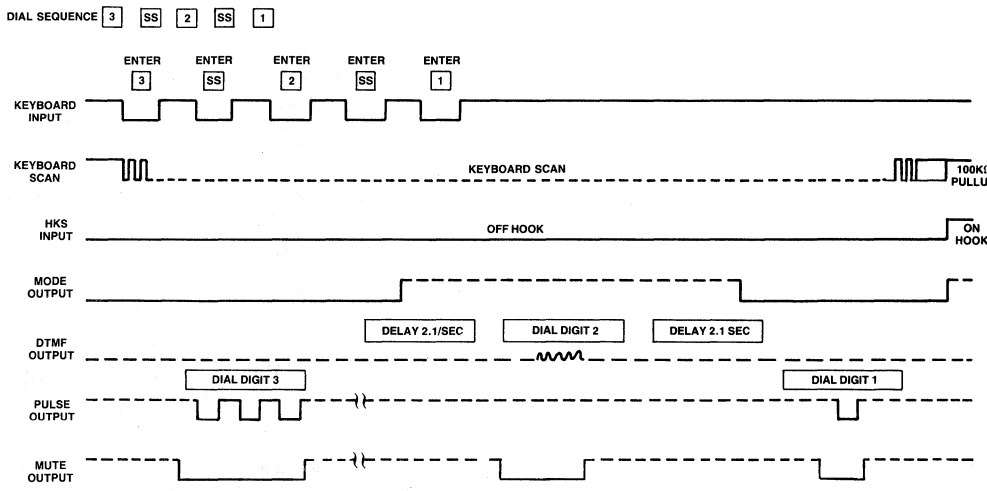
Softswitch allows the user to easily switch from Pulse to Tone Mode while dialing a number sequence. For example, the first digits may be entered in Pulse Mode. Signaling will proceed in Pulse Mode until a Softswitch (Mode) entry is encountered. Any subsequent digits are dialed using DTMF signals. A hookswitch transition or a second Softswitch entry returns dialing to the original Default Mode.

Each special function provides a built-in delay before auto-dialing resumes. The fixed delay introduced by the function is 1.1 seconds. In addition, the fixed delay is preceded and followed by the standard interdigital pause period that depends on the selected signaling mode. Table 5 lists the actual delays produced by each function.

Table 5. Special Function Delay Periods

FUNCTION	DELAY	PULSE MODE	TONE MODE
PAUSE	IDP + 1.1 + IDP	2.9 sec	1.3 sec
SOFTSWITCH	IDP + 1.1 + IDP	2.1 sec	2.1 sec
FLASH (RC)	.6 + IDP	1.5 sec	0.7 sec
(V−)	IDP	0.9 sec	0.1 sec

NOTE:
The Flash delay times do not include the break interval, only the time following break.



NOTE: SS = Softswitch

Figure 11. Pulse and Tone Mode Timing

ABSOLUTE MAXIMUM RATINGS*

DC Supply Voltage ..... 6.5 Volt
Operating Temperature ..... −30°C to +60°C
Storage Temperature ..... −55°C to +125°C
Maximum Power Dissipation (25°C) ..... 500 mW
Maximum Voltage on any Pin ..... (V+)+0.3, (V−)−0.3 volt

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

* All specifications are for 2.5 Volt operation and full operating temperature range unless otherwise stated.

DC CHARACTERISTICS

SYM	PARAMETER	MIN	TYP	MAX	UNIT	NOTES
V+	DC Operating Voltage	2.5		6.0	Volt	
V_{MR}	Memory Retention Voltage	1.5	1.3		Volt	1, 6
I_S	Standby Current		0.2	.750	μA	1
I_{MR}	Memory Retention Current		0.10	0.75	μA	5, 6
I_T	Operating Current (Tone)		300	600	μA	2
I_P	Operating Current (Pulse)		225	350	μA	2
I_{ML}	Mute Output Sink Current	1.0	2.0		mA	3
I_{PL}	Pulse Output Sink Current	1.0	2.0		mA	3
I_{PC}	Pacifier Tone Sink/Source	250	500		μA	4
K_{RU}	Keypad Pullup Resistance		100		kohm	
K_{RD}	Keypad Pulldown Resistance		750		ohm	
V_{IL}	BCD/Keypad Input Level-Low	0		0.2V+	V	
V_{IH}	BCD/Keypad Input Level-High	0.7V+		V+	V	

NOTES:
1. All inputs unloaded, Quiescent Mode (oscillator off), V+ = 2.5 V
2. All outputs unloaded, single key input
3. V_{OUT} = 0.5 Volts, V+ = 2.5 V
4. Sink Current for V_{OUT} = 0.5, Source Current for V_{OUT} = 2.0 Volts
5. Memory Retention Voltage is the point where memory is guaranteed but circuit operation is not.
6. Proper memory retention is guaranteed if either the minimum I_{MR} is provided or the minimum V_{MR}. The design does not have to provide both the minimum current or voltage simultaneously.

AC CHARACTERISTICS KEYPAD INPUTS, PACIFIER TONE

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
T_{KD}	Keypad Debounce Time		32		ms	1
F_{KS}	Keypad Scan Frequency		250		Hz	1
T_{RL}	Two Key Rollover Time		4		ms	1
F_{PT}	Frequency Pacifier Tone		500		Hz	1
T_{PT}	Pacifier Tone Duration		30		ms	1
T_{HFP}	Hookflash Timing		600		ms	1, 3
F_{SR}	BCD Strobe Rate			124	1/sec	1
T_{DS}	Data Setup	2			μs	1, 2
T_{DH}	Data Hold	1			μs	1, 2
T_{ST}	Strobe Width	2		96000	μs	1, 2
T_{SS}	Strobe Separation	9			ms	

NOTES:
1. Crystal oscillator accuracy directly affects these times.
2. Figure 5 illustrates this timing relationship.
3. HOOK FLASH pin input must be tied to V− on the 24-pin version, otherwise this time is described by external RC values.

AC CHARACTERISTICS PULSE MODE OPERATION

SYM	PARAMETERS	MIN	TYP	MAX	UNITS	NOTES
P_R	Pulse Rate		10	20	PPS	1
T_{PDP}	Predigital Pause		140		ms	2
T_{IDP}	Interdigital Pause		940		ms	2
T_{MO}	Mute Overlap Time		4		ms	2
T_B	Break Time (MK5371) (MK5372 Pin 6 to V+) (MK5372 Pin 6 to V−)		60 68 60		ms	2

NOTES:
1. 10 PPS is the nominal rate; 20 PPS is available on the 24-pin version.
2. Figure 10 illustrates this relationship.

AC CHARACTERISTICS TONE MODE

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
T_{NK}	Tone Output No Key Down			−80	dBm	1
T_{Od}	Tone Output (dependent)	−13 173	−12 194	−11 218	dBm mV_{rms}	1, 2 5
PE_d	Pre-Emphasis, High Band	2.3	2.7	3.1	dB	
DC_d	Tone Output DC Bias	1.0	1.2		V	4
T_{Oi}	Tone Output (independent)	−13	−12 194	−11	dBm mV_{rms}	2, 3
PE_i	Pre-Emphasis, High Band		2.0		dB	3
DC_i	Tone Output DC Bias		1.2		V	4
R_E	Tone Output Load		10		kohm	5
T_{RIS}	Tone Output Rise Time		0.1	1.0	ms	6
DIS	Output Distortion		5.0	8.0	%	3
TR	Tone Signaling Rate		5.0		1/sec	
T_{PSD}	Pre-Signal Delay		100		ms	7
T_{ISD}	Inter-Signal Delay		100		ms	

NOTES:

1. O dBm equals 1 mW power into 600 ohms (775 mVolts).
   Important Note: The MK5371/MK5372 are designed to drive a 10k ohm load. The 600 ohm load is only for reference.
2. Single tone (low group).
3. Supply voltage = 2.5 to 6 Volts, R_E=10k ohms.
4. R_E=10k ohms, V+ = 2.5 Volts
5. Supply voltage = 2.5 Volts. These specifications are supply-dependent
6. Time from beginning of tone output waveform to 90% of final magnitude of either frequency. Crystal parameters suggested for proper operation are R_s<100 Ω, L_m=96 mH, C_m=0.02 pF, C_h=5 pF, f=3.579545 MHz, and C_L=18 pF.
7. Time from Mute active to beginning of signaling.

TYPICAL APPLICATION

The MK5371 Mostek Pulse Tone dialer provides both cost-effective telephone-line interface and the logic required for DTMF (Tone) and Loop Disconnect (Pulse) signaling.

Pulse dialing originated with the rotary dial telephone. The Mostek Pulse Tone dialer provides the same capability as the rotary dial telephone and the convenience of pushbutton entry. The subscriber set (telephone) is powered by loop current supplied by the telephone company. Signalling, in Pulse Mode, is accomplished by repeatedly interrupting the loop current. The central office senses, times, and counts each line "break"; the number of breaks corresponds to the digit dialed. The duration of the break period, the dialing rate, and the separation between consecutive digits (IDP time) are controlled by the Pulse Tone dialer IC. Loop disconnect dialing is nearly a world-standard concept.

DTMF signalling consists of modulating the telephone line with a signal comprised of two fundamental frequencies. Each frequency pair represents one of sixteen possible digit (or key) entries. Twelve of these frequency pairs are commonly used (0, 1, 2, ..., *, #). The Mostek Pulse Tone dialer provides DTMF signalling capability controlling signal duration, separation, level, and rate.

The typical application circuit in Figure 12 illustrates one way the Pulse Tone dialer can be used. The pulse output provides the signal to break the line to transistor Q3. Q3 switches off, eliminating the base current to Q4, which also switches off. The majority of the loop current is then eliminated, resullting in a break condition. The IC dialer must be protected from large voltage fluctuations, such as that caused by interrupting the loop current. Transistor Q1 along with R2, C1, and Z1 regulate the voltage to the dialer. The Mute Output signal is active while signalling each digit to mute popping noises at the receiver (earpiece or speaker).

The DTMF tone output drives the base of Q8, which modulates the line. The tone level at tip and ring is determined by the effective impedance of the telephone line and the speech network.

Mode of operation is controlled by switch S1 (which sets the default dialing mode) and the keypad. A change of dialing mode with a Mode (Softswitch) key input is stored in memory and will be repeated when the LND (last number dialed) feature is activated.

Resistor R1 provides a small memory-retention bias current to prevent the device from powering down while on hook. The current required for long term memory retention is less than 1μA.

A ceramic sounder can also be interfaced to pin 11 (BCD/PACIFIER TONE) of the device. A pacifier tone signal is activated for each key entry. This feature provides an audible indication for each valid key entry. Keys may be entered faster than the maximum signalling rate allows. Audible feedback confirms proper key entry.

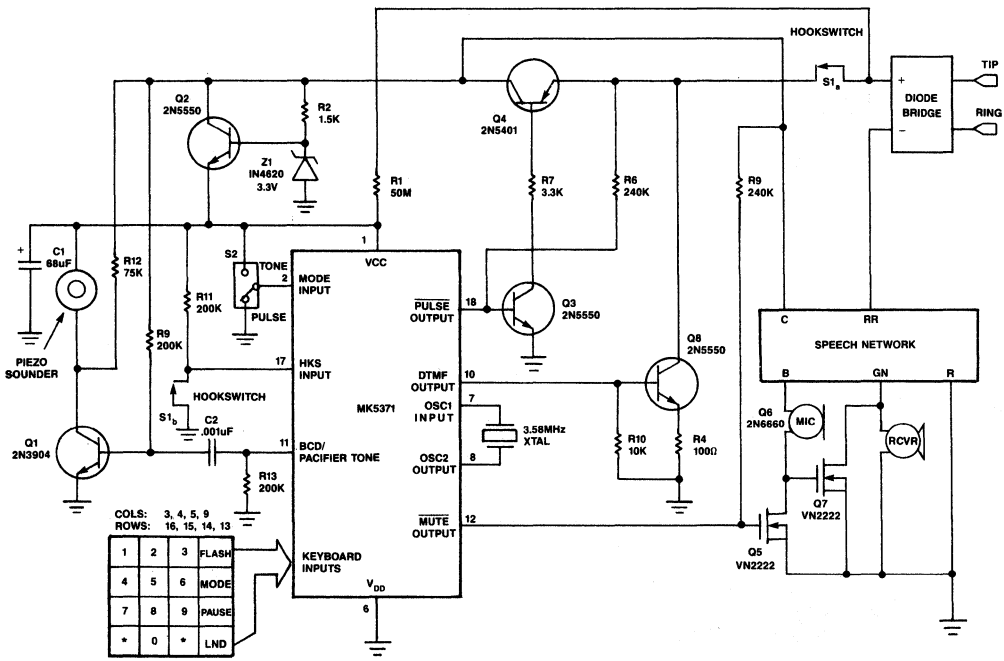
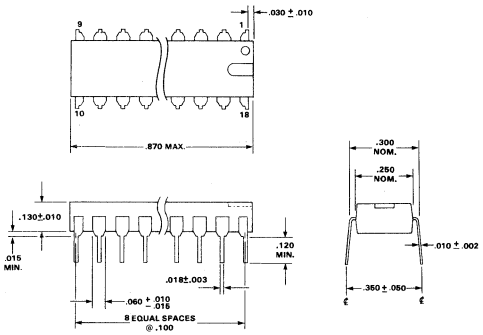


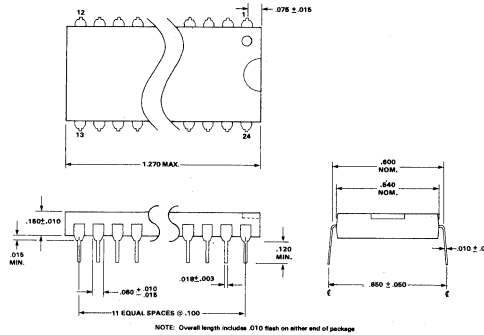
Figure 12. MK5371 Typical Application

PACKAGE DESCRIPTION
18-Pin DIP (N) (.300)
Plastic



NOTE: Overall length includes .010 flash on either end of package

PACKAGE DESCRIPTION
24-Pin DIP (N) (.600)
Plastic



NOTE: Overall length includes .010 flash on either end of package

FEATURES

- ☐ Two select pins allow the user to select 16 different country options.
- ☐ Single chip mixed mode dialer allows dialing in either tone or pulse modes. A * or "SOFTSWITCH" key input can also be used to switch from Pulse to Tone mode operation and is stored in memory.
- ☐ 28 digit storage with LNR (last number redial)
- ☐ P.I.N. (personal identify number) protection method
- ☐ Hookswitch debounce, transients due to line reversals and drop-outs can be masked for a period determined by external RC.
- ☐ Powered from telephone line, low standby current and operating voltage.
- ☐ DTMF signal consistent with key entry period.
- ☐ Minimum DTMF signal duration/separation guaranteed.
- ☐ Timed PABX pause may be stored in Memory.
- ☐ Timed FLASH for extended timed Break recall.

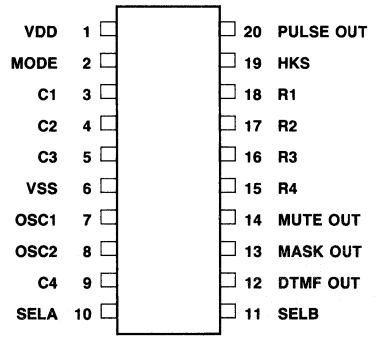


Figure 1. MK53721 Pinout

1	2	3	FLASH
4	5	6	SS
7	8	9	PAUSE
*	0	#	LNR

Figure 2. MK53721 Keypad Configuration

MK53731

SINGLE NUMBER PULSE TONE SWITCHABLE DIALER

COMMUNICATIONS PRODUCTS

FEATURES

- ☐ Single chip DTMF and pulse dialer.
- ☐ Softswitch changes signaling mode from pulse to tone.
- ☐ Recall of last number dialed (up to 28 digits long).
- ☐ Flash key input initiates timed hook flash.
- ☐ Timed PABX pause.
- ☐ 8 Tones Per Second dialing in tone mode and 10 PPS in pulse mode.
- ☐ DTMF active until key release.
- ☐ Minimum DTMF duration/separation guaranteed (74/54 ms).
- ☐ Pacifier tone provides audible indication of valid key input for non-DTMF key entries.
- ☐ Powered from telephone line, low operating voltage for long loop applications.

DESCRIPTION

The MK53731 is a Mostek Silicon Gate CMOS IC that provides necessary signals for either DTMF or loop disconnect (pulse) dialing. The MK53731 buffers up to 28 digits into memory that can be later redialed with a single key input. This memory capacity is sufficient for local, long distance, overseas, and even computerized long-haul networks. Users can store all 12 signaling keys and access several unique functions with single key entries. These functions include: Last Number Dialed (LND), Softswitch, Flash, and Pause. Figure 2 shows the keypad configuration.

A LND key input automatically redials the last number dialed.

Two features simplify PABX dialing. The pause key stores a timed pause in the number sequence. Redial is then delayed until an outside line can be accessed or some other activity occurs before normal signaling resumes. The FLASH key simulates a 560 ms hook flash to transfer calls or to activate other special features provided by the PABX or a central office.

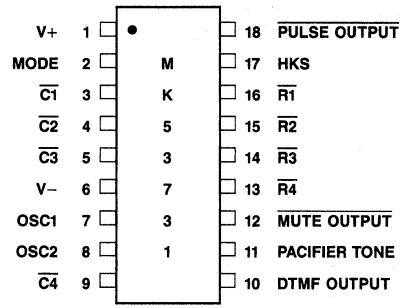


Figure 1. Pin Connection

1	2	3	FLASH
4	5	6	SOFTSWITCH
7	8	9	PAUSE
* SOFTSWITCH	0	#	LND

Figure 2. Keypad Configuration

FUNCTIONAL PIN DESCRIPTION

V+
Pin 1. V+ is the positive supply for the circuit and must meet the maximum and minimum voltage requirements. (See Electrical Specifications.)

MODE
Input. Pin 2. MODE determines the dialer's default operating mode. When the device is powered up or the hookswitch input is switched from on-hook, (V+), to off-hook, (V−), the default determines the signaling mode. A V+ connection defaults to tone mode operation and a V− connection defaults to pulse mode operation.

When dialing in the pulse mode, a softswitch feature will allow a change to the tone mode whenever the * key, or softswitch, is depressed. Subsequent * key inputs will cause the DTMF code for an * to be dialed. The softswitch will only switch from pulse to tone. After returning to on-hook and back to off-hook, the part will be in pulse mode. Redial by the LND key will repeat the softswitch.

$\overline{C1}$, $\overline{C2}$, $\overline{C3}$, $\overline{C4}$, $\overline{R4}$, $\overline{R3}$, $\overline{R2}$, $\overline{R1}$
Keyboard inputs. The MK53731 interfaces with either the standard 2-of-8 with negative common or the single-contact (Form A) keyboard.

A valid keypad entry is either a single Row connected to a single Column or V− simultaneously presented to both a single Row and Column. In its quiescent or standby state, during normal off-hook operation, either the Rows or the Columns are at a logic level 1 (V+). Pulling one input low enables the on-chip oscillator. Keyboard scanning then begins. Scanning consists of Rows and Columns alternately switching high through on-chip pullups. After both a Row and Column key have been detected, the debounce counter is enabled and any noise (bouncing contacts, etc.) is ignored for a debounce period (T_{KD}) of 32 ms. At this time, the keyboard is sampled and if both Row and Column information are valid, the information is buffered into the LND location. If switched on-hook (pin 17 to pin 1), the keyboard inputs are pull high through on-chip pull-up resistors.

In the tone mode, if 2 or more keys in the same row or if 2 or more keys in the same column are depressed a single tone will be output. The tone will correspond to the row or column for which the 2 keys were pushed. This feature is for test purposes, and single tones will not be redialed.

Also in the tone mode, the output tone is continuous in manual dialing as long as the key is pushed. The output tone duration follows the table below:

Table 1. Output Tone Duration

KEY-PUSH TIME, T*	TONE OUTPUT*
$T \leq 32$ ms	No output. Ignored by MK53731.
32 ms $\leq T \leq 75$ ms + T_{KD}	75 ms duration output.
$T \geq 75$ ms + T_{KD}	Output duration = $T - T_{KD}$

*NOTE: T_{KD} is the keypad debounce time which is typically 32 ms.

When redialing in the tone mode, each DTMF output is 75 ms duration, and the tone separation (intersignal delay) is 50 ms.

V−
Input. Pin 6 is the negative supply input to the device. This is the voltage reference for all specifications.

OSC1, OSC2
Pin 7 (input), pin 8 (output). OSC1 and OSC2 are connections to an on-chip inverter used as the timing reference for the circuit. It has sufficient loop gain to oscillate when used with a low-cost television color-burst crystal. The nominal crystal frequency is 3.579545 MHz and any deviation from this standard is directly reflected in the Tone output frequencies. The crystal oscillator provides the time reference for all circuit functions. A ceramic resonator with tolerance of ±0.25% may also be used.

DTMF OUTPUT
Output. Pin 10. An NPN transistor emitter with a collector tied to V+ drives the DTMF OUTPUT pin. The transistor base is connected to an on-chip operational amplifier that mixes the Row and Column tones. Figure 7 shows the timing at this pin.

The DTMF OUTPUT is the summation of a single Row frequency and a single Column frequency. A typical single tone sine wave is shown in Figure 4. This waveform is synthesized using a resistor tree with sinusoidally weighted taps.

The MK53731 is designed to operate from an unregulated supply; the TONE LEVEL is supply independent, and the single row tone output level will be typically:

$$T_{oi} = -12 \text{ dBm} \pm 1 \text{ dB}$$

The DC component of the DTMF output while active is described by the following equation:

$$V_{DC_1} = 0.3\ V+ + 0.5 \text{ Volts}$$

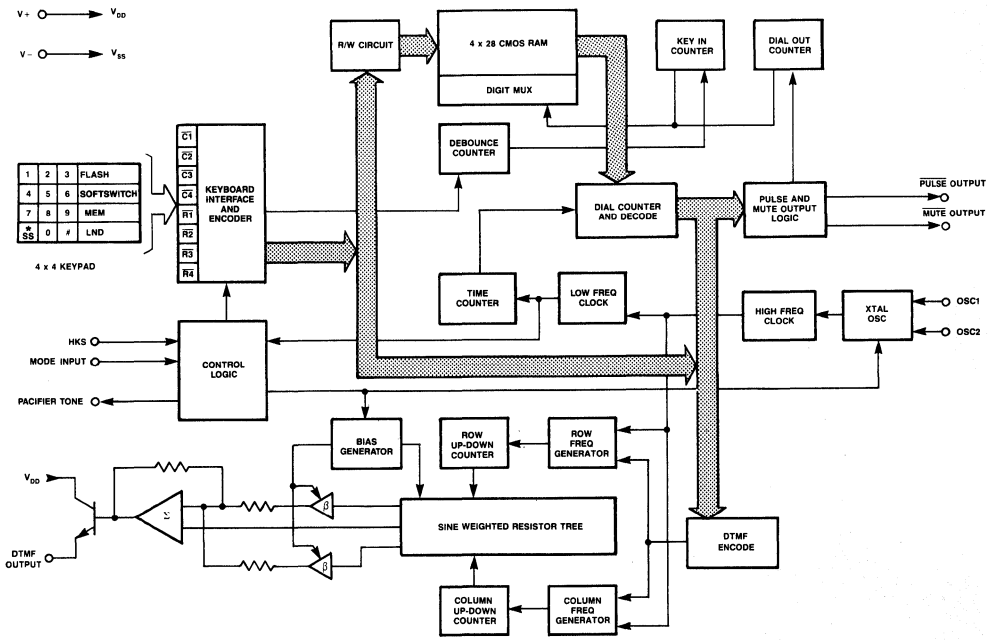


Figure 3. MK53731 Functional Block Diagram

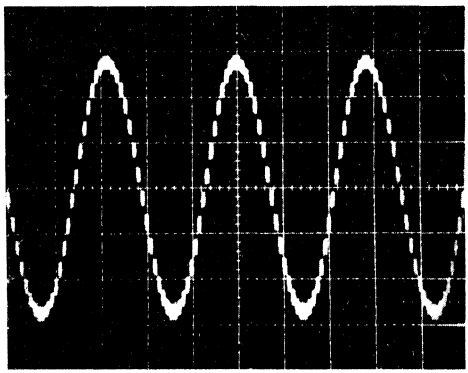


Figure 4. Typical Single Tone

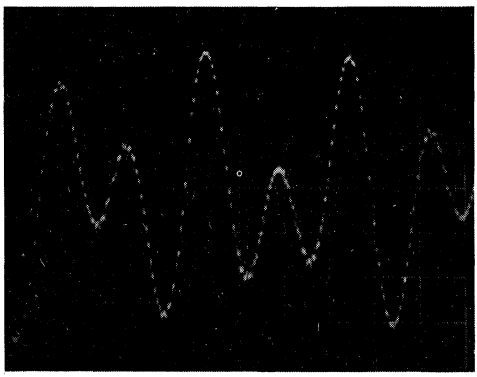


Figure 5. Typical Dual Tone

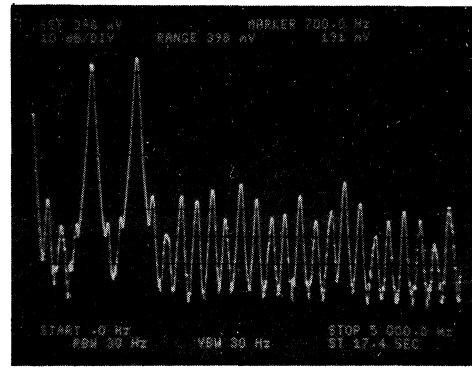


Figure 6. Typical Spectral Response

PACIFIER TONE

Output. Pin 11. A 500 Hz square wave is activated upon acceptance of a valid key input, after the 32 ms debounce time. The square wave terminates after a maximum of 30 ms or when the valid key is no longer present. In pulse mode, all valid key entries activate the pacifier tone. In tone mode, any non-DTMF (FLASH, PAUSE, LND, SOFTSWITCH) entry activates the pacifier tone. The pacifier tone provides audible feedback, confirming that the key has been properly entered and accepted.

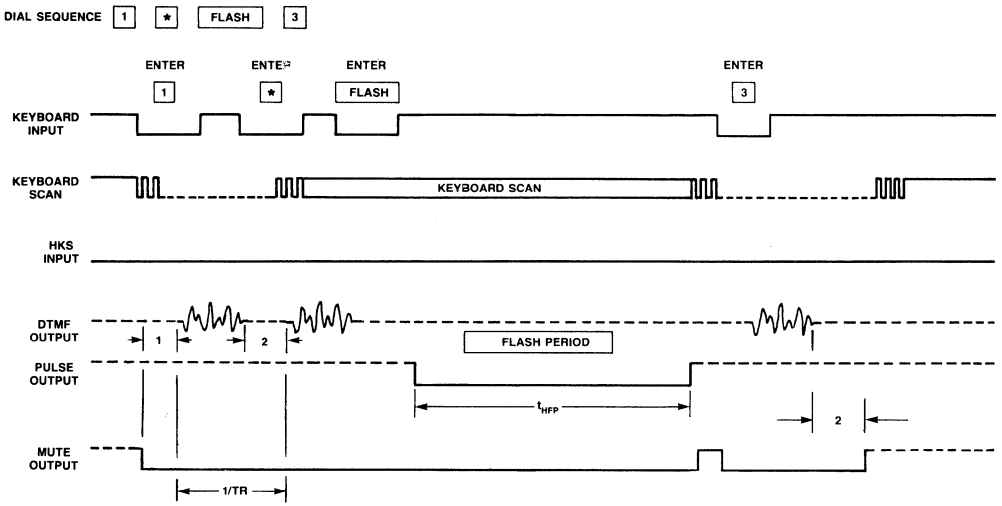
$\overline{\text{MUTE OUTPUT}}$

Output. Pin 12. This pin is the $\overline{\text{MUTE OUTPUT}}$ for both tone and pulse modes. Timing is dependent upon mode.

The $\overline{\text{MUTE OUTPUT}}$ consists of an open drain N-channel device. During standby, the output is high impedance and generally has an external pullup resistor to the positive supply.

Table 2. DTMF Output Frequency

KEY INPUT		STANDARD FREQUENCY	ACTUAL FREQUENCY	% DEVIATION
ROW	1	697	699.1	+0.31
	2	770	766.2	−0.49
	3	852	847.4	−0.54
	4	941	948.0	+0.74
COL	1	1209	1215.9	+0.57
	2	1336	1331.7	−0.32
	3	1477	1471.9	−0.35



NOTE:

For this example, key entries are ≤75 ms, but ≥32 ms.

Figure 7. Tone Mode Timing

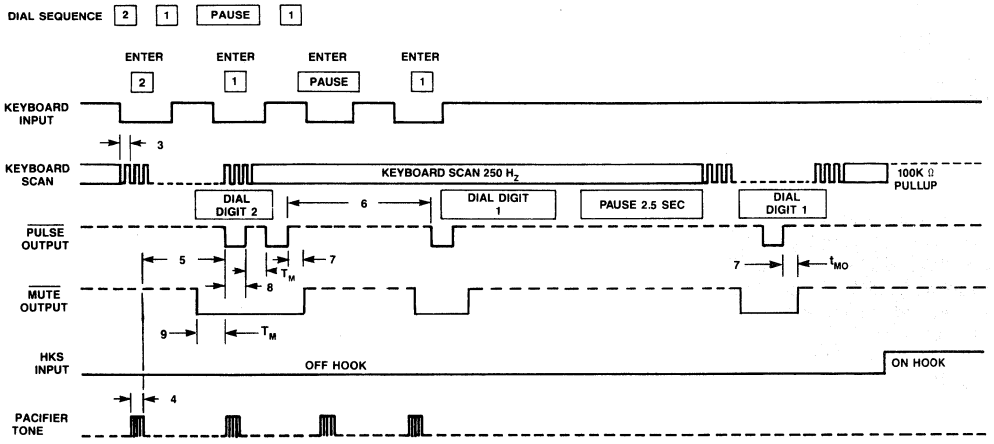


Figure 8. Pulse Mode Timing

In the tone mode, $\overline{\text{MUTE OUTPUT}}$ is used to remove the transmitter and the receiver from the network during DTMF signaling. During dialing, $\overline{\text{MUTE OUTPUT}}$ is active continuously until dialing is completed. $\overline{\text{MUTE OUTPUT}}$ goes active when any key is pushed.

In the pulse mode, $\overline{\text{MUTE OUTPUT}}$ is used to remove the receiver and the network from the line. Different circuitry is required for tone and pulse muting external to the IC and applications using both modes would not necessarily share circuitry. $\overline{\text{MUTE OUTPUT}}$ timing is shown in Figure 8 for pulse mode signaling and Figure 7 for tone mode signaling. $\overline{\text{MUTE OUTPUT}}$ is active during each digit, and not active during the interdigit time. In both tone and pulse modes, $\overline{\text{MUTE OUTPUT}}$ goes active 40 ms before $\overline{\text{PULSE OUTPUT}}$ for a FLASH.

HKS

Input. Pin 17. Pin 17 is the hookswitch input to the MK53731. This is a high-impedance input and must be switched high for on-hook operation or low for off-hook operation. A transition on this input causes the on-chip logic to initialize, terminating any operation in progress at the time. The signaling mode defaults to the mode selected at pin 2. Figure 8 illustrates the timing for this pin.

$\overline{\text{PULSE OUTPUT}}$

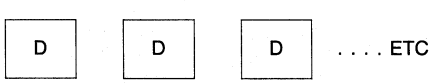
Output. Pin 18. This is an output consisting of an open drain N-channel device. In either pulse or tone mode, the FLASH key will cause a 560 ms output pulse at pin 18.

DEVICE OPERATION (Tone Mode)

When the MK53731 is not actively dialing, it consumes very little current. While on-hook, all keypad input pins are internally pulled high. Row and Column inputs assume opposite states off-hook. The circuit verifies that a valid key has been entered by alternately scanning the Row and Column inputs. If the input is still valid following 32ms of debounce, the digit is stored into memory, and dialing begins after a pre-signal delay of approximately 40 ms (measured from initial key closure). Output tone duration is shown in Table 1.

The MK53731 allows manual dialing of an indefinite number of digits, but if more than 28 digits are dialed, the 53731 will "wrap around". That is, the extra digits beyond 28 will be stored at the beginning of the LND buffer, and the first 28 digits will no longer be available for redial.

NORMAL DIALING (Off-Hook)

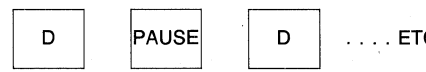


Normal dialing is straightforward, all keyboard entries will be stored in the buffer and signaled in succession.

LAST NUMBER DIALED (LND)

Last number dialing is accomplished by entering the LND key.

PAUSE



A pause may be entered into the dialed sequence at any point by keying in the special function key, PAUSE. Pause inserts a 1.1-second delay into the dialing sequence. The total delay, including pre-digital and post-digital pauses is shown in Table 3.

HOOK FLASH

Hook flash may be entered into the dialed sequence at any point by keying in the function key, FLASH. Flash consists of a timed Break of 560ms. The FLASH function is stored in memory, but it will not be redialed as such. When a FLASH key is pressed, no further key inputs will be accepted until the hookflash function (560 ms break) has been dialed. The key input following a FLASH will be stored as the initial digit of a new number (overwriting the number dialed prior to the FLASH) unless it is another FLASH. Consecutive FLASH entries after a number is dialed will be stored sequentially in the LND memory and a subsequent LND entry will cause the redial of that number with a delay, but not hookflash breaks, at the end of the redialing sequence. When redialing in tone mode, $\overline{\text{MUTE OUTPUT}}$ will remain active during the flash delay period.

SOFTSWITCH

When dialing in the pulse mode, a softswitch feature will allow a change to the tone mode whenever the * key, or SOFTSWITCH, is depressed. Subsequent * key inputs will cause the DTMF code for an * to be dialed. The softswitch will only switch from pulse to tone. After returning to on-hook and back to off-hook, the part will be in pulse mode. Redial by the LND key will repeat the softswitch.

Table 3. Special Function Delays

Each delay shown below represents the time required from after the special function key is depressed until a new digit can be dialed.

The time is considered "FIRST" key is all previous inputs have been completed dialed. The time is considered "AUTO" if in redial, or if previous dialing is still in progress.

FUNCTION	FIRST/AUTO	DELAY (seconds)	
		PULSE	TONE
SOFTSWITCH	FIRST	1.15	—
	AUTO	1.85	—
PAUSE	FIRST	1.84	1.15
	AUTO	2.50	1.20

Absolute Maximum Ratings*

DC Supply Voltage ..... 6.5 Volt
Operating Temperature ..... 0°C to +60°C
Storage Temperature ..... −55°C to +125°C
Maximum Power Dissipation (25°C) ..... 500 mW
Maximum Voltage on any Pin ..... (V+)+.3, (V−)−.3

* All specifications are for 2.5 Volt operation and full operating temperature range unless otherwise stated.

ELECTRICAL CHARACTERISTICS
DC Characteristics

SYM	PARAMETER	MIN	TYP	MAX	UNIT	NOTES
V+ TONE	DC Operating Voltage (Tone Mode)	2.5		6.0	Volts	
V_{MR}	Memory Retention Voltage	1.5	1.3		Volts	1, 6
I_s	Standby Current		0.4	1.0	μA	1
I_{MR}	Memory Retention Current		0.15	0.75	μA	5, 6
V_{MUTE}	Mute Output Operating Voltage	1.8			Volts	7
I_T	Operating Current (Tone)		300	600	μA	2
I_P	Operating Current (Pulse)		150	250	μA	2
I_{ML}	Mute Output (2.5 Volts) Sink Current (4.0 Volts)	1.0 3.0			mA mA	3
I_{PL}	Pulse Output Sink Current	1.0	2.0		mA	3
I_{PC}	Pacifier Tone Sink/Source	250	500		μA	4
K_{RU}	Keypad Pullup Resistance		100		kohm	
K_{RD}	Keypad Pulldown Resistance		500		ohm	
V_{IL}	Keypad Input Level-Low	0		0.3V+	Volt	
V_{IH}	Keypad Input Level-High	0.7V+		V+	Volt	
V_{PULSE}	Operating Voltage (Pulse Mode)	1.8		6.0	Volts	

NOTES
1. All inputs unloaded, Quiescent Mode (oscillator off)
2. All outputs unloaded, single key input
3. V_{OUT} = 0.4 Volts
4. Sink Current for V_{OUT} = 0.5 volts, Source Current for V_{OUT} = 2.0 Volts
5. Memory Retention Voltage is the point where memory is guaranteed but circuit operation is not.
6. Proper memory retention is guaranteed if either the minimum I_{MR} is provided or the minimum V_{MR}. The design does not have to provide both the minimum current or voltage simultaneously.
7. Minimum voltage where activation of mute output with key entry is ensured.

AC Characteristics - Tone Mode

NO.	SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
—	T_{NK}	Tone Output No Key Down			−80	dBm	1
—	T_{Oi}	Tone Output (independent)	−13 173	−12 194	−11 218	dBm mV_{rms}	1, 2 3
—	PE_i	Pre-Emphasis, High Band	1.6	2.0	2.4	dB	
—	DC_i	Tone Output DC Bias (V+ = 2.5) (V+ = 3.5)	 1.2	1.0		Volts Volts	
—	R_E	Tone Output Load		10		kohm	4
—	T_{RIS}	Tone Output Rise Time		1.0		ms	5
—	DIS	Output Distortion		5.0	8.0	%	3
—	TR	Tone Signaling Rate		8.0		1/sec	
1	T_{PSD}	Pre-Signal Delay	40			ms	6
2	T_{ISD}	Inter-Signal Delay (repertory)		54		ms	
	T_{DUR}	Tone Output Duration (repertory)		74		ms	

NOTES

1. O dBm equals 1 mW power into 600 ohms or 775 mVolts.
   Important Note: The MK53731 is designed to drive a 10 kohm load. The 600 ohm load is only for reference.
2. Single tone (low group), as measured at pin 10, T_A = 25°C.
3. Supply voltage = 2.5 to 6 Volts, R_E=10 kohms.
4. Supply voltage = 2.5 Volts.
5. Time from beginning of tone output waveform to 90% of final magnitude of either frequency. Crystal parameters suggested for proper operation are R_s<100 ohms, L_m=96 mH, C_m=0.02 pF, C_h=5pF, f=3.579545 MHz, and C_L=18 pF.
6. Time from initial key input until beginning of signaling.

AC Characteristics - Keypad Inputs, Pacifier Tone

(Numbers in left hand column refer to the timing diagrams.)

NO.	SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
3	T_{KD}	Keypad Debounce Time		32		ms	1
—	F_{KS}	Keypad Scan Frequency		250		Hz	1
—	F_{PT}	Frequency Pacifier Tone		500		Hz	1
4	T_{PT}	Pacifier Tone Duration		30		ms	1
—	T_{HFP}	Hookflash Timing		560		ms	1

NOTES
1. Crystal oscillator accuracy directly affects these times.

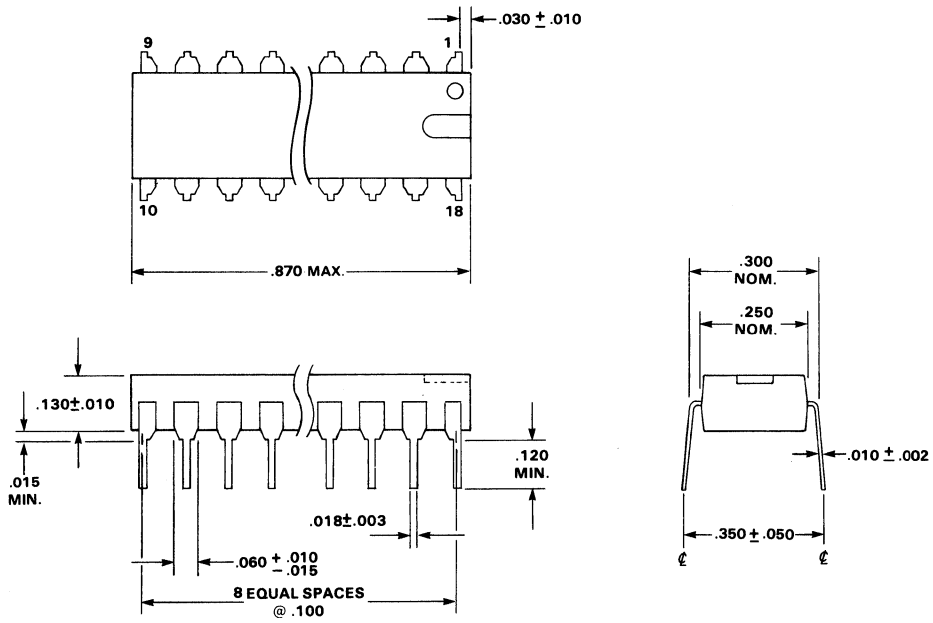
AC Characteristics - Pulse Mode Operation

NO.	SYM	PARAMETERS	MIN	TYP	MAX	UNITS	NOTES
—	P_R	Pulse Rate		10		PPS	1
5	PDP	Predigital Pause		48		ms	2
6	IDP	Interdigital Pause		740		ms	2
7	T_{MO}	Mute Overlap Time		2		ms	2
8	T_B	Break Time		60		ms	2
9	T_M	Make Time		40		ms	2

NOTES
1. 10 PPS is the nominal rate.
2. Figure 8 illustrates this relationship.

PACKAGE DESCRIPTION

18-Pin DIP (N) (.300)
Plastic



NOTE: Overall length includes .010 flash on either end of package

THOMSON COMPONENTS MOSTEK

MK5380(N,P,J)

INTEGRATED TONE DIALER

COMMUNICATIONS PRODUCTS

FEATURES

- Low standby power
- Minimum external parts count
- Uses inexpensive 3.579545 MHz television color-burst crystal to provide high-accuracy tones
- Improved loop compensation
- Distortion lower than industry standards
- Low voltage operation - 2.5 volts
- Uses low-cost calculator-type keyboard (Form A contact) or standard 2-of-8 keyboard
- Auxiliary switching functions on chip
- Multiple key entry pin-selectable to either single tone or no tone

DESCRIPTION

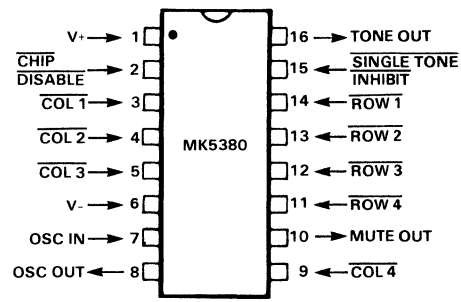
The MK5380 is a monolithic, integrated circuit fabricated using Mostek's Silicon Gate CMOS process. A member of the Tone III* family of integrated tone dialers, the MK5380 uses an inexpensive crystal reference to provide eight different audio sinusoidal frequencies, which are mixed to provide tones suitable for Dual-Tone-Multi-Frequency (DTMF) telephone dialing.

The MK5380 was designed specifically for integrated tone-dialer applications that require the following: wide-supply operation with regulated output, scanned keyboard inputs, auxiliary switching functions, and a $\overline{\text{Chip Disable}}$ input.

Keyboard entries to the MK5380 integrated tone dialer cause the selection of the proper divide ratio to obtain the required two audio frequencies from the 3.579545 MHz reference oscillator.

PIN CONNECTIONS

Figure 1



D-to-A conversion for synthesis of the tones is accomplished on chip by a sinusoidally tapped resistor tree.

Pin connections are shown in Figure 1 and a block diagram of the MK5380 is shown in Figure 2.

FUNCTIONAL DESCRIPTION

V+, Pin 1

Pin 1 is the positive supply pin. The voltage on Pin 1 should be between 2.5 and 10.0 volts, measured relative to V- (Pin 6).

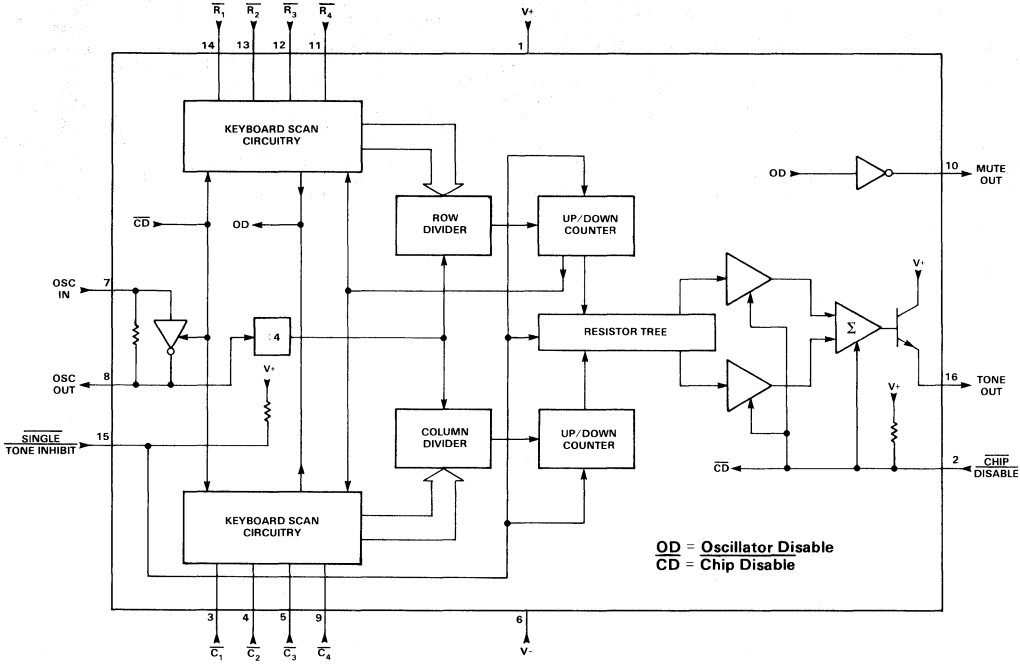
$\overline{\text{CHIP DISABLE}}$, Pin 2

When the $\overline{\text{Chip Disable}}$ input is connected to the V- supply, tone generation will be inhibited, the keyboard inputs will go to a high impedance state, and the amplifiers and oscillator will be powered down. The $\overline{\text{Chip Disable}}$ input has a pull-up resistor to the V+ supply and when floating or tied to V+, the MK5380 will operate normally.

*Trademark of Mostek Corporation

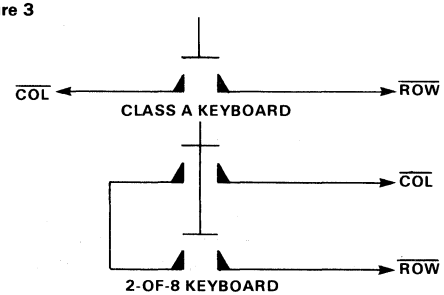
MK5380 BLOCK DIAGRAM

Figure 2



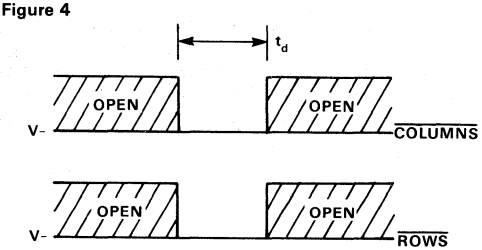
KEYBOARD CONFIGURATION

Figure 3



ELECTRONIC INPUT

Figure 4



NOTE: t_d is minimum tone duration plus oscillator start up time (t_{RISE})

FUNCTIONAL DESCRIPTION (Continued)

COL-ROW INPUTS, Pins 3, 4, 5, 9, 11, 12, 13, 14

The MK5380 features inputs compatible with the standard 2-of-8 keyboard, the inexpensive single-contact (Form A) keyboard, and electronic input. Figure 3 shows how to connect to the two keyboard types and Figure 4 shows waveforms for electronic input.

The internal structure of the MK5380 Row and Column inputs is shown in Figure 5. These inputs are designed to sense a connection between Row and Column, or an electronic input as shown in Figure 4. Table 1 is a functional truth table for these inputs. Note that at least one Row and one Column input must be active to generate a valid output.

When operating with a keyboard, normal operation is for dual-tone generation when any single button is pushed, and single-tone operation when more than one button in the same row or column is pushed. Activation of two or more diagonal buttons will result in no tones being generated.

V-, Pin 6

Pin 6 is the power supply return pin and it is the measurement reference for V+ (Pin 1).

FUNCTIONAL TRUTH TABLE

Table 1

ACTIVE LOW INPUTS		
$\overline{\text{ROW}}$	$\overline{\text{COLUMN}}$	OUTPUT
One	One	Dual Tone
Two or More	One	Column Tone
One	Two or More	Row Tone
Two or More	Two or More	No Tone

NOTE: $\overline{\text{STI}}$ is floating.
$\overline{\text{CD}}$ is floating.

OSC IN, Pin 7; OSC OUT, Pin 8

The MK5380 contains an on-board inverter with sufficient loop gain to provide oscillation when working with a low-cost television color-burst crystal. The inverter's input is Osc In (Pin 7) and output is Osc Out (Pin 8). The circuit is designed to work with a crystal cut to 3.579545 MHz to give the frequencies in Table 2. The oscillator is disabled whenever a keyboard input is not sensed.

Any crystal frequency deviation from 3.579545 MHz will be reflected in the tone output frequency. Most crystals do not vary more than ± .02%.

OUTPUT FREQUENCY DEVIATION

Table 2

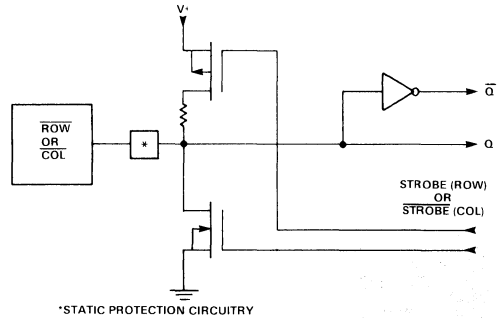
	Standard DTMF (Hz)	Tone Output Frequency Using 3.579545 MHz Crystal	% Deviation From Standard	
$\overline{\text{ROW}}$ f_1	697	699.1	+0.31	Low Group
f_2	770	766.2	-0.49	
f_3	852	847.4	-0.54	
f_4	941	948.0	+0.74	
$\overline{\text{COL}}$ f_5	1209	1215.9	+0.57	High Group
f_6	1336	1331.7	-0.32	
f_7	1477	1471.9	-0.35	
f_8	1633	1645.0	+0.73	

MUTE OUT, Pin 10

The Mute output is a conventional CMOS inverter that pulls to V- with no keyboard input and pulls to the V+ supply when a keyboard entry is sensed. This output is used to control auxiliary switching functions that are required to actuate upon keyboard input. The Mute Output switches regardless of the state of the Single Tone Inhibit input. Mute output is not affected by keyboard inputs when $\overline{\text{CD}}$ is tied to V-.

$\overline{\text{ROW}}$ AND $\overline{\text{COLUMN}}$ INPUTS

Figure 5



NOTE: Chip Disable is floating.
When $\overline{\text{CD}}$ is tied to V-, $\overline{\text{Row}}$ and $\overline{\text{Column}}$ inputs go to a high impedance state.

$\overline{\text{SINGLE TONE INHIBIT}}$, Pin 15

The $\overline{\text{Single Tone Inhibit}}$ input is used to inhibit the generation of other than dual tones. It has a pull-up to the V+ supply and, when floating, single or dual tones may be generated as described in the paragraph under $\overline{\text{Row}}$-Column inputs.

When forced to the V- supply, any time two or more rows (or columns) are activated, no tone will result.

TONE OUT, Pin 16

The Tone output pin is connected internally in the MK5380 to the emitter of an npn transistor whose collector is tied to V+. The base of this transistor is the output of the on-chip operational amplifier which mixes the row and column tones together.

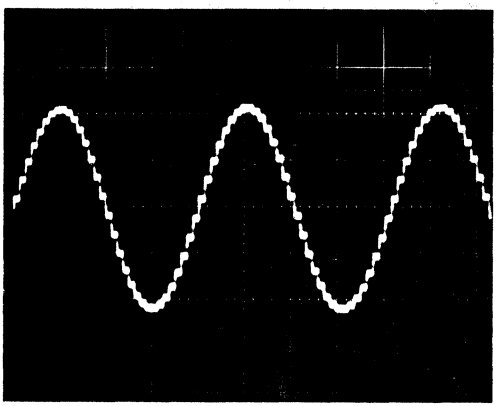
The level of a dual tone output is the sum of the levels of a single row and a single column output. This level is controlled by an on-chip reference which is not sensitive to variations in the supply voltage.

A typical single-tone sine wave output is shown in Figure 6. This waveform is synthesized using a resistor tree with sinusoidally weighted taps.

A simple measurement of distortion may be made directly from the screen of a spectrum analyzer by comparing any component to one of the fundamentals.

TYPICAL SINE WAVE OUTPUT - SINGLE TONE

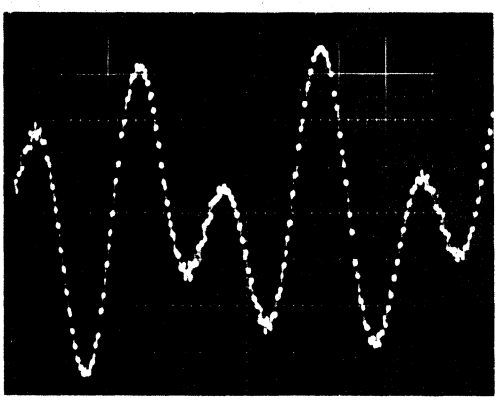
Figure 6



Figures 7 and 8 show a typical dual-tone waveform and its spectral analysis.

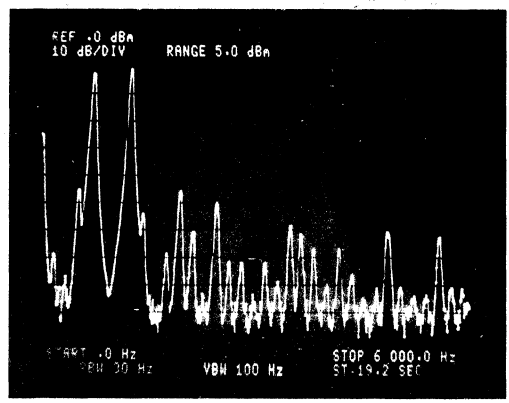
TYPICAL DUAL-TONE WAVEFORM (Row 1, Col 1)

Figure 7



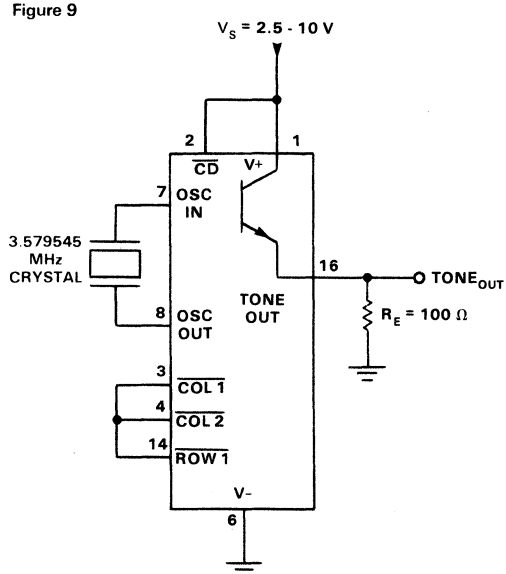
SPECTRAL ANALYSIS OF WAVEFORM IN FIG. 7 (Vert-10 dB/div. Horizontal - 600 Hz/div.)

Figure 8



TONE LEVEL TEST CIRCUIT

Figure 9



NOTE: The above circuit connections are for a Row 1 single tone test. For a Col 1 single-tone test, connect Row 1 (Pin 14) and Row 2 (Pin 13) to Col 1 (Pin 3).

ABSOLUTE MAXIMUM RATINGS*

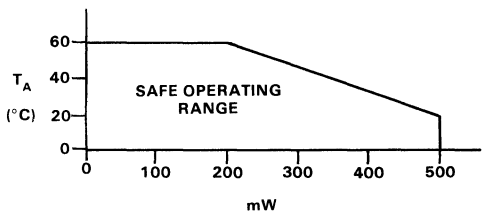
DC Supply Voltage V+ ..... 10.5 volts
Any Input Relative to V+ ..... +0.30 volts
Any Input Relative to V– ..... –0.30 volts
Operating Temperature ..... –30°C to +60°C
Storage Temperature ..... –55°C to +125°C
Maximum Circuit Power Dissipation ..... 500 mW @ 25°C (see derating curve below)

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CHARACTERISTICS

POWER DISSIPATION DERATING CURVE

Figure 10



DERATE AT 9 mW/°C WHEN SOLDERED INTO PC BOARD.

ELECTRICAL CHARACTERISTICS
DC CHARACTERISTICS
($-30°C \leq T_A \leq 60°C$)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V+	DC Operating Voltage	2.5		10.0	V	1, 2
V_{IL}	Input Voltage Low - "0"	V–		30% of V+	V	1
V_{IH}	Input Voltage High - "1"	70% of V+		V+	V	1
R_{IP}	Input Pull-Up Resistance, $\overline{STI}$, $\overline{CD}$	20		125	kΩ	
I_{SSB}	Supply Current - Standby and $\overline{CD}$ floating or tied to V+. (TA = 25°C)		0.1	2.0	μA	3,4,6
			2.0	10.0		3,4,7
I_{SO}	Supply Current - Operating ($\overline{CD}$ floating or tied to V+)		1.0	2.0	mA	3,5,6
			5.0	10		3,5,7
R_{KPU}	Keyboard Pull-Up Resistance $\overline{CD}$ tied to V+		100		kΩ	8
	$\overline{CD}$ tied to V–		10		MΩ	
R_{KPD}	Keyboard Pull-Down Resistance $\overline{CD}$ tied to V+		4.0		kΩ	8
	$\overline{CD}$ tied to V–		10		MΩ	
I_{OLM}	Output Drive, MUTE - No Entry	0.5	2.0		mA	9
		1.0	4.0			10
I_{OHM}	Output Drive, MUTE - Valid Entry	0.5	2.0		mA	11
		1.0	4.0			12

AC CHARACTERISTICS

($-30°C \leq T_A \leq 60°C$; $2.5\ V \leq V+ \leq 10.0\ V$)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
t_{RISE}	Tone Output Rise Time			5.0	ms	13,14
$TONE_{NKD}$	Tone Output-No Key Down or $\overline{CD}$ tied to V–			-80	dBm (600 Ω)	
$TONE_{OUT}$	Tone Output Voltage (Key Down and $\overline{CD}$ floating or tied to V+)	200	245	330	mV_{rms}	15, 16, 17
			155		mV_{rms}	15,18,19
PE_{HB}	Pre-Emphasis, High Band		2.0		dB	16
DIS	Output Distortion		5.0	10.0	%	16
f_{KBS}	Keyboard Scan Frequency	699		948	Hz	8

NOTES

1. All voltages referenced to V– (Pin 6).
2. 2.5 V minimum instantaneous in loop applications.
3. All outputs unloaded.
4. Current out of Pin 6, no key depressed.
5. Current out of Pin 6, one key depressed.
6. V+ = 2.5 V.
7. V+ = 10.0 V.
8. When $\overline{Row}$ or $\overline{Column}$ inputs are sensed, the keyboard inputs are alternately strobed. When a $\overline{Row}$ is strobed, the $\overline{Row}$ pull-down and $\overline{Column}$ pull-up resistances are enabled. This strobing alternates in the frequency range of 699 to 948 Hz depending on which row is selected. When no inputs exist, either a $\overline{Row}$ or a $\overline{Column}$ input will be statically sensed.
9. V+ = 2.5 V, V_{OLM} = 0.5 V.
10. V+ = 10.0 V, V_{OLM} = 0.5 V.
11. V+ = 2.5 V, V_{OHM} = 2.0 V.
12. V+ = 10.0 V, V_{OHM} = 9.5 V.
13. Time from a valid keystroke with no bounce to allow wave to go from minimum to 90% of final magnitude of either frequency.
14. Crystal parameters: $R_S \leq 100\ \Omega$, L_M = 96 mH, C_M = 0.02 pF, C_h = 5 pF, f = 3.579545 MHz, C_L = 18 pF.
15. Single-tone, low-group $T_A = 25°C$.
16. $2.5\ V \leq V+ \leq 10.0\ V$, $R_E = 100\ \Omega$ (See Figure 9).
17. $TONE_{OUT}$ measured at Pin 16 (See Figure 9).
18. $TONE_{OUT}$ (measured at Pin 16 in loop applications) = 155 mV_{rms} (typical). $R_E = 100\ \Omega$. (See Figure 11).
19. The tone level, when used in a subscriber set, is a function of the output resistor R_E and the telephone ac resistance (R_L). The low-group single-tone output amplitude is a function of R_E and R_L by the relationship:

$$\frac{V_o}{TONE_{OUT}} = \frac{1}{0.2 + \frac{R_E}{R_L}}$$

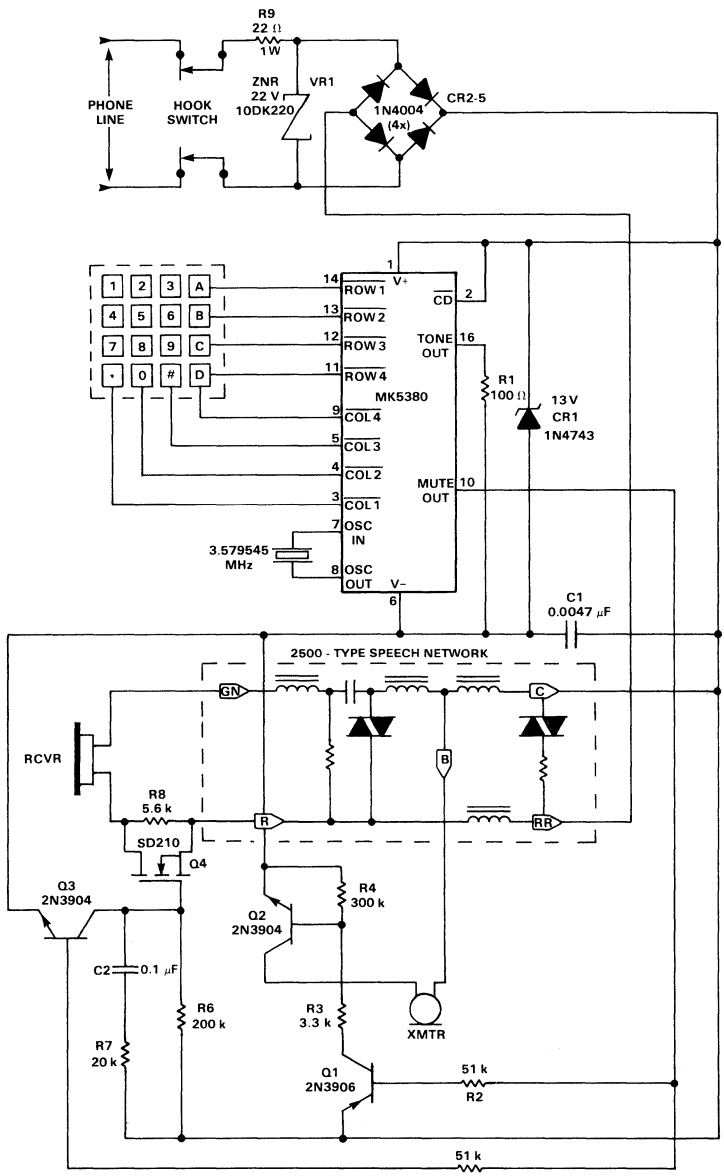
where V_o is the tone output amplitude at the phone line, and R_L is the equivalent ac impedance in shunt with the tone generator (R_L typically varies with loop current). R_E is the resistor value from $TONE_{OUT}$ to V–. In a 2500-Type application R_L will typically vary from 200 to 500 Ω. Thus, at the phone line tone output levels will range from 200 to 400 mV_{rms}, depending on loop current.

TYPICAL APPLICATION

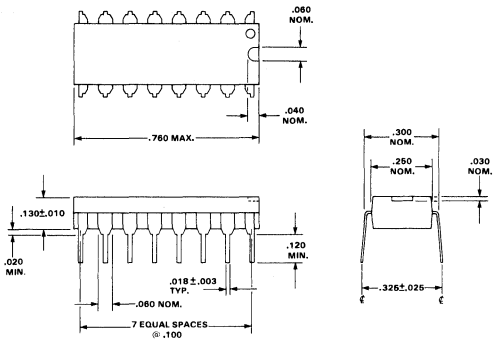
Figure 11 shows an application of the MK5380 in a standard telephone set that uses the standard 2500-Type Speech Network.

TYPICAL APPLICATION IN 2500-TYPE TELEPHONE

Figure 11

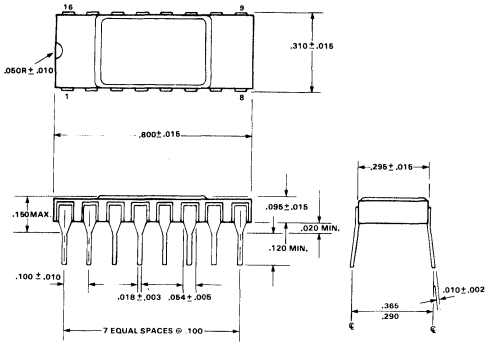


PACKAGE DESCRIPTION
Plastic Dual-In-Line (N)
16-Pin
MK5380N



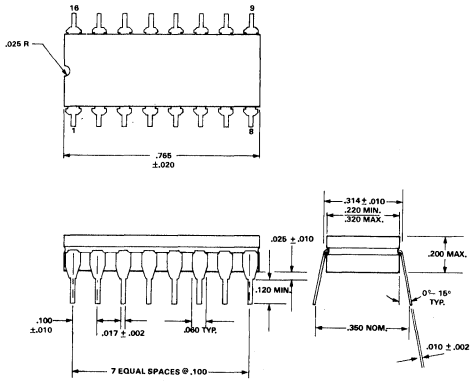
NOTE: Dimensions are in inches.

PACKAGE DESCRIPTION
Side-Braze Ceramic (P)
16-Pin
MK5380P



NOTE: Dimensions are in inches.

PACKAGE DESCRIPTION
Cerdip (J)
16-Pin
MK5380J



NOTE: Dimensions are in inches.

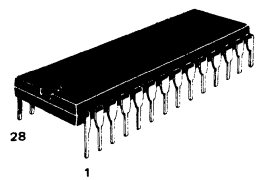
TELEPHONE LOW-COST MONOCHIP

Specially designed for a basic low cost telephone set application, this 28-pin IC provides transmission and line adaptation, DTMF generation and power supply for peripheral circuits. Interface is also possible with a microcomputer for a more sophisticated set.

- Low working voltage
- Wide operation current range
- Adjustable automatic line length receiving and sending gain control
- Adjustable automatic line length tracking anti-sidetone system
- Adjustable dynamic impedance
- Microphone preamplifier compatible with both symmetrical and asymmetrical inputs
- Adjustable microphone amplifier gain
- Adjustable earphone amplifier gain
- Low send and receive noise
- Click-free switch-over from speech mode to dialling mode & vice-versa
- Silent position facility
- Single-tone facility
- Two keys roll over provided
- Switch bounce elimination
- Microcomputer interface available
- Adjustable output tone level
- Temperature independent output level
- Inputs protected against electrostatic discharge
- Power supply for peripheral circuits.
- Soon available in S028 plastic micropackage

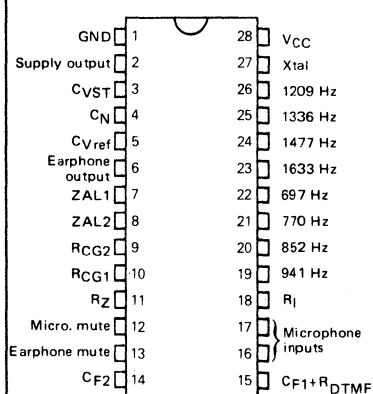
TELEPHONE LOW-COST MONOCHIP

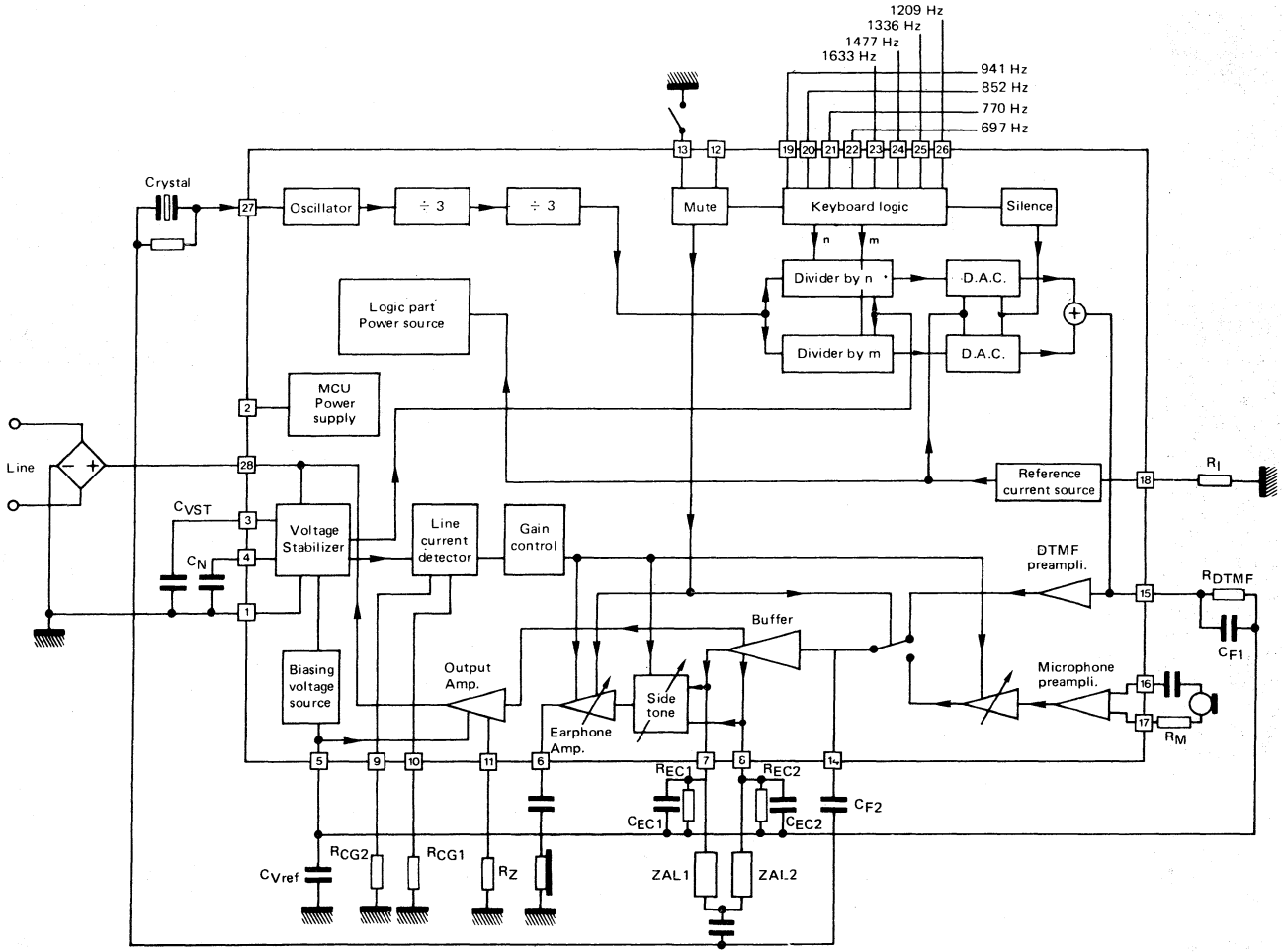
CASE CB-132



DP SUFFIX
PLASTIC PACKAGE

PIN ASSIGNMENT




1209 Hz
1336 Hz
1477 Hz
1633 Hz
941 Hz
852 Hz
770 Hz
697 Hz
Crystal
Oscillator
÷ 3
÷ 3
Mute
Keyboard logic
Silence
n
m
Divider by n
Divider by m
D.A.C.
D.A.C.
Logic part Power source
MCU Power supply
Line
Reference current source
R_I
C_{VST}
C_N
Voltage Stabilizer
Line current detector
Gain control
DTMF preampli.
R_{DTMF}
C_{F1}
Buffer
Biasing voltage source
Output Amp.
Earphone Amp.
Side tone
Microphone preampli.
R_M
R_{EC1}
R_{EC2}
C_{EC1}
C_{EC2}
C_{F2}
C_{Vref}
R_{CG2}
R_{CG1}
R_Z
ZAL1
ZAL2

PIN DESCRIPTION

Name	No	Description
G_{ND}	1	Ground
Supply output	2	Power supply output
C_{VST}	3	C_{VST} decouples the voltage stabilizer
C_N	4	Capacitor to reduce the noise
C_{Vref}	5	C_{Vref} decouples the biasing voltage. This reference biasing voltage is temperature independant.
Earphone output	6	Earphone amplifier output
Z_{AL1}	7	Short line antisidetone circuit Z_{AL1} and earphone amplifier input.
Z_{AL2}	8	Long line antisidetone circuit Z_{AL2} and earphone amplifier input.
R_{CG2} R_{CG1}	9 10	R_{CG2} fixes gain control (see note 4). R_{CG1} fixes gain control (see note 4).
R_Z	11	R_Z fixes the impedance value of the circuit.
Earphone output	12	A short circuit to the ground on this pin mutes the earphone signal.
Micro mute	13	A short circuit to the ground on this pin mutes the microphone signal.
C_{F2}	14	C_{F2} filters both microphone and DTMF signals.
$C_{F1} + R_{DTMF}$	15	C_{F1} and R_{DTMF} filter the DTMF signal & set DTMF signal level..
Microphone inputs	16-17	
R_I	18	$V_{ref.}$ voltage on this pin is temperature stable.
941 Hz	19	"D" logic input. 941 Hz keyboard row.
852 Hz	20	"C" logic input. 852 Hz keyboard row.
770 Hz	21	"B" logic input. 770 Hz keyboard row.
697 Hz	22	"A" logic input. 697 Hz keyboard row.
1633 Hz	23	"H" logic input. 1633 Hz keyboard column.
1477 Hz	24	"G" logic input. 1477 Hz keyboard column.
1336 Hz	25	"F" logic input. 1336 Hz keyboard column.
1209 Hz	26	"E" logic input, 1209 Hz keyboard column.
X_{tal}	27	Oscillator input
V_{CC}	28	

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply voltage	V_{CC}	+8.5	V
Power dissipation	P_{tot}	700	mW
Operating temperature range	T_{aper}	−25 to 65	°C
Storage temperature range	T_{stg}	−55 to 150	°C

STATIC ELECTRICAL CHARACTERISTICS

$-25°C \leq T_{amb} \leq +65°C$
Line impedance $Z_L = 600\ \Omega$

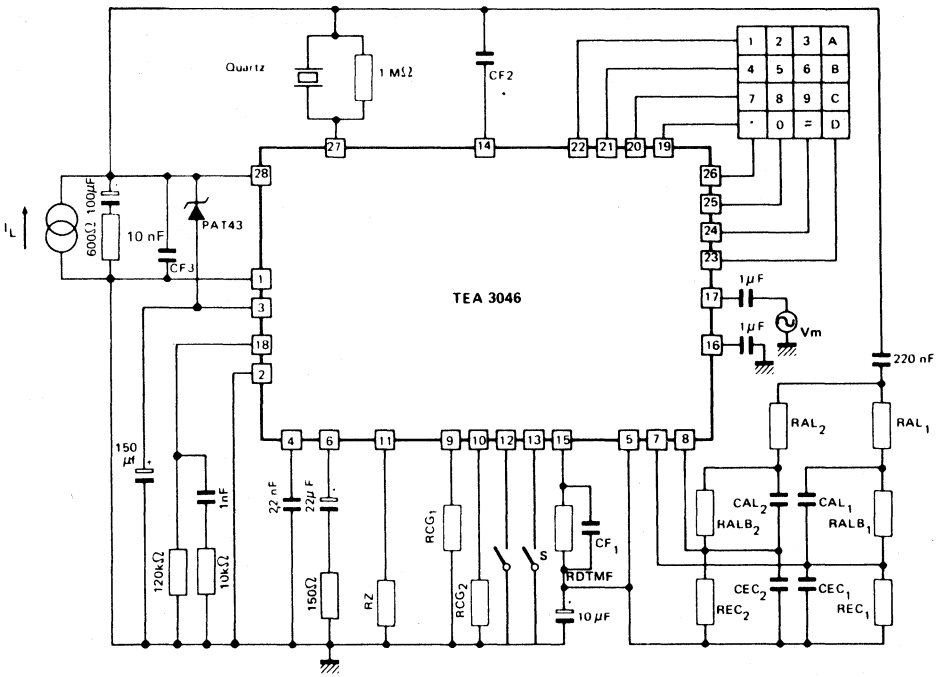
Characteristic	Symbol	Min	Typ	Max	Unit
Line current (pin 28)	–	–	–	–	mA
MPU supply OFF	I_L	15	–	150	
MPU supply ON	I_L	17	–	150	–
Voltage over the I_C (pin 28)	–	–	–	–	V
I_L = 15 mA	V28	3.9	4.6	5.1	–
I_L = 100 mA	V28	–	–	7	–
Voltage stabilizer (pin 3)	–	–	–	–	V
I_L = 15 mA	V_C	–	2.7	–	–
I_L = 100 mA	V_C	–	3.7	–	–
Power supply (pin 2)	–	–	–	–	mA
max current (V2 = 3.2 V)					
Sending mode V28 = 5dBm	I2	0.6	–	–	–
Without A_C line signal	I2	1	1.2	–	–

DYNAMIC ELECTRICAL CHARACTERISTICS

T_{amb} = + 25°C
Line impedance Z_L = 600 Ω
F = 1 kHz

Characteristic	Symbol	Min	Typ	Max	Unit
Max sending gain	–	–	–	–	
R_M = 0 (No gain control action note 1)	G_S max	49.5	50.5	51.5	dB
Gain control					
Sending gain decrease (Note 1)	–	5	6	7	dB
Common mode rejection ratio (G_S max)	C_{MR}	50	60	–	dB
Line signal distortion MPU supply ON					
V28 ⩽ 3.5 dBm	–	–	–	5	%
V28 ⩽ 5.5 dBm	–	–	–	10	–
Line signal distortion MPU supply OFF					
V28 ⩽ 3.5 dBm	–	–	–	2	%
V28 ⩽ 5.5 dBm	–	–	–	10	–
Imput impedance					kΩ
Symetrical mode (pin 16.17)	Zes	1.5	2	2.5	–
Asymetrical mode (pin 16)	Zea	0.7	1	1.3	–
Asymetrical mode (pin 17)	Zea	5	7	9	–
Transmission noise level (pin 28) (Psyphometric R_M = 200 Ω	–	–	– 65	–	dBmp
Gain reduction during dialing (Note 1)	–	50	–	–	dB
2 wires to 4 wires conversion efficiency (Note 2 – Reception gain from line to earphone is o dB: V28/ V26 = 1)					dB
I_L = 30 mA • Z_L = 600 Ω	E	15	–	–	–
I_L = 87 mA • Z_L = Z_{LL}	E	15	–	–	–
Earphone amplifier (Note 3)					dB
Max gain (no gain control I_L = 30 mA • G_R = V6/ V8)	G_R max	19	20	21	–
Gain control (Reception gain decrease)	GR	5	6	7	–
Earphone signal distortion (R earphone > 150 Ω • V6 = – 10 dBV)	–	–	–	3	%
Output noise level	–	–	65	–	dBmp
Impedance: depends on external component, R_Z (Z = (V28/ I28) A_C and R_Z pin 11 = 75 Ω)	Z	500	600	700	Ω
DTMF Grenerat or (note 4)					
Crystal oscillator frequency	–	–	3.579545	–	MHz
Tone frequency accuracy	–	– 1.5	–	+ 1.5	%
Low group tone level (depends on external components)	–	– 11	–	– 6	dBm
High group tone level (depends on external components)	–	– 9	–	– 4	dBm
Preemphasis (depends on external components)	–	+ 1	+ 2	+ 3	dB
Distortion DTMF signal (depends on external components)	–	–	–	– 26	dB
DTMF signal level spread (depends on external components)	–	– 2	–	+ 2	dB
Logic inputs (note 5) keyboard mode					
Switch bounce elimination	–	0.5	–	–	ms
Keyboard contact resistance "ON"	–	–	–	10	kΩ
Keyboard contact resistance "OFF"	–	500	–	–	kΩ
Logic inputs (note 6) M_{PU} mode					
Current drawn by A.B.C. and D input to go low	–	–	20	50	μA
Current to force inputs E.F.G and H to go high	–	–	20	50	μA
Input impedance	–	–	5	–	kΩ
Input max voltage on A.B.C.D. or E.F.G.H. inputs	–	0	–	V28	V

Note 1: Transmission mode - test diagram



External components:

RAL1 = RAL2 = 0
CAL1 = CAL2 = 47 pF
RALB1 = RALB2 = 56 kΩ
REC1 = REC2 = 6.2 kΩ
CEC1 = CEC2 = 2.2 nF
RDTMF = 511 Ω CF1 = 106 nF CF2 = 10 nF
RZ = 75 Ω
RCG1 = 60 kΩ RCG2 = 14 kΩ

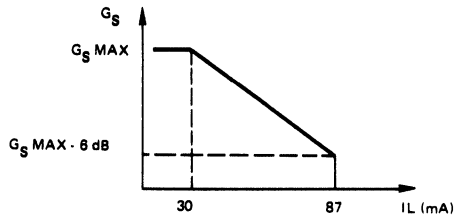
Note 1: test conditions (continued)

Maximum transmission gain for IL = 30 mA

$$GS_{max} = \frac{V28}{Vm}$$

Gain control:

- For IL = 30 mA: GS = GS_{max}.
- For IL = 87 mA: GS = GS_{max} — 6 dB.



- For other values of line current and corresponding values of RCG1 and RCG2: see application note.

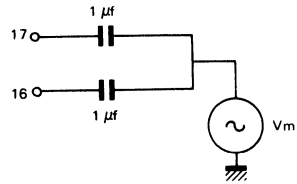
Gain reduction during dialing

- Close swith S (pin 13).

CMRR

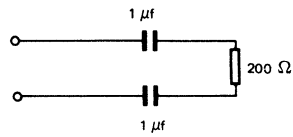
- For IL = 30 mA.

$$GSCM = \frac{V28}{Vm} \quad CMRR = \frac{GS_{max}}{GSCM}$$

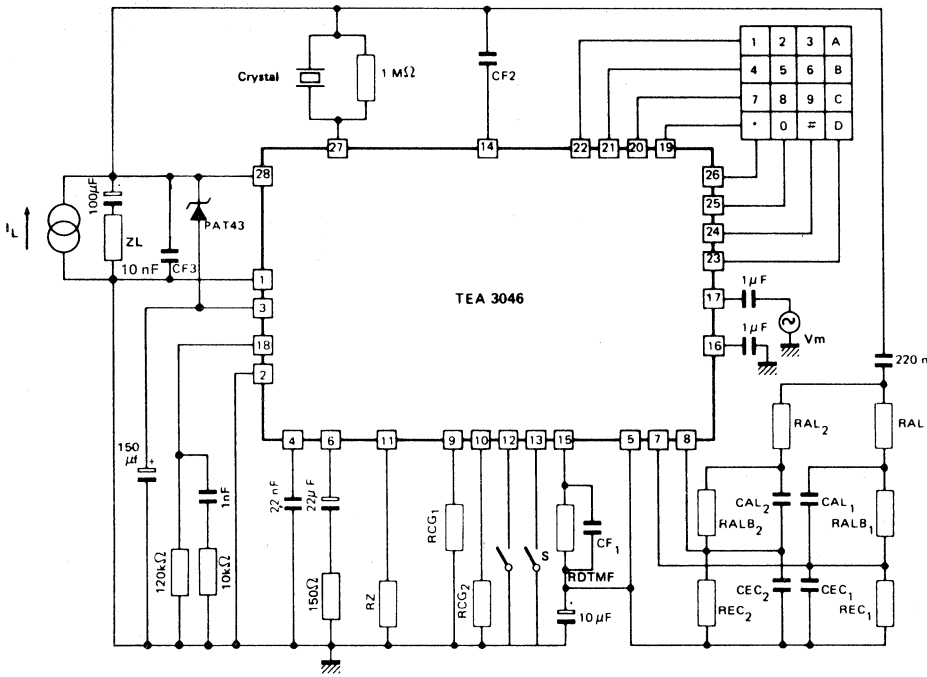


Transmission noise level:

- Measured on pin 28 with IL = 30 mA and the corresponding diagram on the microphone inputs.



Note 2: Antisidetone - test diagram



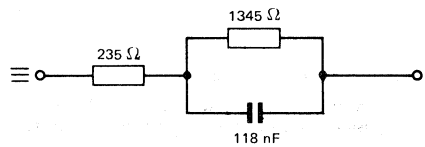
External components:

RZ = 75 Ω RDTMF = 511 Ω CF1 = 106 nF CF2 = 10 nF
RCG1 = 60 kΩ RCG2 = 14 kΩ
RAL1 = 0 RALB1 = 56 kΩ CAL1 = 47 pF REC1 = 6.2 kΩ CEC1 = 2.2 nF
RAL2 = 28 kΩ RALB2 = 51 kΩ CAL2 = 1.15 nF REC2 = 2.7 kΩ CEC2 = 2.2 nF

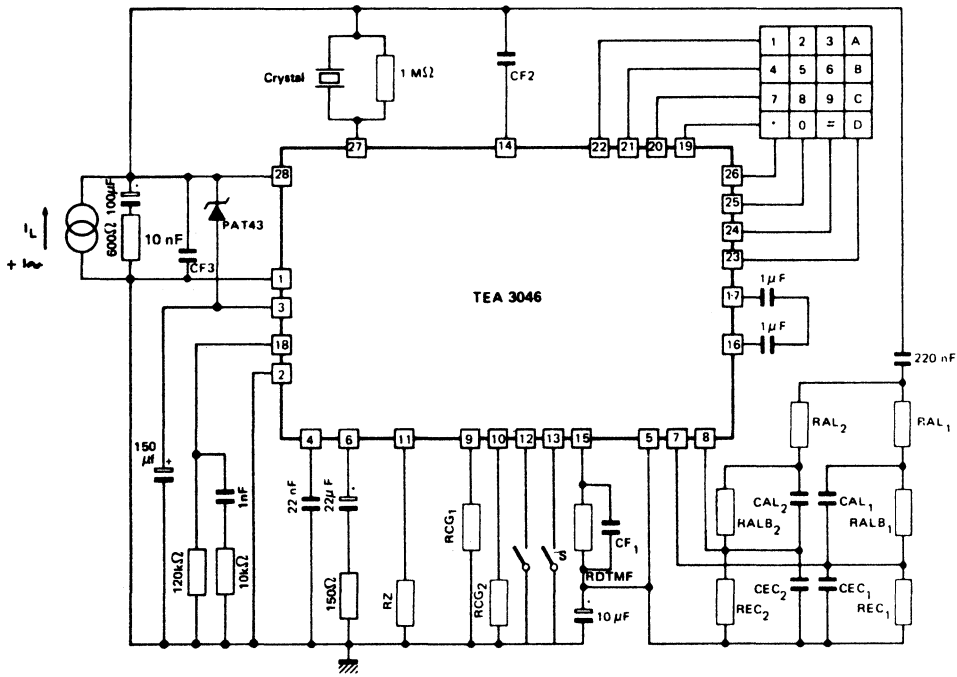
Test conditions:

- Short line: IL = 87 mA ZL = 600 Ω
- Long line: IL = 30 mA ZL = ZLL
  ZLL represents a line 3.5 kilometers long with a diameter = 0.4 mm.
  Antisidetone efficiency:

$$E = 20 \log_{10} \left(\frac{V6}{V28} \right)$$



Note 3: Receiving mode - Test diagram



External conponents:

RAL1 = RAL2 = 0 CAL1 = CAL2 = 47 pF RALB1 = RALB2 = 56 kΩ CEC1 = CEC2 = 62 kΩ
REC1 = REC2 = 2.2 nF RZ = 75 Ω RCG1 = 60 kΩ RCG2 = 14 kΩ RDTMF = 511 Ω
CF1 =106 nF CF2 = 10 nF

Test conditions:

Maximum receiving gain:

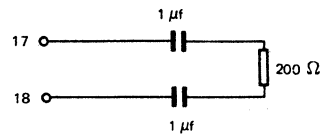
- For I_L = 30 mA $GR_{max} = \frac{V6}{V8}$

Gain control:

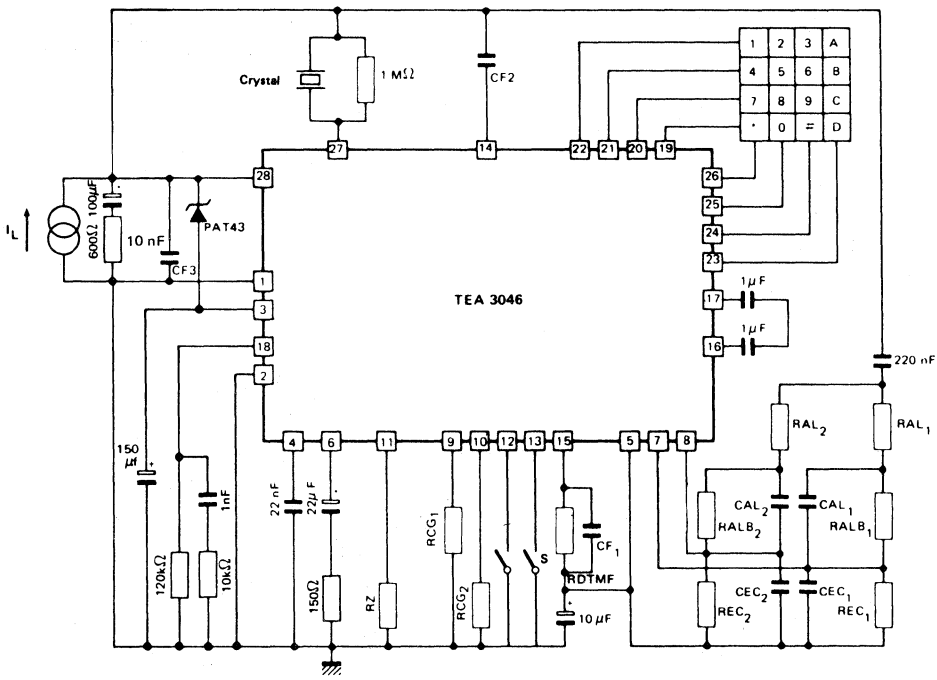
- For IL = 30 mA GR = GR_{max}
- For IL = 87 mA GR = GR_{max} — 6 dB

Output noise level:

- Measured on pin 6, with the corresponding diagram on microphone inputs.



Note 4: DTMF - Test diagram



External conponents:

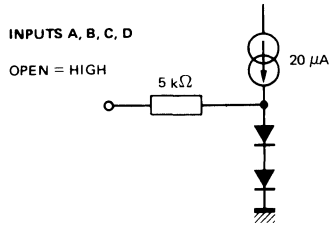
RAL1 = RAL2 = 0 CAL1 = CAL2 = 47 pF RALB1 = RALB2 = 56 kΩ
CEC1 = CEC2 = 62 kΩ REC1 = REC2 = 2.2 nF
RZ = 75 Ω RCG1 = 60 kΩ RCG2 = 14 kΩ
RDTMF = 511 Ω CF1 =100 nF CF2 = 10 nF
IL = 30 mA

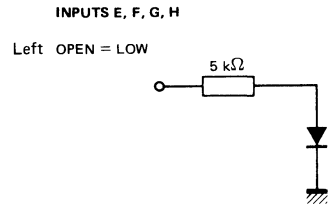
Frequency accuracy, tone levels, preemphasis, distortion can be measured by putting the right code on the logic inputs for every couple of frequencies. See note 5 and 6.

Remaining receiving gain during dialing: the circuit must be in test mode (single-tone).
Remaining gain = 20 $\log_{10}$ (V6/V28).

Note 5: Logic inputs table - Keypad mode

EQUIVALENT DRAWING OF LOGIC INPUTS





Inputs								Generated tones (Hz)	Symbol	Mute	Notes
A	B	C	D	E	F	G	H				
H	H	H	H	L	L	L	L	–	–	off	5.1
L	H	H	H	L	L	L	L	697	–	on	5.2
H	L	H	H	L	L	L	L	770	–	on	
H	H	L	H	L	L	L	L	852	–	on	
H	H	H	L	L	L	L	L	941	–	on	
H	H	H	H	H	L	L	L	1 209	–	on	5.3
H	H	H	H	L	H	L	L	1 336	–	on	
H	H	H	H	L	L	H	L	1 447	–	on	
H	H	H	H	L	L	L	H	1 633	–	on	
L				H				697 + 120	"1"	on	5.4
L					H			697 + 1 336	"2"	on	
L						H		697 + 1 477	"3"	on	
L							H	697 + 1 633	"A"	on	
	L			H				770 + 1 209	"4"	on	
	L				H			770 + 1 336	"5"	on	
	L					H		770 + 1 477	"6"	on	
	L		•				H	770 + 1 633	"B"	on	
		L		H				852 + 1 209	"7"	on	
		L			H			852 + 1 336	"8"	on	
		L				H		852 + 1 477	"9"	on	
		L					H	852 + 1 633	"C"	on	
			L	H				941 + 1 209	"*"	on	
			L		H			941 + 1 336	"0"	on	
			L			H		941 + 1 477	"#"	on	
			L				H	941 + 1 633	"D"		

Note 5.1: Speech mode.

Note 5.2: Test mode.
Low group tones.

Note 5.3: Test mode.
High group tones.

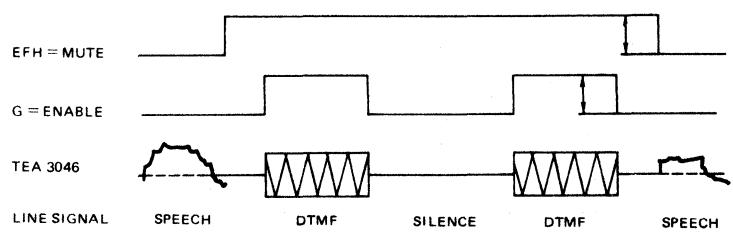
Note 5.4: This table is only valid if E,F,H, = low.
As soon as one of the inputs E,F,G,H, is high, the others are considered low.
As soon as one of the inputs A,B,C,D, is low, the others are considered high.

Note 6: Logic inputs table - Microprocessor mode

Inputs								Generated tones (Hz)	Symbol	Mute	Notes
A	B	C	D	E	F	H	G				
H	H	H	H		L		L	–	–	off	6.1
X	X	X	X		H		L	–	–	on	6.2
H	H	H	H		H		H	697 + 1 209	"1"	on	6.3
H	H	H	L		H		H	697 + 1 336	"2"	on	
H	H	L	H		H		H	697 + 1 477	"3"	on	
H	H	L	L		H		H	697 + 1 633	"A"	on	
H	L	H	H		H		H	770 + 1 209	"4"	on	
H	L	H	L		H		H	770 + 1 336	"5"	on	
H	L	L	H		H		H	770 + 1 477	"6"	on	
H	L	L	L		H		H	770 + 1 633	"B"	on	
L	H	H	H		H		H	852 + 1 209	"7"	on	
L	H	H	L		H		H	852 + 1 336	"8"	on	
L	H	L	H		H		H	852 + 1 477	"9"	on	
L	H	L	L		H		H	852 + 1 633	"C"	on	
L	L	H	H		H		H	941 + 1 209	"*"	on	
L	L	H	L		H		H	941 + 1 336	"0"	on	
L	L	L	H		H		H	941 + 1 477	"#"	On	
L	L	L	L		H		H	941 + 1 633	"D"	on	

Note 6.1: Speeck mode.
Note 6.2: Silence position.
Note 6.3: Mute coincides with tone borsts.

Impedance mute or silent setting



FUNCTIONAL DESCRIPTION

TRANSMISSION AND LINE ADAPTATION

Includes microphone and telephone amplification, both with line length depending gain control and a line impedance automatic matching 2-wire to 4-wire conversion.

The microphone preamplifier performs high CMRR, for crosstalk and radio detection immunity and low noise characteristic. Its architecture allows symmetrical and asymmetrical inputs and external adjustment of gain to fit difference microphone capsules. A single pole filter limits the amplifier bandwidth for a best high frequency figure.

The earphone amplifier is a low consumption type. It is click free when muted and its gain can be externally adjusted.

2-wire to 4-wire conversion is performed by subtracting microphone signal from line before applying it to earphone amplifier. An automatic line impedance tracking antisidetone circuit provides excellent sidetone efficiency for every line length.

The dynamic impedance of the circuit is set by an external resistor to match with different line impedances.

The line length is sensed through the line current. 2 external components allow the gain control to compensate any kind of line length and feeding bridge.

DTMF SIGNAL GENERATION

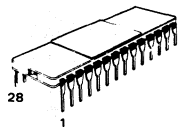
Tones are obtained from a crystal controlled oscillator followed by two independent programmable dividers and 2 sinewave synthetizers. The crystal is a low-cost TV model 3.58 MHz oscillator.

The amplitude of the multi-frequency signal is set by an external resistor.
The required tone frequencies are selected by either an inexpensive single contact 4 x 4 keypad or by a microcomputer. Single-tone operation for testing is also provided.

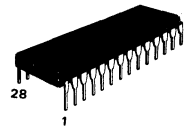
THE POWER SUPPLY

This is 0.6 mA current source with a typ max voltage compliance of a 3.2 V.
It can power either and electret microphone or a microprocessor.
If this source is not used, pin 2 is connected to ground to reduce the ICC (pin 28) current.

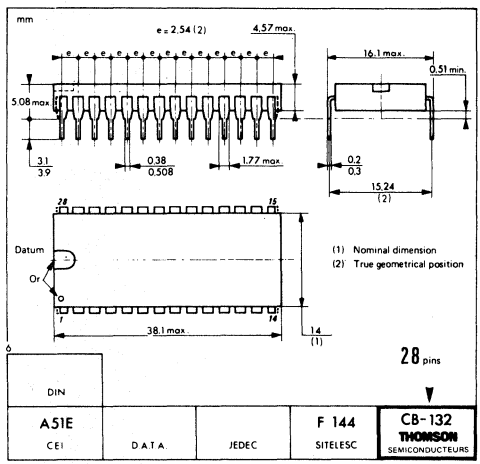
CASE CB-132



C SUFFIX
CERAMIC PACKAGE



P SUFFIX
PLASTIC PACKAGE



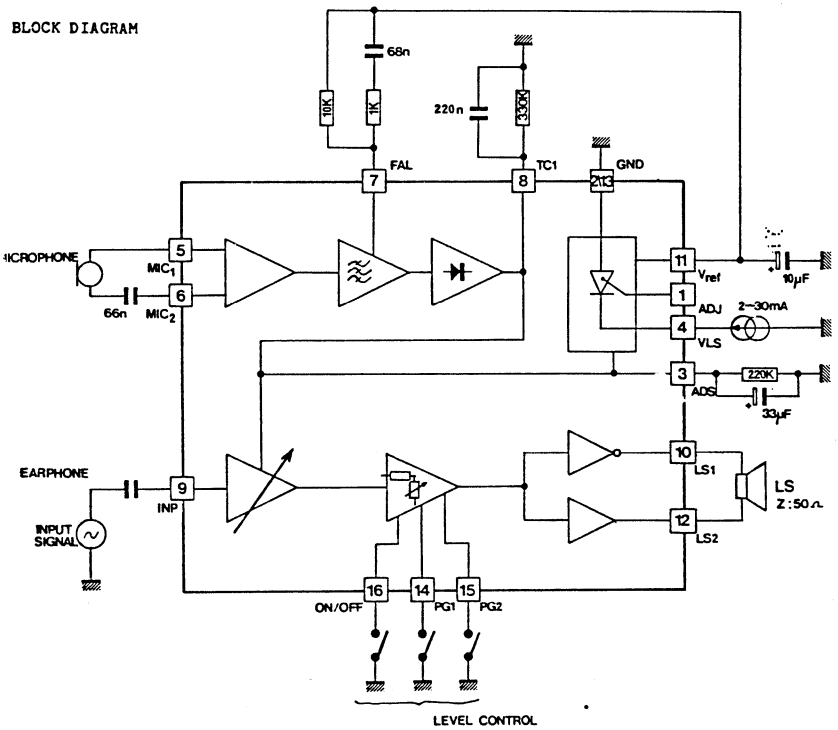
TEA 7531
TELEPHONE SET LOUDSPEAKER AMPLIFIER

The TEA7531 is a 16-pin DIL integrated circuit especially designed to be used as a loudspeaker amplifier. It is the same as the TEA7031 but without the switching supply for MCU.

Functions and features implemented on the chip include:

- Amplifying the incoming signal and feeding it to the loudspeaker. PG0 and PG1 inputs are used to set the loudspeaker gain in a range of 32dB to 14dB in 6dB steps.
- Permitting the loudspeaker to be cut-off thus ensuring privacy of communication.
- Incorporating the antilarsen (Anti acoustic feedback) system.
- Producing maximum output power of 100 mW at 5 V or 25 mW at 3 V (into a 50 Ohms loudspeaker).

BLOCK DIAGRAM



CHAPTER 6 - HIGH SPEED DATA CONVERSION

THOMSON COMPONENTS
MOSTEK

TS8306

20 MHz 6-BIT FLASH A/D CONVERTER

COMMUNICATIONS PRODUCTS

PRODUCT PREVIEW

VIDEO SPEED 6-BIT FLASH A/D CONVERTER

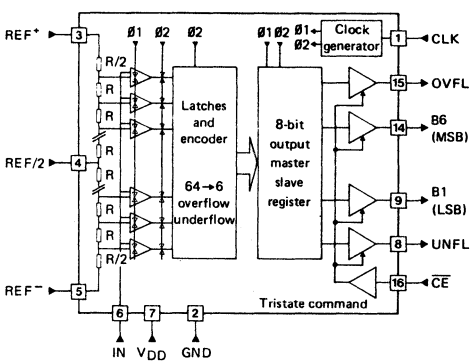
The TS8306 is a monolithic 6 bit HMOS2 parallel (flash) A/D converter designed for 20 MSPS conversion speed.
Parallel sampling is performed via a resistor ladder and 64 auto-balanced comparators. Conversion is accomplished within one clock pulse.

A very low input capacitance (less than 15 pF) and a low input dynamic range (1 volt possible) allow very easy drive of the TS8306.

- 20 MHz sampling rate.
- 10 MHz input bandwidth without sample and hold.
- Accuracy better than 6 mV (operation at low reference possible).
- Single +5V supply.
- Logic inputs and outputs are TTL and CMOS compatible.
- 6 bit data, underflow and overflow lines are 3-state outputs.
- 16 pin package (chip also available).
- Very low cost device.
- Soon available in SO16 plastic micropackage.

- High speed data acquisition.
- TV video digitizing.
- Radar pulse analysis.
- Medical imaging.
- General purpose hybrid ADC's.
- Optical recognition.
- Fax machine and video printer.
- All high speed A/D conversion applications where low power and low cost are required.

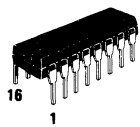
BLOCK DIAGRAM



HMOS2

20 MHz
6-BIT FLASH
A/D CONVERTER

CASE CB-79

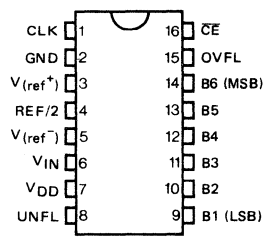


P SUFFIX
PLASTIC PACKAGE

ALSO AVAILABLE

C SUFFIX	J SUFFIX
CERAMIC PACKAGE	CERDIP PACKAGE

PIN ASSIGNMENT



PIN DESCRIPTION

NAME	PIN TYPE	N°	FUNCTION	DESCRIPTION
CLK	I	1	Clock input	TTL level accepted
GND	I	2	General ground	Inside, analog and digital ground are separated.
$V_{(ref^+)}$	I	3	Upper reference	Access to the upper resistance ladder
REF/2	I	4	Middle reference	Access to the middle resistance ladder. The conversion law can be changed by forcing this point by an external voltage source.
$V_{(ref^-)}$	I	5	Lower reference	Access to the lower resistance ladder.
V_{IN}	I	6	Analog input	
V_{DD}	I	7	Positive supply	Inside, analog and digital supply are separated.
UNFL	O	8	Under flow status line	This line is set to logical "1" when the input signal is lower than the $V_{(ref^-)}$ voltage. All data (B1 to B6) are reset to logical "0".
B1 (LSB) to B6 (MSB)	O	9 to 14	Output data	
OVFL	O	15	Overflow status line	This line is set to logical "1" when the input signal is higher than the $V_{(ref^+)}$ voltage ; all data (B1 to B6 are set to logical "1".
$\overline{CE}$	I	16	Tristate enable	$\overline{CE}$ commands the tristate mode for all output buffers (B1 to B6, OVFL and UNFL). When $\overline{CE}$ = "1" : tristate $\overline{CE}$ = "0" : output valid

MAXIMUM RATINGS

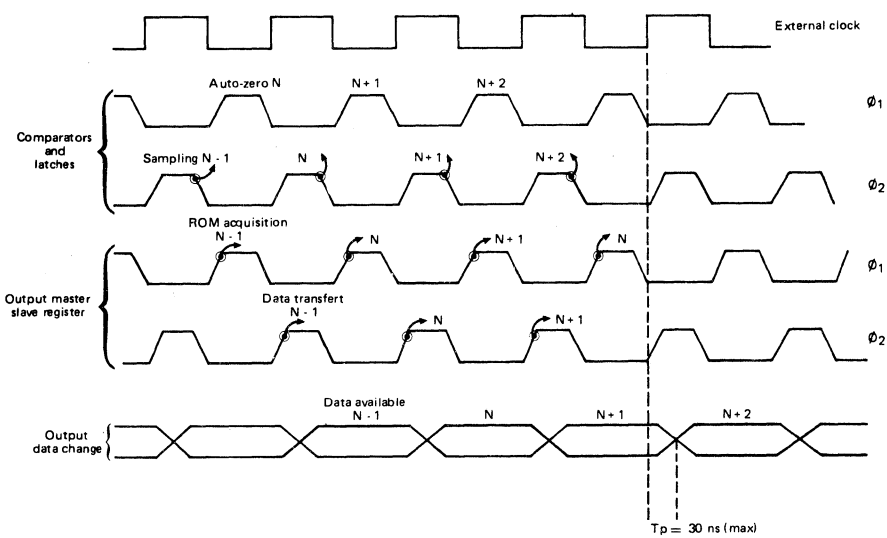
Rating	Symbol	Value	Unit
Supply voltage	V_{DD}	0 to + 7	V
Storage temperature	T_{stg}	- 60 to + 150	°C
Operating temperature	T_{amb}	- 60 to + 130	°C
Power supply current on pins (2, 7)	I_7, I_2	150	mA

ELECTRICAL CHARACTERISTICS

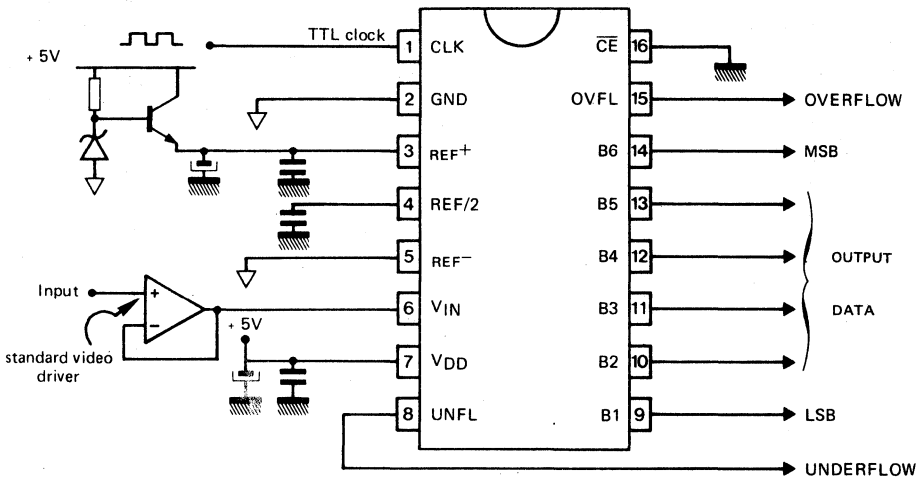
T_{amb} = +25 °C, V_{DD} = + 5 V, V_{REF+} = + 2 V, V_{REF-} = 0V

Characteristic	Symbol	Min	Typ	Max	Unit
Resolution	N	–	–	6	BIT
Integral linearity error	I_{LE}	0	± 1/2	0	LSB
Differential linearity error	D_{LE}	–	–	1/4	LSB
Quantizing error	Q_E	– 1/2	–	+ 1/2	LSB
Voltage supply	V_{DD}	4	5	5.25	V
Power dissipation (15 MHz)	P_D	–	–	120	mW
Maximum sample rate	F_S	–	20	–	MHz
Analog bandwith	F_C	–	10	–	MHz
Aperture jitter	t_a	–	–	250	pS
Reference ladder:					
lower reference voltage	REF^-	– 0.5	0	–	V
upper reference voltage	REF^+	0.8	2	V_{DD} - 1.5	V
full scale range	$REF^+ - REF^-$	–	2	–	–
ladder resistance	R_L	–	1.5	–	kΩ
Input capacitence	C_{in}	–	–	15	pF
Logic output low voltage	V_{OL}	–	–	0.4	V
high voltage	V_{OH}	2.4	–	–	V
Digital input low voltage	V_{IH}	–	–	0.8	V
high voltage	V_{IL}	2.4	–	–	V

TIMING DIAGRAM



TYPICAL CONFIGURATION

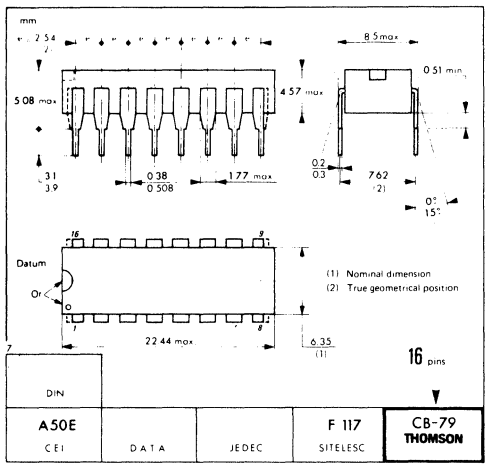


Conventions

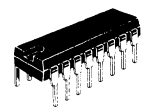
- = Incoming ground pin
- = Ground plane connected to the incoming ground pin

Caution for use

- = 22 µF tantalum capacitors (as near as possible to the incoming ground pin)
- = 100 nF ceramic capacitors (as near as possible to the device pin)
- Avoid DC current flows in the ground plane
- Try to respect star connections for high DC current flows (connection to the incoming pin)



CB-79

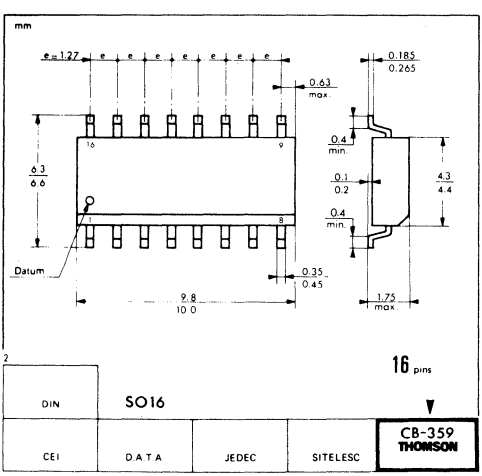


P SUFFIX
PLASTIC PACKAGE

ALSO AVAILABLE

C SUFFIX
CERAMIC PACKAGE

J SUFFIX
CERDIP PACKAGE



CB-359

FP SUFFIX
PLASTIC PACKAGE

NOTES

ADVANCE INFORMATION

VIDEO SPEED 8-BIT FLASH A/D CONVERTER

The TS8308 is a monolithic 8-bit HMOS2 parallel (flash) A/D converter designed for 20 MSPS conversion speed.
Parallel sampling is performed via resistor ladder and 256 comparators. Conversion is accomplished within one pulse.
A very low input capacitance (less than 30 pF) and a low input dynamic range (1 V possible) allow a very easy drive of the TS8308.

Typical characteristics:

- Single +5 V supply.
- ±1 LSB integral non linearity.
- ±0.5 LSB differential non linearity.
- 20 MHz sampling rate.
- 5 MHz input signal without sample and hold adjunction.
- Very low input capacitance (max. 25 pF).
- All logic inputs and outputs are TTL compatible.
- Data output: 8-bit binary code + overflow.
- Output buffers for 8-bit data and overflow are 3-state type.
- Accuracy better than 6 mV.
- Pin to pin compatible with RCA CA 3308.

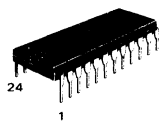
Typical applications:

- TV video digitizing.
- Ultrasound signature analysis.
- Transient signal analysis.
- Radar pulse analysis.
- High energy physics research.
- High speed oscilloscope storage/display.
- General purpose hybrid ADCs.
- Optical character recognition.
- Digital signal processor data acquisition systems.
- Satellite operations.
- Portable video speed products.
- Video printer.
- Fax machine.
- Image processing.
- Medical imaging.
- All high speed A/D conversion applications where low power and low cost are required.

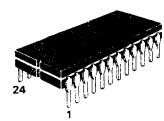
HMOS2

VIDEO SPEED 8-BIT FLASH A/D CONVERTER

CASE CB-68



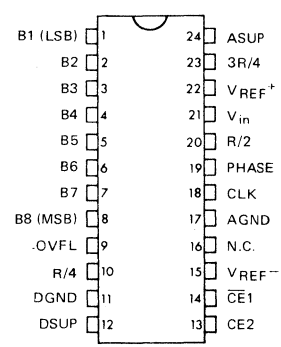
P SUFFIX
PLASTIC PACKAGE



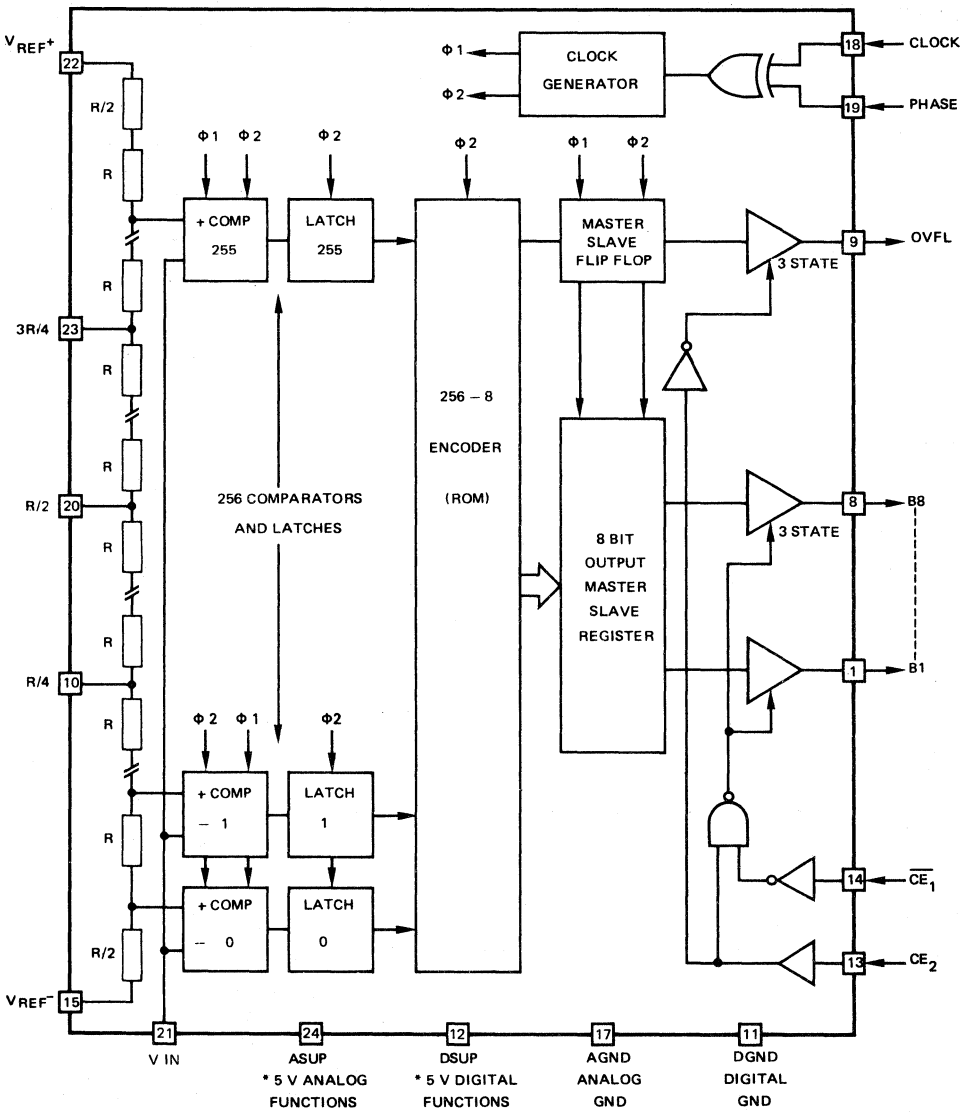
J SUFFIX
CERDIP PACKAGE

Ceramic package (C Suffix) is also available

PIN ASSIGNMENT



BLOCK DIAGRAM



PIN DESCRIPTION

Name	Type	Number	Function	Description
B_1 (LSB) to B_8 (MSB)	O	1 to 8	Output data	Tristate buffer outputs
OVFL	O	9	Overflow status line	This line is set to logical "1" when the input signal is higher than the $V_{REF}+$ voltage. All data (B_1 to B_8) are set to logical "1".
R/4	I	10	First quarter reference	Access to the first quarter reference voltage
DGND	I	11	Digital ground	
DSUP	I	12	Digital supply	
CE2	I	13	Tristate command	CE2 = "0" : tristate for both overflow status and data lines
$\overline{CE1}$	I	14	Tristate command	CE2 = "1" : overflow valid Iout data lines valid only if $\overline{CE1}$ = "0".
$V_{REF}-$	I	15	Lower reference	Access to the lower reference voltage. A voltage source must be applied (or ground)
NC		16	Non connected	
AGND	I	17	Analog ground	
CLK	I	18	Clock input	TTL levels
PHASE	I	19	Phase input	When phase is "0" the input signal is sampled on the failing edge of the input clock. When phase is "1" " the input signal is sampled on the rising edge of the input clock
R/2	I	20	Half reference	Access to the half reference voltage
V_{IN}	I	21	Analog input	
$V_{REF}+$	I	22	Upper reference	Access to the upper reference voltage. A voltage source must be applied
3 R/4	I	23	Third quarter reference	Access to the third quarter reference voltage
ASUP	I	24	Analog supply	

MAXIMUM RATINGS

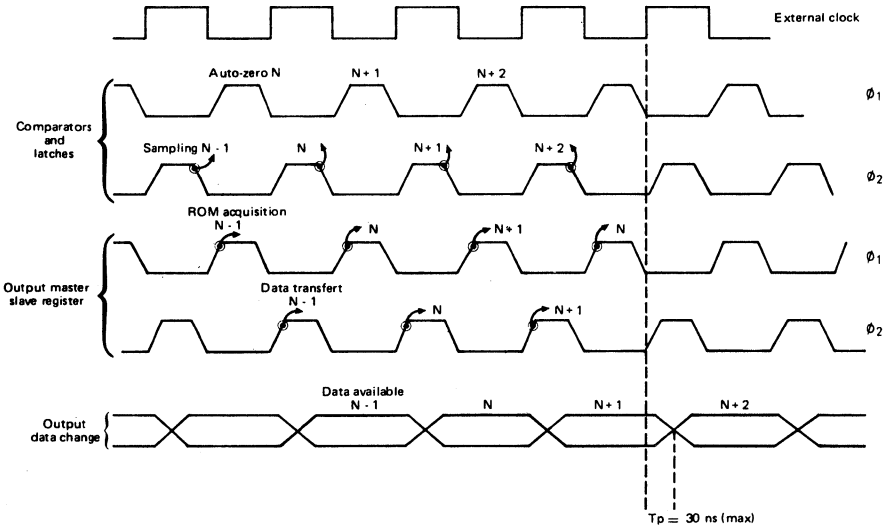
Rating	Symbol	Value	Unit
Supply voltage	V_{DD}	0 to + 7	V
Storage temperature	T stg	- 60 to + 150	°C
Operating temperature	T oper	- 60 to + 130	°C
Power supply current on pins (2,7)	I_7, I_2	150	mA

ELECTRICAL CHARACTERISTICS

T_{amb} = + 25 °C $A_{SUP} = D_{SUP}$ = +5 V V_{REF+} = +2 V V_{REF-} = 0 V

Characteristic	Symbol	Min	Typ	Max	Unit
Resolution	N	—	—	8	Bits
Linearity error	ILE	—	± 1/2	—	LSB
Differential linearity error	DLE	—	± 1/4	—	LSB
Quantizing error	QE	- 1/2	—	+ 1/2	LSB
Voltage supply	ASUP, DSUP	4	5	5.25	V
Power dissipation (15 MHz) : Analog supply	P_{DA}	—	150	—	mW
Digital supply	P_{DD}	—	250	—	mW
Maximum sample rate	F_s	15	20	—	MSPS
Analog bandwith	F_c	—	5	—	MHz
Aperture jitter	t_a	—	—	250	ps
Reference ladder :					
Lower reference voltage	V_{REF-}	- 0.5	0	—	V
Upper reference voltage	V_{REF+}	1	2	V_{DD} - 1.5	V
Full scale range	$V_{REF+} - V_{REF-}$	1	2	V_{DD} - 1.5	V
Ladder resistance	R_{REF}	400	650	900	Ω
Input capacitance	C_{in}		25	30	pF
Logic output low voltage	V_{OL}	—	—	0.4	V
high voltage	V_{OH}	2.4	—	—	V
Digital input low voltage	V_{IH}	—	—	0.8	V
high voltage	V_{IL}	2.4	—	—	V

TIMING DIAGRAM (PHASE = " O ")



NB : If phase is set to "1", the external clock is inverted inside the circuit

FUNCTIONAL DESCRIPTION

Circuit TS8308 includes:

- a sequencer generating internal clock,
- a core ensuring conversion,
- an output circuit delivering digital data,
- the sequencer generates 6 internal clocks from pins CLK and PHASE:

Internal phases	Circuits concerned	Function	Value (PHASE = 0)
Φ 1	Comparators	Autozero	$\overline{CLK}$
Φ 2	Comparators	Sampling and comparison	CLK
Φ 3	Latches	Storage	Φ 2 + D
Φ 4	Encoder	Transmission	Φ2 + D
Φ 5	Output master/slave flip - flop	Sampling	Φ 1 + D
Φ 6	Output master/slave flip - flop	Storage	Φ 2 + D

N.B. : D is a time-delay introduced to compensate for signal propagation time.

- the core includes:
  - A resistor linear network delivering 256 reference voltages distributed linearly between external reference voltages V_{REF}^+ and V_{REF}^-. Access to quarter (R/4), half (R/2) and three quarter (3R/4) bridges enable the following:
    - either improve linearity by externally forcing reference voltages,
    - filter disturbances going through the bridge by means of external capacitors,
    - or delinearize the bridge by means of external resistors (law of linear compression by blocks).
  - A set of 256 voltage comparators parallel connected across the 256 taps of the reference bridge and the input analog signal which defines the 256 (2^8) quantification levels.
    In first phase Φ1, these comparators store their flip-flop threshold then, in phase Φ2 they compare the thresholds with the input signal.
    The comparators with an input signal voltage lower than the reference voltage present a given state at the output, the others present the complementary state.
    The 256 comparators output is stored in 256 latches at the end of phase Φ3 = Φ2.
  - A 256 to 8 decoder detecting the transition between the comparators in a given state and the ones in the complementary state.
    The line enabled corresponds to the last comparator which has tripped, i.e. the comparator with the reference voltage nearest by default to the input signal.
  - A ROM following the decoder and coding over 8 bits the detected comparison chain in binary.
    If the input signal is lower than the lowest reference voltage (1st comparator), code 0 is written at the output.
    If the input signal is higher than the upper most reference voltage (256th comparator), code 255 is written at the output and overflow bit is set to 1.
- The output stage consists of 9 identical parts (8 bits and overflow) each formed of a flip-flop D connected to the ROM output with an output buffer. This buffer is enabled on phase Φ6 = Φ2 and includes a selective high impedance command.
  Inputs $\overline{CE1}$ and CE2 switch the output bits to this 3rd state (with overflow bit if required) in order to facilitate the following*:
  - parallel connection of the 2 converters thus providing a double sampling frequency while maintaining an 8 bit resolution,
  - series connection of the 2 converters providing a 9 bit resolution while maintaining a 20 MHz sampling frequency.

$\overline{CE1}$	CE2	B1,...B8 in 3rd state	B9 (OVFL) in 3rd state
0	0	Yes	Yes
0	1	No	No
1	0	Yes	Yes
1	1	Yes	No

* See application information.

TYPICAL EVALUATION CIRCUIT

The general circuit used for the flash converter in typical conditions (8 bits, 20 MHz) is represented on figure 1.

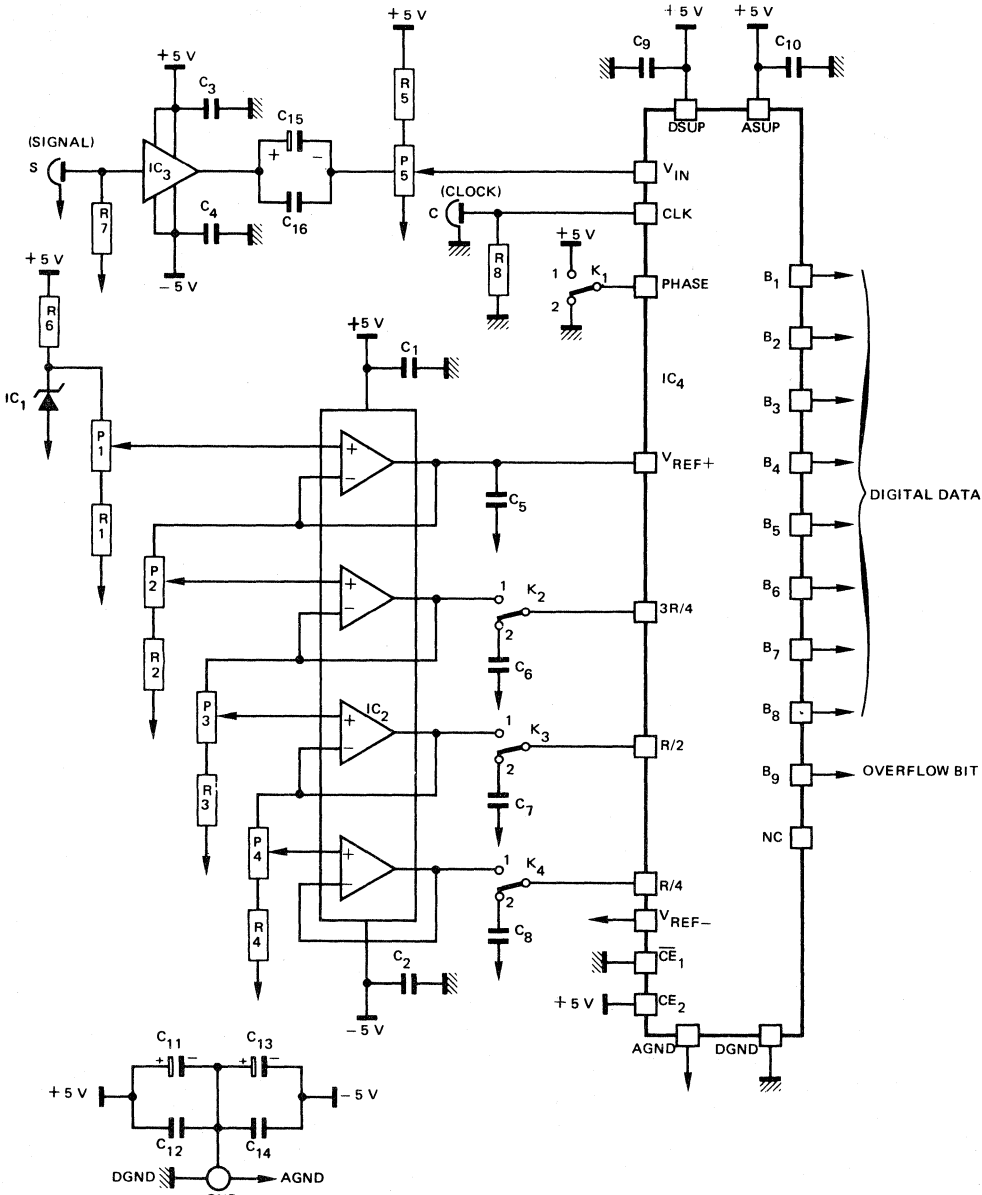
- Voltage reference.
  Flash converter requiring a positive reference voltage (V_{REF}^+) ranging from 1.5 V to 3 V (typ: 2 V), the circuit generates a reference voltage of 2.5 V from the power supply voltage (+5 V) and a precision regulation diode (IC_1).
- Resistor bridge reference voltages.
  The circuit allows to access some particular points on the resistor bridge. These points correspond to 3/4, 1/2 and 1/4 of the bridge total resistance. This feature enables use of the flash convertor in two ways:
  - — in linear operation with these 3 points grounded by uncoupling capacitors in order to filter disturbances along the bridge (K2, K3 and K4 in position 2),
  - — in non-linear operation with the following 2 functions:
    - improvement in flash converter integral linearity by forcing the 3 points to their corresponding voltages (K2, K3 and K4 on poisition 1),
    - implementation of a non-linear conversion law (compression law for instance) in order to better observe the results of the conversion on one part only of the transfer characteristic (K2, K3, K4 on position 1).
- Analog signal.
  The input analog signal must be driven by a wide band buffer amplifier (IC_3) with a very low output impedance.

* For typical application circuit, the same surroundings can be used.

In order to eliminate the almost uncontrollable offsets introduced by the source generator or buffer amplifier proper, two capacitors parallel mounted (C_{15} and C_{16}) are added in series after the amplifier.
For low frequencies (< 1MHz) tantalum capacitor (C_{15}) is used as a short-circuit; for higher frequencies (> 1 MHz) the ceramic capacitor (C_{16}) is used as a short-circuit.
After these capacitors, a potentiometer (P5) with the middle point connected to the flash converter input adds a DC component to the input signal. The signal thus obtained has an overage value different from zero, lying between V_{REF}^- and V_{REF}^+ and which can be converted by the flash converter.

- Clock signal.
  Clock signals are TTL or CMOS signals. The PHASE command is used to invert (K_1 on position 1) or not (K_1 on position 2) the external signal.
- Considerations on electrical layout.
  A certain number of elementary precautions should be taken in the electrical layout when using high frequencies.
  The main ones are as follows:
  - — a ground plane for the components,
  - — the ground tracks corresponding to the various signals (clock, input signal, references) are separated and connected together to a single point,
  - — a star distributed power supplies (idem for ground) to avoid any possible loop,
  - — a maximum capacitive uncoupling as close as possible to each circuit.

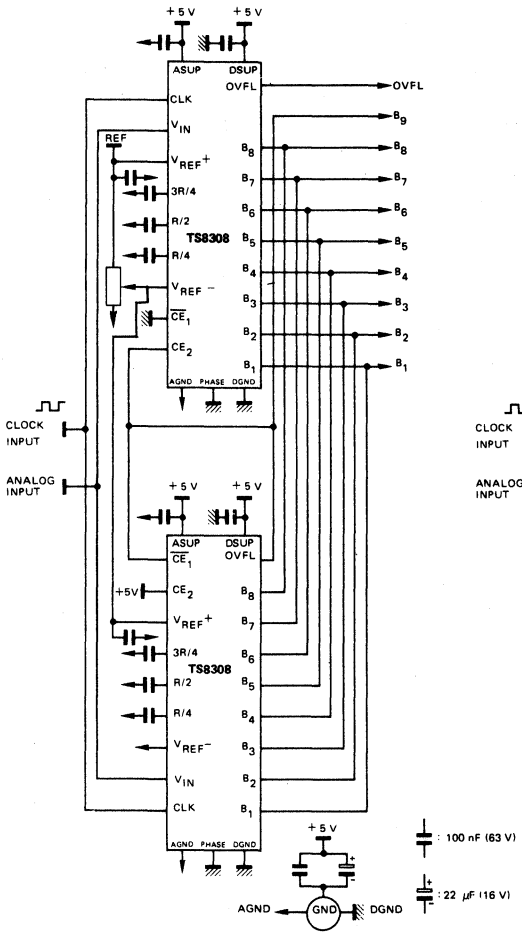
TYPICAL EVALUATION CIRCUIT
(continued)



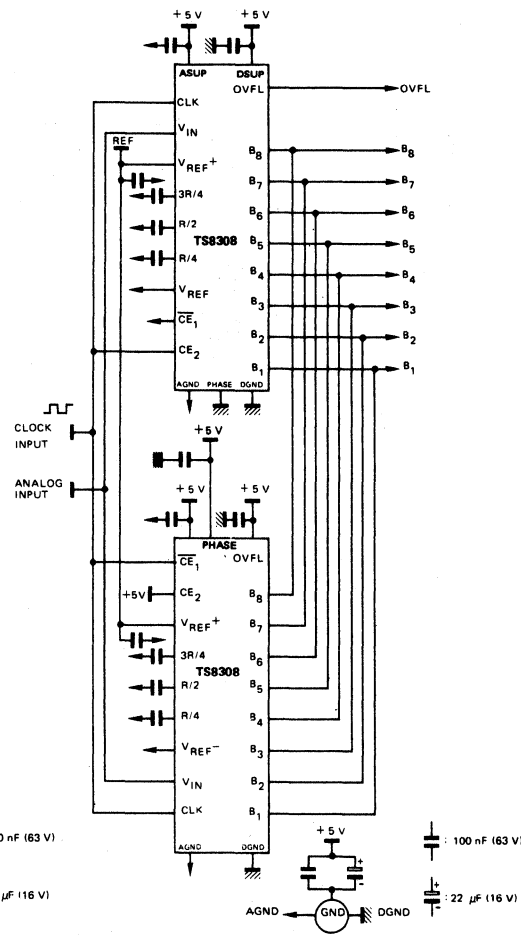
8 BIT RESOLUTION CONFIGURATION 20 MHZ SAMPLING RATE

Component	Value	Component	Value
R1	5.6 KΩ (1/4 W)	C1	100 nF 63 V
R2	3.3 KΩ (1/4 W)	C2	100 nF 63 V
R3	1.2 KΩ (1/4 W)	C3	100 nF 63 V
R4	560 Ω (1/4 W)	C4	100 nF 63 V
R5	10 KΩ (1/4 W)	C5	100 nF 63 V
R6	2 KΩ (1/4 W)	C6	100 nF 63 V
R7	47Ω (1/4 W)	C7	100 nF 63 V
R8	47 Ω (1/4 W)	C8	100 nF 63 V
P1	10 KΩ (multiturns)	C9	100 nF 63 V
P2	10 KΩ (multiturns)	C10	100 nF 63 V
P3	10 KΩ (multiturns)	C11	22 μF 16 V (Tantalum)
P4	10 KΩ (multiturns)	C12	100 nF 63 V
P5	10 KΩ (multiturns)	C13	22 μF 16 V (Tantalum)
IC1	TDB 0136	C14	100 nF 63 V
IC2	TDB 0084	C15	68 μF 16 V (Tantalum)
IC3	LH 0002	C16	100 nF 63 V
IC4	TS 8308		

TYPICAL APPLICATION



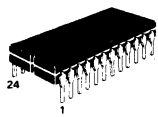
TYPICAL TS8308 9 BIT RESOLUTION CONFIGURATION
20 MHz SAMPLING RATE



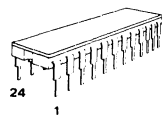
TYPICAL TS8308 8 BIT RESOLUTION CONFIGURATION
40 MHz SAMPLING RATE

CASE

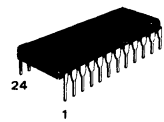
CB-68



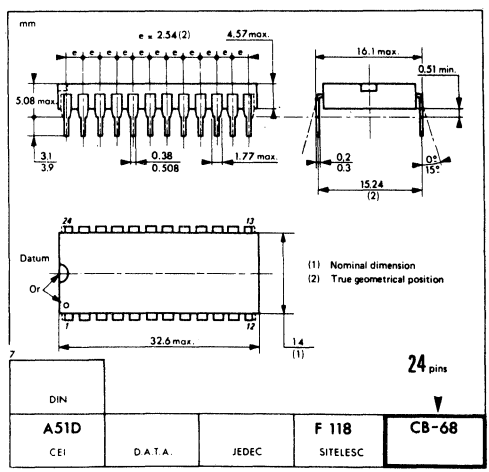
J SUFFIX
CERDIP PACKAGE



C SUFFIX
CERAMIC PACKAGE



P SUFFIX
PLASTIC PACKAGE



NOTES

THOMSON COMPONENTS
MOSTEK

TS8328

VIDEO SPEED 8-BIT FLASH A/D CONVERTER

COMMUNICATIONS PRODUCTS

ADVANCE INFORMATION

VIDEO SPEED 8-BIT FLASH A-D CONVERTER

The TS8328 is the minimal configuration (20 pins) of the TS8308 (24 pins) full flash ADC.
This monolithic parallel A/D converter is designed for 20MSPS conversion rate. Sampling is performed via a resistor ladder and 256 auto-balanced high speed and high accuracy comparators. Conversion is accomplished within one clock pulse.
A very low input capacitance (less than 25 pF) and a low input dynamic range (1 V possible) allow a very easy drive of the TS8328.

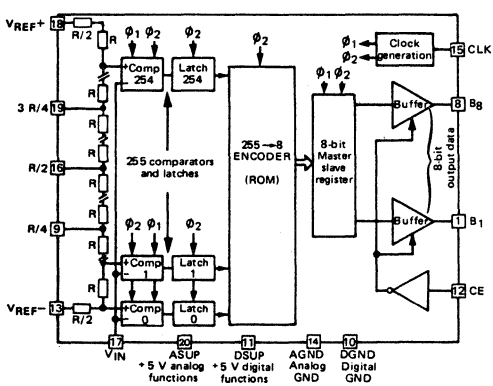
Typical characteristics:

- Single +5 V supply.
- ±1 LSB integral non linearity.
- ±0.5 LSB differential non linearity.
- 20 MHz sampling rate.
- 5 MHz input signal without sample and hold adjunction.
- Very low input capacitance (max 25 pF).
- All logic inputs and outputs are TTL compatible.
- Data output: 8-bit binary code.
- Output buffers for 8-bit data are 3-state type.
- Accuracy better than 6 mV.
- 20 pins slim line package (0.3 inch).

Typical applications:

- Pulse coding for high energy physics experiments.
- High speed data acquisition and instrumentation.
- TV and video digitizing.
- Radar pulse coding.
- Medical and industrial imaging.
- Optical recognition.
- All high speed A/D conversion applications where low power and low cost are required.

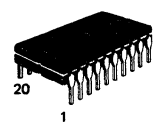
BLOCK DIAGRAM



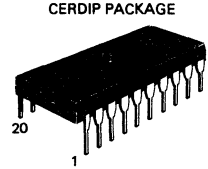
HMOS2

VIDEO SPEED 8 BIT FLASH ADC

CASE CB-194



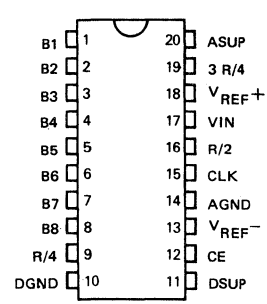
J SUFFIX
CERDIP PACKAGE



P SUFFIX
PLASTIC PACKAGE

* Ceramic package (C Suffix) is also available.

PIN ASSIGNMENT



PIN DESCRIPTION

Name	Type	N°	Function	Description
B_1 (LSB) to B_8 (MSB)	O (MSB)	1 to 8	Output data	Tristate buffer outputs
R/4	I	9	First quarter reference	Access to the first quarter reference voltage
DGND	I	10	Digital ground	
DSUP	I	11	Digital supply	
CE	I	12	Tristate command	Commands the 3 state mode for data lines CE = "0" : 3 state CE = "1" : data valid
V_{REF}-	I	13	Lower reference	Access to the lower reference voltage. A voltage source must be applied (or ground).
AGND	I	14	Analog ground	
CLK	I	15	Clock input	The input signal is sampled on the falling edge of the clock. Output data are changing on the next rising edge.
R/2	I	16	Half reference	Access to the half reference voltage.
VIN	I	17	Signal input	
V_{REF}+	I	18	Upper reference	Access to the upper reference voltage. A voltage source must be applied.
3 R/4	I	19	Third quarter reference	Access to the third quarter reference voltage.
ASUP	I	20	Analog supply	

MAXIMUM/RATINGS

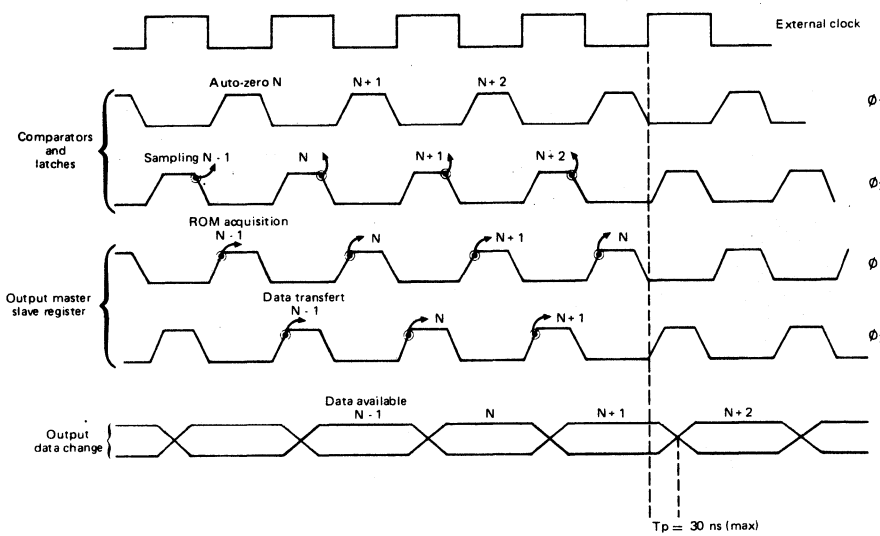
Rating	Symbol	Value	Unit
Supply voltage	V_{DD}	- 0.3 to + 7	V
Storage temperature	t_{stg}	- 60 to 150	°C
Operating temperature	t_{oper}	- 60 to 130	°C
Power supply current	I_{10}, I_{11}, I_{14}, I_{20}	150	mA

ELECTRICAL CHARACTERISTICS

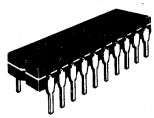
T_{amb} = + 25 °C ASUP = DSUP = + 5 V V_{REF+} = + 2 V V_{REF-} = 0 V

Characteristic	Symbol	Min	Typ	Max	Unit
Resolution	N			8	Bits
Linearity error	ILE		± 1		LSB
Differential linearity error	DLE		± 1/2		LSB
Quantizing error	QE	- 1/2		+ 1/2	LSB
Voltage supply	ASUP, DSUP	4	5	5.25	V
Power dissipation (15 MHz) : Analog supply	P_{DA}		300		mW
Digital supply	P_{DD}		100		mW
Maximum sample rate	F_S	15	20		MSPS
Analog bandwidth	F_c		5		MHz
Aperture jitter	t_a			250	ps
Reference ladder :					
Lower reference voltage	V_{REF-}	0	0		V
Upper reference voltage	V_{REF+}		2	V_{DD} - 15	V
Full scale range	$V_{REF+} - V_{REF-}$	1	2	V_{DD} - 1.5	V
Ladder resistance	R_{REF}	500	650	800	Ω
Input capacitance	C_{in}		25	30	pF
Logic output low voltage	V_{OL}			0.4	V
high voltage	V_{OH}	2.4			V
Digital input low voltage	V_{IH}			0.8	V
high voltage	V_{IL}	2.4			V

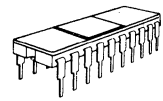
TIMING DIAGRAM



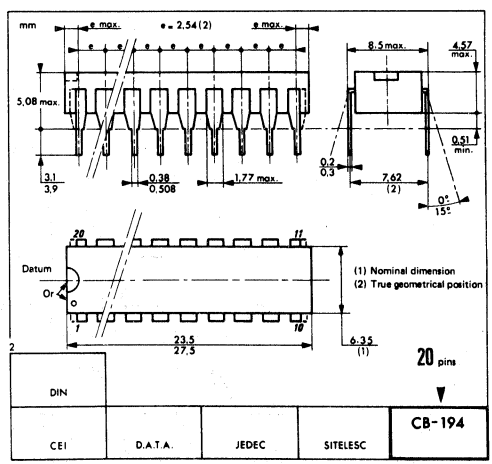
CASE CB-194



J SUFFIX
CERDIP PACKAGE



C SUFFIX
CERAMIC PACKAGE



CHAPTER 7 - INTEGRATED CIRCUITS SHORT FORM CATALOG

Summary

ASIC PRODUCTS

SEA-OF-GATES

ISB 12000 SERIES

FEATURES

- 1.2 micron HCMOS process, poly silicide gates, 2-layer metal with Titanium barriers and hermetic silicon nitride passivation.
- 2-input NAND gate delay=0.3ns, Fanout=2, T_A=25°C, V_{DD}=5V.
- Channelless architecture utilizing transistor gate isolation.
- Gate count ranging from 8,000 to 128,000.
- Extensive macrocell, macrofunction and megacell library elements available.
- Full function TTL and CMOS I/O cells.
- Configurable drive up to 8 mA with slew rate control. Buffers may be paralleled to generate 16 mA of source/sink drive.
- Augmented metal grid to maximize power distribution.
- VAX based design system, interfaces from multiple workstations.
- Latch-up trigger current >1 A. ESD protection >2000 V. Short circuit protection.
- ISB054 evaluation device available.
- Full military capability.
- Broad ceramic and plastic package offering.

PRODUCT OUTLINE

DEVICE NUMBER	INTERNAL CELLS	GATE (1) COMPLEXITY	ESTIMATED (2) USEABLE GATES	TOTAL (3) DEVICE PADS	MAXIMUM I/O
ISB12008	20,000	8,000	3,000	88	76
ISB12011	28,800	11,520	4,500	104	92
ISB12015	39,200	15,680	6,000	120	108
ISB12020	51,200	20,480	8,000	136	120
ISB12025	64,800	25,920	10,000	152	136
ISB12038	96,800	38,720	15,000	184	164
ISB12054	135,200	54,080	20,000	216	200
ISB12076	192,200	76,880	30,000	256	232
ISB12103	259,200	103,680	40,000	296	256 (4)
ISB12128	320,000	128,000	50,000	328	256 (4)

NOTES:

1. A factor of 2.5 is used to derive gate complexity from raw cells.
2. A conservative routing efficiency of 40% is quoted. This number will vary depending on the design.
3. Eight dedicated Vdd/Vss pads. I/O pads may be reconfigured for additional Vdd/Vss pads.
4. I/O signals currently limited to 256 by tester constraints.

ABSOLUTE MAXIMUM RATINGS (REFERENCE TO VSS)

SYMBOL	PARAMETER	VALUE	UNIT
V_{DD}	DC SUPPLY VOLTAGE	−0.5 to + 7.0	V
V_I	INPUT VOLTAGE	−0.5 to V_{DD}+0.5	V
I_I	DC INPUT CURRENT	±20	mA
T_{TSTG}	STORAGE TEMP. RANGE (CERAMIC)	−65 to 150	°C
T_{STG}	STORAGE TEMP. RANGE (PLASTIC)	−40 to 125	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	VALUE	UNIT
V_{DD}	DC SUPPLY VOLTAGE	+3 to + 6	V
T_A	OPERATING AMBIENT (MILITARY)	−55 to +125	°C
T_A	OPERATING AMBIENT (INDUSTRIAL)	−40 to +85	°C
T_A	OPERATING AMBIENT (COMMERCIAL)	0 to 70	°C

PACKAGE SELECTOR GUIDE FOR THE ISB 12000 SERIES

DEVICE NUMBER	TOTAL (3) DEVICE PADS	CERAMIC AND PLASTIC PIN GRID ARRAY					PLASTIC AND CERAMIC CHIP CARRIERS		PLASTIC QUAD FLAT PACK	
		84	120	180	224	296	68	84	100	132
ISB 12008	88	X					X	X		
ISB 12011	104	X					X	X	X	
ISB 12015	120	X	X				X	X	X	X
ISB 12020	136	X	X				X	X	X	X
ISB 12025	152		X	X			X	X		X
ISBM 12038	184		X	X						X
ISB 12054	216			X	X					
ISB 12076	256			X	X	X				
ISB 12103	296			X	X	X				
ISB 12128	328			X	X	X				

TELECOMMUNICATIONS/DATA COMMUNICATIONS

DATA COMMUNICATION CIRCUITS

PART NO.	TECHNOLOGY	FUNCTION	SUPPLY	PINS/PACKAGE
ETHERNET				
MK68590	NMOS	Local Area Network Controller for Ethernet (LANCE),	5V	48 DIP
MK68591	Bipolar	Serial Interface Adapter (SIA) with 10 Mbps Manchester encoder/decoder for Ethernet	5V	24-DIP 600 mil width
MK68592	Bipolar	Serial Interface Adapter (SIA) same as 68591, but in smaller package	5V	24 DIP 300 MIL width
STARLAN				
MK5030	CMOS	StarLAN Hub - 12 port, cascadable (Demo board available)	5V	48 DIP
MK5033	CMOS	General purpose std/diff. Manchester encoder/decoder	5V	28 DIP
MK5035	CMOS	StarLAN Station	5V	20 DIP
MK50351	CMOS	StarLAN Station for use with variable bit rate controller	5V	20 DIP
PACKET SWITCHING				
MK5025	CMOS	CCITT, X.25 LAPB/LAPD controller 1980 & 1984 specification compatible	5V	48 DIP
MK5027*	CMOS	CCITT, Common Channel Signalling System Number Seven (SS7)	5V	48 DIP

SWITCHING

Switching connection and concentration

PART NO.	TECHNOLOGY	FUNCTION	SUPPLY	PINS
EF73321	NMOS	PCM clock recovery and transceiver.	+ 5	16

Subscriber Board: Single channel CODEC plus filters

PART NO.	TECHNOLOGY	FUNCTION	SUPPLY	PINS
ETC5057	CMOS	Single channel A-law serial COFIDEC compatible with NSC TP3057	± 5V	16
ETC5054	CMOS	Single channel μ-law serial COFIDEC compatible with NSC TP3054	± 5V	16
ETC5067	CMOS	Single channel A-law serial COFIDEC with push-pull power amplifiers	± 5V	20
ETC5064	CMOS	Single channel μ-law serial COFIDEC with push-pull power amplifiers	± 5V	20
TS5070* TS5071*	CMOS	2nd generation COFIDEC programmable functions and direct interface to SLIC	± 5V	20

* To be introduced

TELECOMMUNICATIONS/DATA COMMUNICATIONS

SWITCHING

Subscriber Board (Continued)

PART NO.	TECHNOLOGY	FUNCTION	SUPPLY	PINS
ETC5040	CMOS	PCM filters for use with MK5116 series, compatible with TP3040	± 5V	16

TRANSIENT PROTECTION

PART NO.	TECHNOLOGY	FUNCTION	PACKAGE
TPA62 To TPA270	Bipolar	Bidirectional transient protection breakdown voltage 62V = TPA62 270V = TPA270 Max Power = 1.3W	Axial Leads F126
TPB62 To TPB270	Bipolar	Bidirectional transient protection breakdown voltage 62V = TPB62 270V = TPB270 Max Power = 5W	Axial Leads CB429
TPC62 To TPC270	Bipolar	Dual bidirectional transient protection breakdown voltage 62V = TPC62 270V = TPC270 Max Power = 20W	To 220

TELEPHONE SET

PART NO.	TECHNOLOGY	FUNCTION	SUPPLY	PINS
TEA3046	Bipolar	Telephone transmission and DMTF Dialer	Line supply	28
TEA7031	Bipolar	Telephone loudspeaker amplifier.	Line supply	28
TEA7531	Bipolar	Telephone loudspeaker amplifier	Line supply	16
EFG71891	CMOS	DTMF generator for binary coded hexadecimal data 8 pin package with serial input port	+3 to 5.25V	14 8

TELECOMMUNICATIONS/DATA COMMUNICATIONS

TELEPHONE SET

PART NO.	TECHNOLOGY	FUNCTION	SUPPLY	PINS
MK5370	CMOS	TonePulse™ switchable dialer, with last # redial	2.5V to 6.5V	18
MK5371	CMOS	TonePulse™ switchable dialer, with BCD input and last # redial	2.5V to 6.5V	18
MK53721*	CMOS	TonePulse™ WORLD DIALER™ with redial and options for various countries standards	2.5V to 6V	20
MK5375	CMOS	TonePulse™ switchable dialer with 10 number memory	+2.5V to +6.0V	18
MK5376	CMOS	TonePulse™ switchable dialer with 10 number memory for European market	2.5V to 6.0V	24
MK5380	CMOS	Low cost tone only dialer	2.5V to 10.0V	16
MK53731	CMOS	Full feature TonePulse™ switchable dialer with last number redial	2.5V to 6V	18
MK53761*	CMOS	Full feature TonePulse™ repertory dialer with 10 number memory	2.5V to 6V	18
MK53762*	CMOS	TonePulse™ repertory dialer. 10 number memory uses one key per number location for recall	2.5V to 6V	20
MK53763**	CMOS	TonePulse™ WORLD DIALER™ with 13 number memory, single key auto-dialing, and various country options.	2.5 V to 6V	24 300 MIL width

* To be introduced in 1Q'88
** To be introduced in 3Q'88

HIGH SPEED DATA CONVERSION

PART NO.	FUNCTION	SAMPLING RATE	SUPPLY	PINS
TS8328	8-bit flash A/D Converter (min. version of TS8308)	20 MHz	+5V	20

TELECOMMUNICATIONS/DATA COMMUNICATIONS

MODEMs

PART NO.	TECHNOLOGY	FUNCTION	BAUD RATE	SUPPLY
EFG7515	CMOS	Monochip DPSK modem. CCITT-V22 and BELL212A (Demo board available).	Tx: 1200/300 Rx: 1200/300 Full Duplex	±5V
TDA7868	Bipolar	Direct connect circuit for modem interfaces to phone line. Provides line adaptation and ring detection.	NA	Telephone Line Supply
TS68930	HMOS2	High performance (IO MIPS, 160 ns cycle) Digital Signal Processor (Emulator board available)	25 MHz	5V
TS68931	HMOS2	External ROM version of TS68930	25 MHz	5V
TS68950	CMOS	Modem analog front end transmitter	V.22, V.32 up to 19200 bps	±5V
TS68951	CMOS	Modem analog front end receiver	V.22, V.32 up to 19200 bps	±5V
TS68952	CMOS	Modem analog front end XMIT/RCVR Clock generator	V.22, V.32 up to 19200 bps	±5V

ISDN

PART NO.	TECHNOLOGY	FUNCTION	SUPPLY	PINS
TBD*	CMOS	ISDN transceiver "S" interface device	+5V	20
TBD*	CMOS	HDLC controller	+5V	28
TBD*	CMOS	U interface	+5V	TBD
TBD*	CMOS	ISDN power supply	Phone line	18
TBD*	CMOS	Telephone set COFIDEC	Phone line	TBD

* To be announced

MILITARY PRODUCTS

MEMORIES

PART NO.	DESCRIPTION	ORG.	ACCESS TIME	GRADE
MKB4116	DRAM	16K × 1	150, 200, 250 ns	883 (Last Time Buy)
MKJ4116	DRAM	16K × 1	200, 250 ns	JAN (Last Time Buy)
MKB/J4564	DRAM	64K × 1	120, 150, 200 ns	883/DESC/JAN
MKB/J45F56	DRAM	256K × 1	100, 120, 150 ns	883/DESC/JAN
MKB41H68	CMOS SRAM	4K × 4	25, 35, 45 ns	883/DESC
MKB41H87	CMOS SRAM	64K × 1	35, 45, 55 ns	To be intro.
MKB48H64	CMOS SRAM	8K × 8	35, 45, 55 ns	To be intro.
MKB/J4501	Biport FIFO	512 × 9	65, 80, 100, 120, 150, 200 ns	883/JAN
MKB4505	Biport FIFO	1K × 5	35, 45, 55 ns	To be intro.

4-BIT MICROPROCESSORS 2900 FAMILY

PART NO.	FUNCTION	ALT. SOURCE	PINS	GRADE
TS2901BMCB/B	4-bit bipolar microprocessor slice	Am2901B	40	883
TS2901CMCB/B	Improved speed 4 Bit microprocessor slice	AM2901C	40	883
TS2910MCB/B	Microprogram controller	Am2910	40	883
TS2911AMCB/B	Microprogram sequencer	Am2911A	20	883
TS2914MCB/B	Vectored priority interrupt controller	Am2914	40	883
TS2915AMCB/B	Quad 3-State Bus Transceiver with interface logic	Am2915A	24	883
TS2917AMCB/B	Quad 3-State Bus Transceiver with interface logic	Am2917A	20	883
TS2918MCB/B	Quad D register with standard and 3-State Outputs	Am2918	16	883
TS2919MCB/B	Quad D register with Dual 3-State Outputs	Am2919	20	883

MILITARY PRODUCTS

8-BIT MICROPROCESSORS 6800 FAMILY

PART NO.	TECHNOLOGY	CLOCK FREQ. (MHz)	GRADE
EF6800MCB/B	NMOS	1,1.5	883
EF6802MCB/B	NMOS	1,1.5	883
EF6809MCB/B	HMOS	1,1.5	883
EF6821MCB/B	NMOS	1,1.5	883
EF6840MCB/B	NMOS	1,1.5	883
EF6850MCB/B	NMOS	1,1.5	883
EF6852MCB/B	NMOS	1,1.5	883
EF6854MCB/B	NMOS	1,1.5	883
EF6810MCB/B	NMOS	1,1.5	883

Available in ceramic and cerdip DIL packages as well as ceramic chip-carriers.

16-BIT MICROPROCESSORS 68000 FAMILY

PART NO.	TECHNOLOGY	CLOCK FREQ. (MHz)	GRADE
MKB/J68000P	HMOS	4,6,8,10,12	883/DESC/JAN
MKB68901P	NMOS	4,5	883
TS68000MCB/C	HMOS	8,10,12	883
TS68008MCB/B	HMOS	8,10,12	883

Also available in ceramic DIL packages, pin-grid arrays and ceramic or chip-carrier.

TS68230MCB/B	HMOS	8,10	883

Available in ceramic DIL package and ceramic chip-carrier.

MICROPROCESSORS/MICROCONTROLLERS

DEVELOPMENT & EMULATION 8-BIT

PART NO.	FUNCTION
TST IN48	General purpose development tool for 4 and 8 bit micros
EFT-MU94	ET9400 family (CMOS and NMOS) emulator
EFT-MUP4 EFT-MUP5	EF6804P2/J2, EF68HC04P3 emulator EF6805P2/P4/P6, EF6805R2/U2, EF6805R3/U3 emulator

4-BIT MICROPROCESSORS 2900 FAMILY

PART NO.	FUNCTION	ALT. SOURCE	PINS
TS2901B TS2901C	4-bit bipolar microprocessor slice Improved speed 4 Bit microprocessor slice	Am2901B Am2901C	40 40
TS2902A	High speed look-ahead carry generator	Am2902A	16
TS2909A	Microprogram sequencer	Am2909A	28
TS2910	Microprogram controller	Am2910	40
TS2911A	Microprogram sequencer	Am2911A	20
TS2914	Vectored priority interrupt controller	Am2914	40
TS2915A	Quad 3-State Bus Transceiver with interface logic	Am2915A	24
TS2917A	Quad 3-State Bus Transceiver with interface logic	Am2917A	20
TS2918	Quad D register with standard and 3-State Outputs	Am2918	16
TS2919	Quad D register with Dual 3-State Outputs	Am2919	20

MICROPROCESSORS/MICROCONTROLLERS

8-BIT MICROPROCESSORS 6800 FAMILY

PART NO.	TECHNOLOGY	CLOCK FREQ. (MHz)	FEATURES	ALT. SOURCE	PINS
EF6802 EF68A02 EF68B02	NMOS	1 1.5 2	6800 MPU, 128 bytes of RAM, on-chip oscillator	MC6802 MC68A02 MC68B02	40
EF6803 EF68A03 EF68B03	HMOS	1 1.5 2	8-bit microp., 16-bit add. bus, Multiply, RAM: 128b, SCI-Timer	MC6803 MC68A03 MC68B03	40
EF6803U4 EF68A03U4 EF68B03U4	HMOS	1 1.5 2	Same as above but: RAM: 192b, enhanced timer	MC6803U4 MC68A03U4 MC68B03U4	40
EF6809 EF68A09 EF68B09	HMOS	1 1.5 2	High performance 8-bit MPU, 6800 compatible, On-chip oscillator	MC6809 MC68A09 MC68B09	40
EF6809E EF68A09E EF68B09E	HMOS	1 1.5 2	High performance 8-bit MPU, 6800 compatible, External clock	MC6809E MC68A09E MC68B09E	40
TS68008-8 TS68008-10 TS68008-12	HMOS	8 10 12.5	16-bit microprocessor with 8-bit data bus	MC68008-8 MC68008-10 MC68008-12	40

Available in plastic, ceramic, cerdip DIL packages and plastic or ceramic chip-carriers.

8-BIT PERIPHERALS 6800 FAMILY

PART NO.	TECHNOLOGY	CLOCK FREQ. (MHz)	FEATURES	ALT. SOURCE	PINS
EF6821 EF68A21 EF68B21	NMOS	1 1.5 2	Peripheral Interface Adapter (PIA)	MC6821 MC68A21 MC68B21	40
EF6840 EF68A40 EF68B40	NMOS	1 1.5 2	Programmable Timer Module (PTM)	MC6840 MC68A40 MC68B40	28
EF6850 EF68A50 EF68B50	NMOS	1 1.5 2	Asynchronous Communication Interface Adapter (ACIA)	MC6850 MC68A50 MC68B50	24
EF6854 EF68A54 EF68B54	NMOS	1 1.5 2	Advanced Data-Link Controller (ADLC)	MC6854 MC68A54 MC68B54	28

8-BIT PERIPHERALS 3880 FAMILY

PART NO.	TECHNOLOGY	CLOCK FREQ. (MHz)	FEATURES	ALT. SOURCE	PINS
MK3801-04 MK3801-06	NMOS	4 6	Serial timer interrupt (STI)	—	40

* To be introduced

Available in plastic DIL package.

MICROPROCESSORS/MICROCONTROLLERS

16-BIT MICROPROCESSORS 68000 FAMILY

PART NO.	TECHNOLOGY	CLOCK FREQ. (MHz)	FEATURES	ALT. SOURCE	PINS
TS68000-8	HMOS	8	16-bit microprocessor with 32-bit internal structure	MC68000-8	64
TS68000-10		10		MC68000-10	
TS68000-12		12.5		MC68000-12	
TS68000-16		16		—	
TS68008-8	HMOS	8	TS68000 8-bit bus version	MC68008-8	48
TS68008-10		10		MC68008-10	
TS68008-12		12.5		MC68008-12	

* To be introduced

Also available in ceramic and plastic DIL packages, pin-grid arrays and ceramic or plastic chip-carrier.

16-BIT PERIPHERALS 68000 FAMILY

PART NO.	TECHNOLOGY	CLOCK FREQ. (MHz)	FEATURES	ALT. SOURCE	PINS
MK68230-8	HMOS	8	Parallel interface/timer	MC68230-8	48
MK68230-10		10		MC68230-10	
MK68564	HMOS	4,5	Serial I/O	—	48
TS68HC901	HCMOS	4,5,8	CMOS multifunction peripheral	—	48
MK68901	HMOS	4,5	Multifunction peripheral	MC68901	48
TS68930	HMOS2	6.25	High performance digital signal processor with internal program ROM 160 μs cycle time, 2 × 128 × 16-bit internal RAM	—	48
TS68931	HMOS2	6.25	ROMLESS version of TS68930 64K addressing range	—	84
MK68590	NMOS	10	Local Area Network Controller for Ethernet (LANCE), cheapernet	AM7990	48 DIP
MK68591	Bip	10	Serial Interface Adapter (SIA) with 10 Mb/s Manchester encoder/decoder for Ethernet, cheapernet, etc.	—	24 DIP 600 MIL width
MK68592	Bip	10	Serial Interface Adapter (SIA) same as 68591, but in smaller package	AM7992	24 DIP 300 MIL width

Available in plastic and ceramic DIL packages, plastic chip carrier packages.

MICROPROCESSORS/MICROCONTROLLERS

4-BIT MICROCONTROLLERS 9400 FAMILY

PART NO.	TECHNOLOGY	ROM × 8	RAM × 4	I/O LINES	INSTRUCTION CYCLE (μs)	SUPPLY (V)	ALT. SOURCE	PINS
ETL9410/11/13	NMOS Low Power	512	32	19/16/15	15-40	4.5-6.3	COP410L/11/13L	24/20
ETC9410/11/13	CMOS	512	32		4-DC	2.4-5.5	COP410C/11C/13C	24/20
ET9420/21/22	NMOS	1024	64	23/19/15	4-10	4.5-6.3	COP420/21/22	28/24/20
ETL9420/21/22	NMOS Low Power	1024	64		15-40	4.5-6.3	COP420L/21L/22L	28/24/20
ETC9420/21/22	CMOS	1024	64		4-DC	2.4-5.5	COP424C/25C/26C	28/24/20
ETL9444/45	NMOS Low Power	2048	128	23/19	15-40	4.5-6.3	COP444L/45L	28/24
ETC9444/45	CMOS	2048	128		4-DC	2.4-5.5	COP444C/45C	28/24

*To be introduced

Common features: software compatible (same instruction set). Pin compatible. Three levels of stack. 8 bidirectional tristate I/O. Serial I/O and internal counter, interrupt programmable I/O. All devices are with plastic package (DIL) and also SOIC and PLCC for some devices. Available with extended temperature range (−40°C to +85°C): ET93XX or ETC93XX.

8-BIT MICROCONTROLLERS 6804 FAMILY

PART NO.	TECHNOLOGY	ROM × 8	RAM × 8	I/O	ALT. SOURCE	PINS
EF6804P2	HMOS	1024	32	20	MC6804P2	28
EF6804J2	HMOS	1024	32	12	MC6804J2	20
EF68HC04J3*	HCMOS	2048	124	12	MC68HC04J3	20
EF68HC04P3	HCMOS	2048	124	20	MC68HC04P3	28

Available in plastic, ceramic, DIL packages or chip-carriers. All software compatible. Timer.

8-BIT MICROCONTROLLERS 6805 FAMILY

PART NO.	TECHNOLOGY	ROM × 8	RAM × 8	I/O	FEATURES	ALT. SOURCE	PINS
EF6805P2	HMOS	1100	64	20	—	MC6805P2-HD6805S1	28
EF6805P6	HMOS	1796	64	20	—	MC6805P6	28
EF6805R2	HMOS	2048	64	32	A/D Converter	MC6805R2	40
EF6805R3	HMOS	3776	112	32	A/D Converter	MC6805R3-HD6805W0	40
EF6805T2	HMOS	2508	64	19	On-chip PLL	MC6805T2	28
EF6805U2	HMOS	2048	64	32	—	MC6805U2	40
EF6805U3	HMOS	3776	112	32	—	MC6805U3	40

Available in plastic, ceramic, DIL packages or chip-carrier. Ext. temp range (−40°C, +85°C). All software compatible. Interrupt capabilities. Timer.

MICROPROCESSORS/MICROCONTROLLERS

8-BIT MICROCONTROLLERS MK3870 FAMILY

PART NO.	TECHNOLOGY	ROM × 8	RAM × 8	I/O	FEATURES	ALT. SOURCE	PINS
MK2870/10	NMOS	1024	64	20	—	M2872	28
MK3870/10	NMOS	1024	64	32	—	M3872	40
MK3870/20	NMOS	2048	64	32	—	M3870.2	40
MK3870/22	NMOS	2048	128	32	—	M3872	40
MK3870/40	NMOS	4096	64	32	—	M3872	40
MK3870/42	NMOS	4032	128	32	—	M3872	40
MK3873/22	NMOS	2048	128	29	SI, SO, SLCK	M38730,33	40
MK3875/22	NMOS	2048	128	29	SI, SO, SLCK	M3875	40
MK3875/42	NMOS	4032	128	29	SI, SO, SLCK	M3875	40

Common features: Software compatible (same instruction set), timer, interrupt capabilities, parallel I/O (TTL compatible).
All devices are with plastic or ceramic package (DIL).
Also available with extended temperature range.

8-BIT MICROCONTROLLERS EF6801 FAMILY

PART NO.	TECHNOLOGY	ROM × 8	RAM × 8	I/O	FEATURES	ALT. SOURCE	PINS
EF6801	HMOS	2048	128	31	SCI, Timer, stand-by RAM	MC6801 HD6801-S0	40
EF6801-U4	HMOS	4096	192	31	Enhanced SCI and Timer Stand-by RAM	MC6801-U4 HD6801-V0	40

Common features: 8 x 8 multiply instruction. Timer. 64K byte addressing space. Serial communication interface. All devices available in DIL ceramic or plastic package and plastic chip carrier (PLCC)/−40°C to +85°C).

STANDARD MICROCONTROLLERS MK38P70 (97xxx) FAMILY

PART NO.	TECHNOLOGY	ADDRESSABLE ROM × 8	ON CHIP RAM × 8	I/O	FEATURES	SUPPORT	PINS
MK97400	NMOS	4096	128	32	TTL Ports	4K EPROM	40 (24/28)
MK97403	NMOS	4096	128	32	TTL Ports	4K EPROM	40 (24/28)
MK97410	NMOS	4096	128	32	Open drain ports	4K EPROM	40 (24/28)
MK97501	NMOS	65472	128	32	TTL ports	8K EPROM	40 (28)
MK97521	NMOS	65472	128	32	Open drain and TTL ports	8K EPROM	40 (28)

Common features: EPROM version of MK3870, piggyback ceramic package accepts 24 or 28 pins memories, pin to pin compatible with 3870. Available in extended temperature range.

MICROPROCESSORS/MICROCONTROLLERS

GRAPHIC CIRCUITS

PART NO.	TECHNOLOGY	FEATURES	ALT. SOURCE	PINS
EF9345	HMOS	Single chip alphanumeric and semigraphic display processor 25/21 rows of 40 or 80 characters. Color, B/W		40
EF9367	HMOS	Graphic display processor. Up to 512 × 1024 interlaced 50/60 Hz - Color, B/W		40
EF9369	HMOS	Palette circuit 16 × 4096 compatible with all display circuits	**	28
EF9370	HMOS	Enhanced version of 9369	**	28
TS68483	HMOS	High performance drawing processor	**	68
TS68493	HMOS	Enhanced version of 68483	**	68
TS68494	HMOS	Palette circuit 256 × 4096	**	48

** Alternate source to be announced.

MEMORIES

ZEROPOWER™ CMOS SRAMs

DEVICE	ORGANIZATION	ACCESS TIME	I_{CC}	I_{SB}	FEATURES	TEMP RANGE	PINS	PKGS
MK48Z02	2K × 8	120,150,200, 250 ns	80 mA	1 mA	ZEROPOWER	C, I	24	B
MK48Z12	2K × 8	120,150,200, 250 ns	80 mA	1 mA	V_{CC} = ±10%	C, I	24	B
MK48Z08	8K × 8	150,200,250 ns	80 mA	1 mA	ZEROPOWER	C	28	B
MK48Z09	8K × 8	150,200,250 ns	80 mA	1 mA	Power Fail Interrupt Output	C	28	B
MK48Z18	8K × 8	150,200,250 ns	80 mA	1 mA	V_{CC} = ±10%	C	28	B
MK48Z19	8K × 8	150,200,250 ns	80 mA	1 mA	Power Fail Interrupt Output V_{CC} = ±10%	C	28	B
MK48Z32	32K × 8	150,200 ns	85 mA	10 mA	ZEROPOWER	C	28	B

Common Features: Integral lithium battery for data retention in the absence of power. U.L. recognized versions available; designated MK48ZxxBU.

TIMEKEEPER™ CMOS SRAMs

DEVICE	ORGANIZATION	ACCESS TIME	I_{CC}	I_{SB}	FEATURES	TEMP RANGE	PINS	PKGS
MK48T02	2K × 8	120,150,200 250 ns	80 mA	3 mA	TIMEKEEPER	C	24	B
MK48T12	2K × 8	120,150,200, 250 ns	80 mA	3 mA	V_{CC} = ±10%	C	24	B

Common Features: CMOS SRAMS containing real time clock, crystal, and lithium battery in a single package. U.L. recognized versions available; designated MK48TxxBU.

BATTERY BACK-UP CMOS SRAMs

DEVICE	ORGANIZATION	ACCESS TIME	I_{CC}	I_{BAT}	TEMP RANGE	PINS	PKGS
MK48C02A	2K × 8	150,200,250 ns	80 mA	1μA	C	28	N

STATIC RAMs

DEVICE	ORGANIZATION	ACCESS TIME	I_{CC}	I_{SB}	TEMP RANGE	PINS	PKGS
ET2147H	4K × 1	35,55 ns	180 mA	30 mA	C	18	J

*** To be introduced**

MEMORIES

VERY FAST CMOS STATIC RAMs

DEVICE	ORGANIZATION	ACCESS TIME	I_{CC}	I_{SB}	FEATURES	TEMP RANGE	PINS	PKGS
MK41H66	16K × 1	20,25,35 ns	120 mA	—	Fast $\overline{CS}$ Access	C	20	N
MK41H67	16K × 1	20,25,35 ns	120 mA	50μA	$\overline{CE}$ Power Down	C	20	N
MK41H68	4K × 4	20,25,35 ns	120 mA	50μA	$\overline{CE}$ Power Down	C	20	N
MK41H69	4K × 4	20,25,35 ns	120 mA	—	Fast $\overline{CS}$ Access	C	20	N
MK41H79	4K × 4	20,25,35 ns	120 mA	—	$\overline{CE}$/OE/CLR	C	22	N
MK48H64*	8K × 8	35,45,55 ns	90 mA	10μA	$\overline{E_1}$, E_2 Power Down	C	28	N
MK41H87*	64K × 1	35,45,55 ns	60 mA	50μA	$\overline{CE}$ Power Down	C	24	N

CMOS CACHE TAGRAMs

DEVICE	ORGANIZATION	ACCESS TIME	I_{CC}	I_{SB}	FEATURES	TEMP RANGE	PINS	PKGS
MK41H80	4K × 4	20,25,35 ns	120 mA	—	Cache Comparator w/$\overline{CLR}$	C	22	N
MK4202	2K × 20	20,25 ns	200 mA	—	Cache Comparator w/$\overline{CLR}$	C	68	K
MK48H74*	8K × 8	35,45,55 ns	—	—	Cache Comparator w/$\overline{CLR}$	C	28	N
MK4850*	512 × 9	20 ns	95 mA	—	Cache Comparator w/$\overline{CLR}$	C	24	N
MK4852*	2K × 9	20 ns	125 mA	—	Cache Comparator w/$\overline{CLR}$	C	28	N

CMOS BiPORT FIFOs

DEVICE	DESCRIPTION	ACCESS TIME	CYCLE TIME	I_{CC}	TEMP RANGE	PINS	PKGS
MK4501	BiPort FIFO 512 × 9	65,80,100,120, 150,200 ns	80,100,120,140, 175,235 ns	80 mA	C	28,32	N,K
MK4503	BiPort FIFO 2K × 9	65,80,100,120, 150,200 ns	80,100,120,140, 175,235 ns	120 mA	C	28,32	N,K
MK4505M	Clocked FIFO 1K × 5	15,20,25 ns	25,33,50 ns	100 mA	C	24	N
MK4505S	Clocked FIFO 1K × 5 (3 State Outputs)	15,20,25 ns	25,33,50 ns	100 mA	C	20	N
MK45264/5	(64 × 5) × 2 (BiDirectional FIFO)	50 ns	60 ns	60 mA	C	24	N

CMOS BiPORT RAMs

DEVICE	DESCRIPTION	ACCESS TIME	CYCLE TIME	I_{CC}	TEMP RANGE	PINS	PKGS
MK4511	BiPort RAM 512 × 9	120,150,200 ns	150,190,250 ns	50 mA	C	28,32	N
MK4532*	Dual Port RAM 2K × 8 (Master)	55,70,90 ns	55,70,90 ns	60 mA	C	48,52	N,K
MK4532A*	Dual Port RAM 2K × 8 (Master)	30,35,45 ns	30,35,45 ns	60 mA	C	48,52	N,K
MK4542*	Dual Port RAM 2K × 8 (Slave)	55,70,90 ns	55,70,90 ns	60 mA	C	48,52	N,K
MK4542A*	Dual Port RAM 2K × 8 (Slave)	30,35,45 ns	30,35,45 ns	60 mA	C	48,52	N,K
MK45AM8*	16K Dual Port RAM w/×8 and ×16 Ports ×8 Port A/D Multiplexed	60,70 ns	60,70 ns	60 mA	C	68	K
MK45DP8*	16K Dual Port RAM w/×8 and ×16 Ports	60,70 ns	60,70 ns	60 mA	C	68	K

* To be introduced

Package Type: J CERDIP
N Plastic DIP
K Plastic Leadless Chip Carrier
E Ceramic Leadless Chip Carrier
B Plastic DIP w/Top Hat

Temperature Range: C 0°C to +70°C
I −40°C to +85°C

MEMORIES

NMOS EPROMs

DEVICE	ORGANIZATION	ACCESS TIME	CONSUMPTION	TEMP RANGE	PINS
ET2716	2K × 8	350,450 ns	525/132 mW	C	24

CMOS EPROMs

DEVICE	ORGANIZATION	ACCESS TIME	CONSUMPTION	TEMP RANGE	PINS
ETC2716	2K × 8	450,550 ns	25/0.5 mW	C,E,V	24
ETC2732	4K × 8	350,450,550 ns	25/0.5 mW	C,E,V	24
TS27C64	8K × 8	250,300 ns	150/2.5 mW	C,V	28
TS27C256*	32K × 8	150,200,250,300 ns	200/2.5 mW	C,V	28
TS27C1024*	64K × 16	120,150,200,250 ns	250/5.0 mW	C,V	40
TS27C1001*	128K × 8	120,150,200,250 ns	250/5.0 mW	C,V	32

CMOS EEPROMs

DEVICE	ORGANIZATION	ACCESS TIME	CONSUMPTION	DATA RETENTION	TEMP RANGE	PINS
TS59C11*	64K × 16 or 128K × 8	—	15/.5 mW	10 yrs	C	8
TS93C46*	64K × 16 or 128K × 8	—	15/.5 mW	10 yrs	C	8
TS28C16A*	2K × 8	150 ns	125/.5 mW	10 yrs	C	24
TS28C17A*	2K × 8	150 ns	125/.5 mW	10 yrs	C	24
TS28C64*	8K × 8	150,200,250 ns	150/.5 mW	10 yrs	C	28

ONE-TIME PROGRAMMABLE CMOS ROMs

DEVICE	ORGANIZATION	ACCESS TIME	CONSUMPTION	TEMP RANGE	PINS	PKGS
TS27C64	8K × 8	150,200,250,300 ns	150/2.5 mW	C,V,T	28,32	P,FN
TS27C256*	32K × 8	150,200,250,300 ns	200/2.5 mW	C,V,T	28,32	P,FN
TS27C1024*	64K × 16	120,150,200,250 ns	250/5.0 mW	C,V	40,44	P,FN
TS27C1001*	128K × 8	120,150,200,250 ns	250/5.0 mW	C,V	32	P

* To be introduced

Package Type: P Plastic DIP
FN Plastic Leadless Chip Carrier

Temperature Range: C 0°C to +70°C
E −25°C to +70°C
V −40°C to +85°C
T −40°C to +105°C

MEMORIES

BIPOLAR PROMs

PART NO.	TECHNOLOGY	ORGANIZATION	OUTPUT	ACCESS TIME (t_{ACC} max)	SUPPLY	PINS
TS71181A*	H BIP II	1K × 8	3-state	45 ns	+5V	24
TS71181B*	H BIP II	1K × 8	3-state	35 ns	+5V	24
TS71181C*	H BIP II	1K × 8	3-state	25 ns	+5V	24
TS71281A*	H BIP II	1K × 8	3-state	45 ns	+5V	24 (Slim line)
TS71281B*	H BIP II	1K × 8	3-state	35 ns	+5V	24 (Slim line)
TS71281C*	H BIP II	1K × 8	3-state	25 ns	+5V	24 (Slim line)
TS71191A	Advanced TTL	2K × 8	3-state	60 ns	+5V	24
TS71191B	Advanced TTL	2K × 8	3-state	45 ns	+5V	24
TS71191C	Advanced TTL	2K × 8	3-state	35 ns	+5V	24
TS71191D	Advanced TTL	2K × 8	3-state	25 ns	+5V	24
TS71291C	H BIP II	2K × 8	3-state	35 ns	+5V	24 (Slim line)
TS71291D	H BIP II	2K × 8	3-state	25 ns	+5V	24 (Slim line)
TS71321B*	H BIP II	4K × 8	3-state	55 ns	+5V	24
TS71321C*	H BIP II	4K × 8	3-state	45 ns	+5V	24
TS71641*	H BIP II	8K × 8	3-state	55 ns	+5V	24

* To be introduced

LINEAR

AUTO-PROTECTED CONTROLS DRIVERS (LAMPS, RELAYS, TRIACS, MOTORS...)

PART NO.	FEATURES	TEMPERATURE RANGE (•)	PACKAGES (2)
TDE1607	V_{CC} = 36V, I_{OUT} = 0.3 A	I	CM, DP
TDE1647	V_{CC} = 45V, I_{OUT} = 0.3 A	I	CM, DP, FP
TDE1737	V_{CC} = 45V, I_{OUT} = 0.3 A	I	CM, DP, FP
TDE1747	V_{CC} = 45V, I_{OUT} = 0.3 A	I	CM, DP, FP
TDE1767,A	V_{CC} = 45V, I_{OUT} = 0.5 A	I	DP
TDF1778	V_{CC} = 32V, I_{OUT} = 2 A (Dual)	F	SP
TDF1779,A	V_{CC} = 35V, I_{OUT} = 2 A (Dual)	F	SP
TDE1787,A	V_{CC} = 60V, I_{OUT} = 0.3 A	I	DP
TDE1798	V_{CC} = 35V, I_{OUT} = 0.5 A	I	DP
TDE3207	V_{CC} = 36V, I_{OUT} = 0.15 A	I	DP, FP
TDE1780*	V_{CC} = 35V, I_{OUT} = 2 A (Dual)	I	DP, SP

SENSORS-DETECTORS

PART NO.	FEATURES	TEMPERATURE RANGE (1)	PACKAGES (2)
LM135 (235-335,A)	Precision temp. sensors	C, I, M	Z
TDA0159A	Proximity detector	I	FP, DP
TDE0160	Proximity detector	I	FP, DP
TDA0161	Proximity detector	I	CM, DP, FP
TDA0162	Proximity detector	I	CM, DP, FP

J-FET OP-AMPs SINGLE

PART NO.	FEATURES	TEMPERATURE RANGE (1)	PACKAGES (2)
TL061	Low power	C, I, M	DP, FP, DG, GC, H
TL071	Low noise	C, I, M	DP, FP, DG, GC, H
TL081	Standard	C, I, M	DP, FP, DG, GC, H
LF155,A(255,A-355,A)	Low power	C, I, M	DP, DG, GC, H
LF156,A(256,A-356,A)	High speed	C, I, M	DP, DG, GC, H
LF157,A(257,A-357,A)	Very high speed	C, I, M	DP, DG, GC, H

J-FET OP-AMPS DUAL

PART NO.	FEATURES	TEMPERATURE RANGE (1)	PACKAGES (2)
TL062	Low power	C, I, M	DP, FP, DG, GC, H
TL072	Low noise	C, I, M	DP, FP, DG, GC, H
TL082	Standard	C, I, M	DP, FP, DG, GC, H

* Product in development

(1) C = 0 −70: M = −55 −125°: I = −25 −85° or Max Junction Temp = 150°

(2) CM = TO100 Family Metal Can, DP = Dual In Line Plastic, DG = Dual In Line Ceramic, FP = Small Outline IC - Plastic, H = TO99 Metal Can, GC = Ceramic LCC, K = TO3 Metal Can, SP = TO220 Family

LINEAR

J-FET OP-AMPS QUAD

PART NO.	FEATURES	TEMPERATURE RANGE (1)	PACKAGES (2)
TL064	Low power	C, I, M	DP, FP, DG, DC, GC
TL074	Low noise	C, I, M	DP, FP, DG, DC, GC
TL084	Standard	C, I, M	DP, FP, DG, DC, GC

BIPOLAR OP-AMPs SINGLE

PART NO.	FEATURES	TEMPERATURE RANGE (1)	PACKAGES (2)
LM101A(201A, 301A)	Low offset	C, I, M	DP, FP, DG, GC, H
LM108(208-308)	Precision	C, I, M	DP, FP, DG, GC, H
LM118(218-318)	High speed	C, I, M	DP, FP, DG, GC, H
UA709	Standard	M	H
UA741	Standard	C, I, M	DP, FP, DG, GC, H
UA748	Standard	C, M	DP, FP, DG, GC, H
UA776	Programmable	C, M	DP, FP, DG, GC, H
TDB7910	Power op-amp.	C	DP

BIPOLAR OP-AMPS DUAL

PART NO.	FEATURES	TEMPERATURE RANGE (1)	PACKAGES(1)
LM158(258-358)	Single power supply	C, I, M	DP, FP, DG, GC, H
LM1458(1558)	Standard	C, I, M	DP, FP, DG, GC, H
LM2904	Single power supply	I	DP, FP
MC4558	Single power supply, high speed	C, M, I	DP, FP, DG, H
TE.1033	For filter design	I, C•	DP, FP, DG, GC

BIPOLAR OP-AMPS QUAD

PART NO.	FEATURES	TEMPERATURE RANGE (1)	PACKAGES (2)
LM124(224,324)	Single power supply	C, I, M	DP, FP, DG, GC, DC
LM146(246,346)	Programmable	C, I, M	DP, FP, DG, GC
LM148(248,348)	Standard	C, I, M	DP, FP, DG, GC
LM2902	Single power supply	V	DP, FP
MC3303(3403,3503)	Single power supply	C, M	DP, FP, DG, GC
TE.4033	General purpose	B, C•	DP, FP, DG, GC

COMPARATORS SINGLE

PART NO.	FEATURES	TEMPERATURE RANGE (1)	PACKAGES (2)
LM111(211,311)	Standard	C, I, M	DP, FP, DG, GC, H

LINEAR

COMPARATORS DUAL

PART NO.	FEATURES	TEMPERATURE RANGE (1)	PACKAGES (2)
LM119(219,319)	Standard	C, I, M	DP, FP, DG, GC, H
LM193(293,393)	Single power supply	C, I, M	DP, FP, GC, H
LM2903	Single power supply	C	DP, FP

COMPARATORS QUAD

PART NO.	FEATURES	TEMPERATURE RANGE (1)	PACKAGES (2)
LM139,A(239,A-339,A)	Standard	C, I, M	DP, FP, DG, GC, DC
LM2901	Single power supply	I	DP, FP
MC3302	Single power supply	I	DP

VOLTAGE REGULATORS FIXED

PART NO.	OUTPUT VOLTAGE	OUTPUT CURRENT	TEMPERATURE RANGE (1)	PACKAGES (2)
LM109 (209,309)	5V	1.5 A or 2.5 A	C, I, M	H, K
LM123 (223,323)	5V	3 A	C, I, M	K
TEA5110	5V (Dual)	0.1 A	C	DP
UA7805,B	5V	1.5 A	C, I, M	SP, K
UA78S05,B	5V	2 A	C	SP, K
UA7806	6V	1.5 A	C, M	SP, K
UA7808	8V	1.5 A	C, M	SP, K
UA78S09,B	9V	2 A	C	SP, K
UA7812,B	12V	1.5 A	C, I, M	SP, K
UA78S12,B	12V	2 A	C	SP, K
UA7815	15V	1.5 A	C, I, M	SP, K
UA78S15,B	15V	2 A	C	SP, K
UA7818	18V	1.5 A	C, M	SP, K
UA7824	24V	1.5 A	C, M	SP, K
UA7905,B	−5V	1.5 A	C, I, M	SP, K
UA7912,B	−12V	1.5 A	C, I, M	SP, K
UA7915,B	−15V	1.5 A	C, I, M	SP, K

VOLTAGE REGULATORS ADJUSTABLE

PART NO.	OUTPUT VOLTAGE	OUTPUT CURRENT	TEMPERATURE RANGE (1)	PACKAGES (2)
L200	2.85V/32V	2 A	I	SP5
LM105 (205, 305)	4.5V/40V (105, 205) 4.5V/30V (305)	≤25 mA	C, I, M	H
LM117 (217, 317)	1.2V/40V	1.5 A (K, SP) 0.5 A (H)	C, I, M	SP, H, K
LM137 (237, 337)	−1.2V/ −40	1.5 A (K, SP) 0.5 A (H)	C, I, M	S, H, K
LM138 (238, 338)	1.2V/35V	5 A	C, I, M	K
UA723, A	2V/37V	50 mA	C, I, M	DP, FP, DG, H

VOLTAGE REGULATORS WATCHDOG

PART NO.	OUTPUT VOLTAGE	OUTPUT CURRENT	TEMPERATURE RANGE (1)	PACKAGES (2)
TEA7105	5V	100 mA	C, I	DP

LINEAR

VOLTAGE REGULATORS LOW DROP OUT AUTOMOTIVE

PART NO.	OUTPUT VOLTAGE	OUTPUT CURRENT	TEMPERATURE RANGE (1)	PACKAGES (2)
TEA7034	+5V	≥500 mA	C, I	SP5-2
TEA7605*	+5V	500 mA	C	SP

POWER CONTROLLER SWITCH MODE POWER SUPPLY

PART NO.	FUNCTION	PACKAGE (2)
TEA2018A	Power supply control circuit for fixed frequency fly-back power supplies up to 80W. Direct drive of the switching transistor. Output current $I_B = KI_C$. Total protection from overload short-circuit and temperature. Low rest current.	DP-8
TEA2019	Power supply control circuit for fixed frequency fly-back power supplies up to 80W. Direct drive of the switching transistor. Output current $I_B = KI_C$. Total protection from overload, short-circuit and temperature. — Low rest current. — Sync. capability with internal PLL.	DP-14
TEA2162	Control IC for fixed frequency fly-back power supplies up to 200W. In conjunction width TEA2029, this IC provides full secondary regulation for color TV applications (Master/Slave). Optimized power stage drive current. Over-voltage / current protections. Soft-start procedure.	Batwing DP-16
UAA4006B	Control circuit for fixed frequency fly-back power supplies up to 200W. Direct drive of switching transistor with self regulated base current. Reduced storage time. Total protection from overload, short-circuit and temperature. Very low rest current.	DP-16 SP

TIMERS & MISCELLANEOUS

PART NO.	FEATURES	TEMPERATURE RANGE (1)	PACKAGES (2)
LM134 (234-334)	Adj. current source	C, I, M	Z
LM236,A (336,A)	2.5V voltage references	C, I	Z
NE/SE555	Timer	C, I, M	DP, FP, DG, H
NE/SE556	Timer	C, M	DP, FP, DG
ESM683	Analog gate	C	FP
JUCA4532	Thermal printhead driver	C	Chip
UAA4002	Transistor driver	A	DP

MOTOR DRIVERS STEPPER MOTOR CONTROLLERS

PART NO.	TYPE	OUTPUT CURRENT	TEMPERATURE	PACKAGE
TEA3717	Bipolar	1 A	C	DP, SP
TEA3718,S	Bipolar	1.5 A	C	DP, SP
L702	Unipolar	2.0 A	C	DP, SP
UCN4801	Unipolar	400 mA	C	DP
UAA4003	DC	—	C	DP
TDA1154	DC	1.2 A	C	DP
UAA2081	Unipolar	1 A (Dual)	C	DP

CONSUMER CIRCUITS

TELEVISION AND MONITOR DEFLECTION

PART NO.		FUNCTION	PACKAGE (2)
TEA2017	Horizontal and vertical	Complete horizontal and vertical deflection circuit for black and white TV sets. Direct drive of frame yoke (maximum output current: ± 1.5 A), direct drive of line darlington, muting output.	SP-15
TEA2026C		TV scanning and power supply digital processor includes 50-60 Hz identification, security and start-up systems.	DP-28
TEA2029C		TV scanning and power supply digital processor includes 50-60 Hz identification, security and start-up systems. In conjunction with TEA2162, it provides SMPS secondary regulation.	DP-28
TEA2037A		Low cost horizontal and vertical deflection circuit for black and white TV sets and monochrome displays. Direct drive of frame yoke (maximum output current: ± 1 A), direct drive of line darlington.	Batwing DP-16
TBA920,S	Horizontal	Line Oscillator, syn, separator, phase comparator for monochrome TV sets.	DP-16
TDA2593		Line oscillator combination, burst, blanking and frame pulse separation for color TV sets.	DP-16
TEA2031A	Parabolic correction	Ensures the vertical rate, parabolic and keystone correction for 110° screens	DP-8

VIDEO AND SOUND IF CIRCUITS

PART NO.		FUNCTION	PACKAGE (2)
TDA2540	Video IF	IF amplifier with demodulator and AFC (CCIR standard) for NPN tuner.	DP-16
TDA2541		IF amplifier with demodulator and AFC (CCIR standard) for PNP tuner.	DP-16
TDA2542		IF amplifier with demodulator and AFC (French standard).	DP-16
TDA4426		Very stable IF amplifier with demodulator and AFC for PNP tuner.	DP-18
TDA4427		Very stable IF amplifier with demodulator and AFC for PNP tuner and inverted AFC.	DP-18
TDA4443		IF amplifier with demodulator for multistandard applications. High input sensitivity. Large AGC capabilities.	DP-16
TDA4445A	Sound IF	Quasi parallel sound processing with quadrature inter-carrier demodulator. Very high input sensitivity. Good AM suppression.	DP-16
TDA4445B		AM/FM sound demodulator. Low AM distortion. Very high input sensitivity. No adjustment for the AM demodulator.	DP-16

CONSUMER CIRCUITS

PERITELEVISION

PART NO.		FUNCTION	PACKAGE (2)
TEA1014	Video and AF switch	For monosound TV sets. Follows the SCART specifications n° 108.	DP-14
TEA2014	Video switch	Switched 2 Vpp video output. Not switched 75 Ω, 1 Vpp video output.	DP-8
TEA5114,A	R-G-B switch	3-channel high frequency switch (20 MHz), designed for R-G-B and video applications. Low output impedance (75 Ω).	DP-16
TEA5115		5-switch (R-G-B, Fast blanking, Sync.) video signal selector. 25 MHz bandwidth for R-G-B signals.	DP-18

REMOTE CONTROL - CHANNEL SELECTION

PART NO.		FUNCTION	PACKAGE (2)
UAA4000	Transmitter	For ultra-sonic or infra-red transmission, 32 command capability. Pulse position modulation provides excellent noise immunity.	DP-18
UAA4009	Receiver	Complete circuit for PPM demodulation. 12 channel tuning voltage switch (remote and keyboard), one DC voltage output for volume adjustment, standby information.	DP-18
TEA5049	PreAmp	A low cost infra-red preamplifier for remote control reception	DP-14

AUDIO AF AMPLIFIERS

PART NO.	APPLICATION	MAX. VALUES		NORMAL CONDITIONS			NOTE	PACKAGE (2)
		V_{CC}(V)	I_O(A)	V_{CC}(V)	R_L(Ω)	P_O(W)		
TBA820M	Radio and portable recorders	16	1.5	9	8	1.2	—	DP-8
TCA830SM		20	2	9	4	2	—	DP-8
TEA2025B	Portable radio dual AF amplifier	15	1.5	9	4	2.3*	Fully protected	Batwing DP-16
TDA2003	Car radio	18/40**	3.5	14.4	2	10	Fully protected	SP5
TDA2006	TV and record players	30	3	24	4	12	Fully protected	SP5
TDA2030		36/42**	3.5	28	4	18	Fully protected	SP5
TDA2040	Hi-Fi/Stereo TV receivers	40	4	32	4	22 d=0.5%	Fully protected	SP5

*P_O(W) Output per channel except bridge applications (both amplifiers)
**Peak voltage (50 ms)

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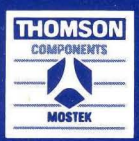

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